VS1307

64 x 8, Serial, I²C Real-Time Clock

REPLACEMENT of DS1307 Series

VER.02-0809 VOSSEL Product Datasheet

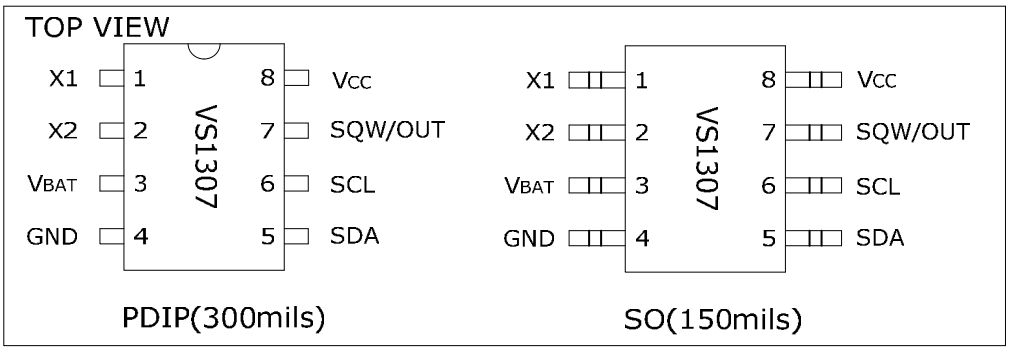
GENERAL DESCRIPTION

The VS1307 serial real-time clock (RTC) is a low-power, full binary-coded decimal (BCD) clock/calendar plus 56 bytes of NV SRAM. Address and data are transferred serially through an I²C, bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator. The VS1307 has a built-in power-sense circuit that detects power failures and automatically switches to the backup supply. Timekeeping operation continues while the part operates from the backup supply.

FEATURES

- Real-Time Clock (RTC) Counts Seconds, Minutes, Hours, Date of the Month, Month, Day of the week, and Year with Leap-Year Compensation Valid Up to 2100
- 56-Byte, Battery-Backed, Nonvolatile (NV) RAM for Data Storage
- I²C Serial Interface, standard mode (100 kHz)
- Programmable Square-Wave Output Signal
- Automatic Power-Fail Detect and Switch Circuitry
- Consumes Less than 500nA in Battery-Backup Mode with Oscillator Running
- Available in 8-Pin PDIP or 8-Pin SOIC for Surface Mount
- Optional Industrial Temperature Range:-40°C to +85°C

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	X1	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance (CL) of 12.5pF. X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, X2, is floated if an external oscillator is connected to X1.
2	X2	
3	V_{BAT}	Backup Supply Input for Any Standard 3V Lithium Cell or Other Energy Source. Battery voltage must be held between the minimum and maximum limits for proper operation. Diodes in series between the battery and the VBAT pin may prevent proper operation. If a backup supply is not required, VBAT must be grounded. The nominal power-fail trip point (VPF) voltage at which access to the RTC and user RAM is denied is set by the internal circuitry as 1.25 x VBAT nominal. A lithium battery with 48mAhr or greater will back up the VS1307 for more than 10 years in the absence of power at +25°C.
4	GND	Ground
5	SDA	Serial Data Input/output. SDA is the data input/output for the I^2C serial interface. The SDA pin is open drain and requires an external pull up resistor.
6	SCL	Serial Clock Input. SCL is the clock input for the I^2C interface and is used to synchronize data movement on the serial interface.
7	SQW/OUT	Square Wave/Output Driver. When enabled, the SQWE bit set to 1, the SQW/OUT pin outputs one of four square-wave frequencies (1Hz, 4kHz, 8kHz, 32kHz). The SQW/OUT pin is open drain and requires an external pull up resistor. SQW/OUT operates with either VCC or VBAT applied.
8	V_{CC}	Primary Power Supply. When voltage is applied within normal limits, the device is fully accessible and data can be written and read. When a backup supply is connected to the device and VCC is below VTP, read and writes are inhibited. However, the timekeeping function continues unaffected by the lower input voltage.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground.....-0.5V to +7.0V
Operating Temperature Range (No condensing) Commercial.....0°C to +70°C
Industrial.....-40°C to +85°C
Storage Temperature Range.....-55°C to +125°C
Soldering Temperature (DIP, leads).....+260°C for 10 seconds
Soldering Temperature (surface mount).....See JPC/JEDEC Standard J-STD-020

NOTE: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.*

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to +70°C, TA = -40°C to +85°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	VCC		4.5	5.0	5.5	V
Logic 1 Input	VIH		2.2		VCC + 0.3	V
Logic 0 Input	VIL		-0.3		+0.8	V
VBAT Battery Voltage	VBAT		2.0	3	3.5	V

DC ELECTRICAL CHARACTERISTICS

(VCC = 4.5V to 5.5V; TA = 0°C to +70°C, TA = -40°C to +85°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNTIX
Input Leakage (SCL)	ILI		-1		1	µA
I/O Leakage (SDA, SQW/OUT)	ILO		-1		1	µA
Logic 0 Output (IOL = 5mA)	VOL				0.4	V
Active Supply Current (fSCL = 100kHz)	ICCA				1.5	mA
Standby Current	ICCS	(Note 3)			200	µA
VBAT Leakage Current	IBATLKG			5	50	nA
Power-Fail Voltage (VBAT = 3.0V)	VPF		1.216 x VBAT	1.25 x VBAT	1.284 x VBAT	V

DC ELECTRICAL CHARACTERISTICS

(VCC = 0V, VBAT = 3.0V; TA = 0°C to +70°C, TA = -40°C to +85°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VBAT Current (OSC ON); SQW/OUT OFF	IBAT1			300	500	nA
VBAT Current (OSC ON); SQW/OUT ON (32kHz)	IBAT2			480	800	nA
VBAT Data-Retention Current (Oscillator Off)	IBATDR			10	100	nA

WARNING: Negative undershoots below -0.3V while the part is in battery-backed mode may cause loss of data.

AC ELECTRICAL CHARACTERISTICS

(VCC = 4.5V to 5.5V; TA = 0°C to +70°C, TA = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	fSCL		0		100	kHz
Bus Free Time Between a STOP and START	tBUF		4.7			µs

Condition						
Hold Time (Repeated) START Condition	tHD:STA	(Note 4)	4.0			µs
LOW Period of SCL Clock	tLOW		4.7			µs
HIGH Period of SCL Clock	tHIGH		4.0			µs
Setup Time for a Repeated START Condition	tSU:STA		4.7			µs
Data Hold Time	tHD:DAT		0			µs
Data Setup Time	tSU:DAT	(Notes 5, 6)	250			ns
Rise Time of Both SDA and SCL Signals	tR				1000	ns
Fall Time of Both SDA and SCL Signals	tF				300	ns
Setup Time for STOP Condition	tSU:STO		4.7			µs

CAPACITANCE

(TA = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pin Capacitance (SDA, SCL)	CI/O				10	pF
Capacitance Load for Each Bus Line	CB	(Note 7)			400	pF

Note 1: All voltages are referenced to ground.

Note 2: Limits at -40°C are guaranteed by design and are not production tested.

Note 3: ICCS specified with VCC = 5.0V and SDA, SCL = 5.0V.

Note 4: After this period, the first clock pulse is generated.

Note 5: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the VIH(MIN) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 6: The maximum tHD:DAT only has to be met if the device does not stretch the LOW period (tLOW) of the SCL signal.

Note 7: CB—total capacitance of one bus line in pF.

TIMING DIAGRAM

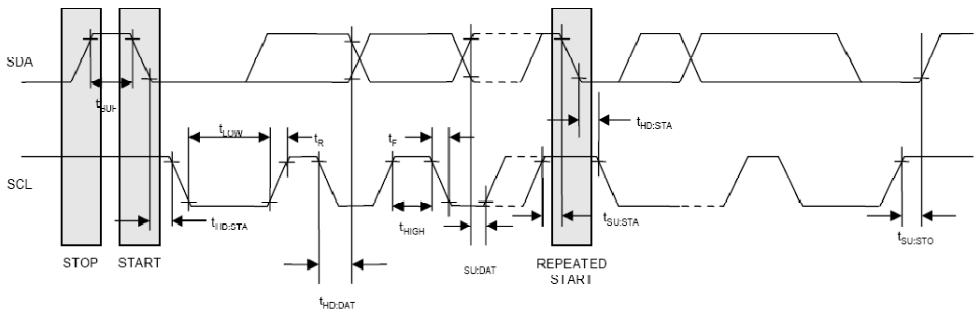
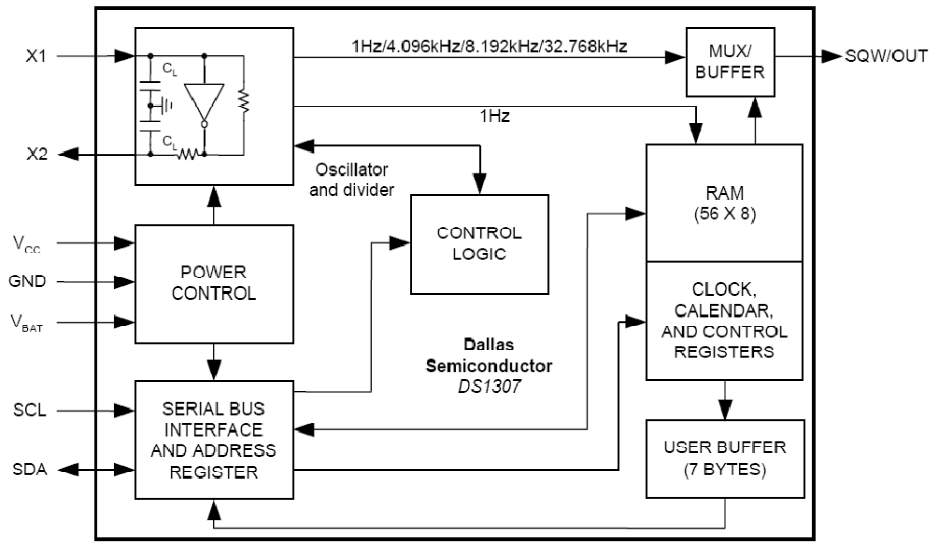
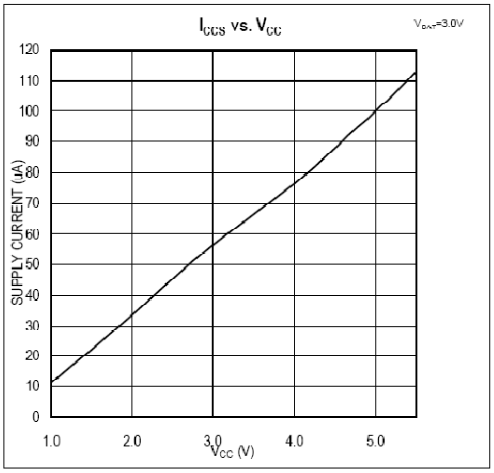


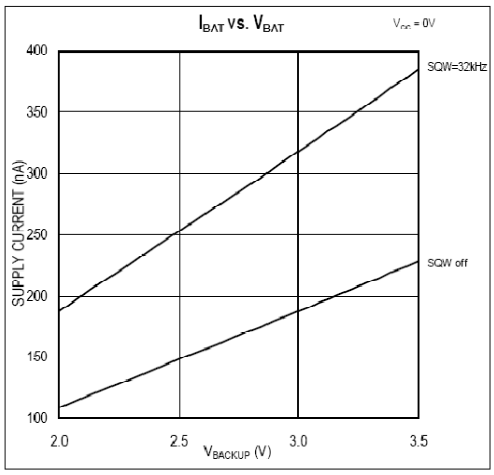
Figure 1. Block Diagram

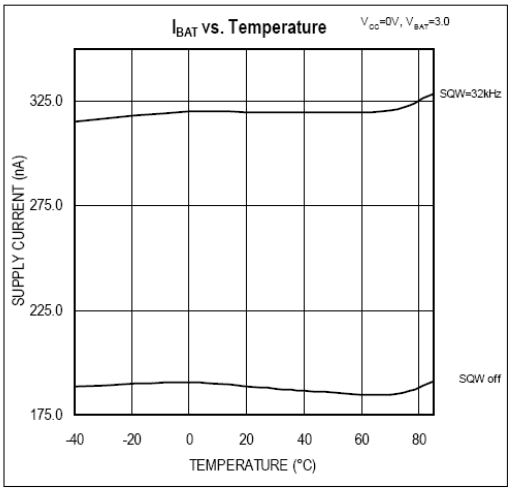


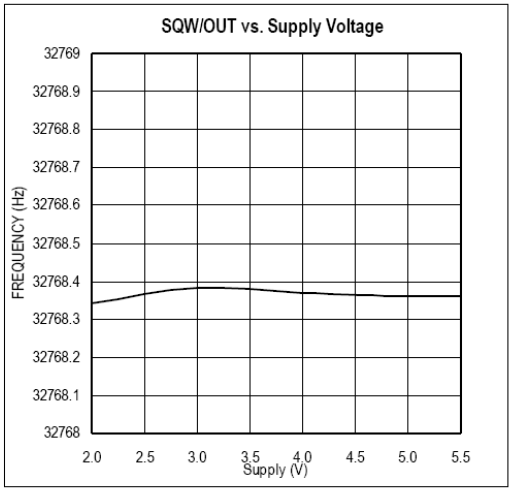
TYPICAL OPERATING CHARACTERISTICS

(VCC = 5.0V, TA = +25°C, unless otherwise noted.)









DETAILED DESCRIPTION

The VS1307 is a low-power clock/calendar with 56 bytes of battery-backed SRAM. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The VS1307 operates as a slave device on the I^2C bus. Access is obtained by implementing a START condition and providing a device identification code followed by a register address. Subsequent registers can be accessed sequentially until a STOP condition is executed. When VCC falls below 1.25 x VBAT, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out of tolerance system. When VCC falls below VBAT, the device switches into a low-current battery-backup mode. Upon power-up, the device switches from battery to VCC when VCC is greater than VBAT +0.2V and recognizes inputs when VCC is greater than 1.25 x VBAT. The block diagram in Figure 1 shows the main elements of the serial RTC.

OSCILLATOR CIRCUIT

The VS1307 uses an external 32.768 kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 1 specifies several crystal parameters for the external crystal. Figure 1. shows a functional schematic of the oscillator circuit. If using a crystal with the specified characteristics, the startup time is usually less than one second.

CLOCK ACCURACY

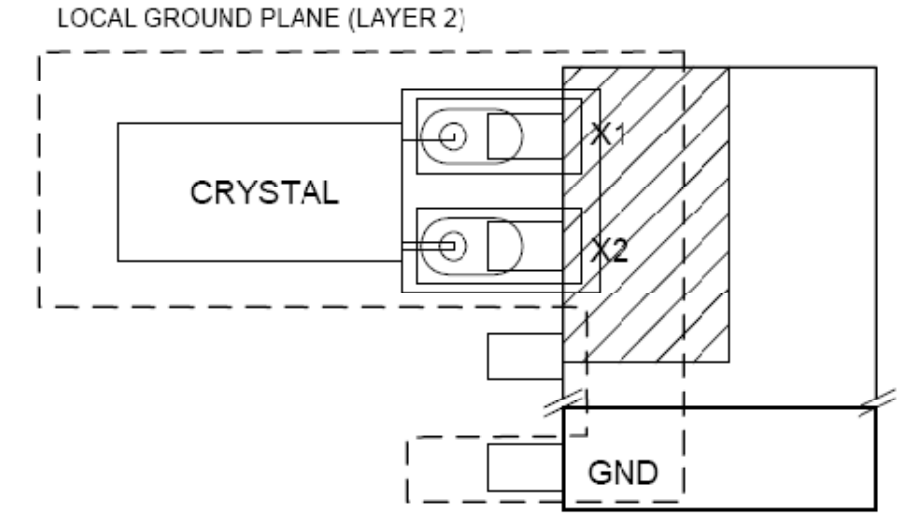
The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error will be added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit may

result in the clock running fast.

Table 1. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	fo		32.768		kHz
Series Resistance	ESR			45	KΩ
Load Capacitance	CL		12.5		pF

Figure 2. Recommended Layout for Crystal



NOTE: AVOID ROUTING SIGNAL LINES IN THE CROSSHATCHED AREA (UPPER LEFT QUADRANT) OF THE PACKAGE UNLESS THERE IS A GROUND PLANE BETWEEN THE SIGNAL LINE AND THE DEVICE PACKAGE.

RTC AND RAM ADDRESS MAP

Table 2 shows the address map for the VS1307 RTC and RAM registers. The RTC registers are located in address locations 00h to 07h. The RAM registers are located in address locations 08h to 3Fh. During a multi-byte access, when the address pointer reaches 3Fh, the end of RAM space, it wraps around to location 00h, the beginning of the clock space.

CLOCK AND CALENDAR

The time and calendar information is obtained by reading the appropriate register bytes. Table 2 shows the RTC registers. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the BCD format. The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on.) Illogical time and date entries result in undefined operation. Bit 7 of

Register 0 is the clock halt (CH) bit. When this bit is set to 1, the oscillator is disabled. When cleared to 0, the oscillator is enabled.

Note that the initial power-on state of all registers is not defined. Therefore, it is important to enable the oscillator (CH bit = 0) during initial configuration.

The VS1307 can be run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12-hour or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20 to 23 hours). The hours value must be re-entered whenever the 12/24-hour mode bit is changed.

When reading or writing the time and date registers, secondary (user) buffers are used to prevent errors when the internal registers update. When reading the time and date registers, the user buffers are synchronized to the internal registers on any I^2C START. The time information is read from these secondary registers while the clock continues to run. This eliminates the need to re-read the registers in case the internal registers update during a read. The divider chain is reset whenever the seconds register is written. Write transfers occur on the I^2C acknowledge from the VS1307. Once the divider chain is reset, to avoid rollover issues, the remaining time and date registers must be written within one second.

Table 2. Timekeeper Registers

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
00H	CH	10 Seconds			Seconds				Seconds	00-59
01H		10 Minutes			Minutes				Minutes	00-59
02H	0	12 24	10Hour PM/AM	10Hour	ours				Hours	1–12 +AM/PM 00–23
03H	0	0	0	0	0	DAY			DAY	01-07
04H	0	0	10 Date		Date				Date	01-31
05H	0	0	0	10Month	Month				Month	00-12
06H	10 Year				Year				Year	00-99
07H	OUT	0	0	SQWE	0	0	RS1	RS0	Control	—
08H-3FH									RAM 56X8	00H-FFH

CONTROL REGISTER

The VS1307 control register is used to control the operation of the SQW/OUT pin.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT0
OUT	0	0	SQWE	0	0	RS1	RS0

Bit 7: Output Control (OUT). This bit controls the output level of the SQW/OUT pin when the square wave output is disabled. If SQWE = 0, the logic level on the SQW/OUT pin is 1 if

OUT = 1 and is 0 if OUT = 0.

Bit 4: Square-Wave Enable (SQWE). This bit, when set to logic 1, enables the oscillator output. The frequency of the square-wave output depends upon the value of the RS0 and RS1 bits. With the square-wave output set to 1Hz, the clock registers update on the falling edge of the square-wave.

Bits 1, 0: Rate Select (RS1, RS0). These bits control the frequency of the square-wave output when the square-wave output has been enabled. The following table lists the square-wave frequencies that can be selected with the RS bits.

RS1	RS0	SQW/OUT OUTPUT	SQWE	OUT
0	0	1Hz	1	X
0	1	4.096kHz	1	X
1	0	8.192kHz	1	X
1	1	32.768kHz	1	X
X	X	0	0	0
X	X	1	0	1

I²C DATA BUS

The VS1307 supports the I²C protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the message is called a master. The devices that are controlled by the master are referred to as slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The VS1307 operates as a slave on the I²C bus.

Figures 3, 4, and 5 detail how data is transferred on the I²C bus.

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a START condition,

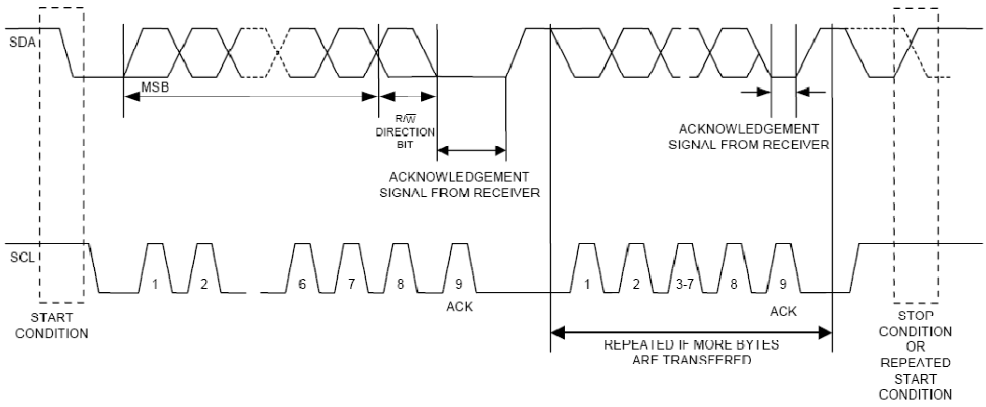
the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited, and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit. Within the I^2C bus specifications a standard mode (100 kHz clock rate) and a fast mode (400 kHz clock rate) are defined. The VS1307 operates in the standard mode (100 kHz) only.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 3. Data Transfer on I^2C Serial Bus



Depending upon the state of the R/W bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.
2. **Data transfer from a slave transmitter to a master receiver.** The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. This is followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last

received byte, a "not acknowledge" is returned. The master device generates all the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released. Data is transferred with the most significant bit (MSB) first.

The VS1307 may operate in the following two modes:

1. **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Hardware performs address recognition after reception of the slave address and direction bit (see Figure 4). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-bit VS1307 address, which is 1101000, followed by the direction bit (R/W), which for a write is 0. After receiving and decoding the slave address byte, the VS1307 outputs an acknowledge on SDA. After the VS1307 acknowledges the slave address + write bit, the master transmits a word address to the VS1307. This sets the register pointer on the VS1307, with the VS1307 acknowledging the transfer. The master can then transmit zero or more bytes of data with the VS1307 acknowledging each byte received. The register pointer automatically increments after each data byte are written. The master will generate a STOP condition to terminate the data write.

2. **Slave Transmitter Mode (Read Mode):** The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. The VS1307 transmits serial data on SDA while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer (see Figure 5). The slave address byte is the first byte received after the START condition is generated by the master. The slave address byte contains the 7-bit VS1307 address, which is 1101000, followed by the direction bit (R/W), which is 1 for a read. After receiving and decoding the slave address the VS1307 outputs an acknowledge on SDA. The VS1307 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The register pointer automatically increments after each byte are read. The VS1307 must receive a Not Acknowledge to end a read.

Figure 4. Data Write—Slave Receiver Mode

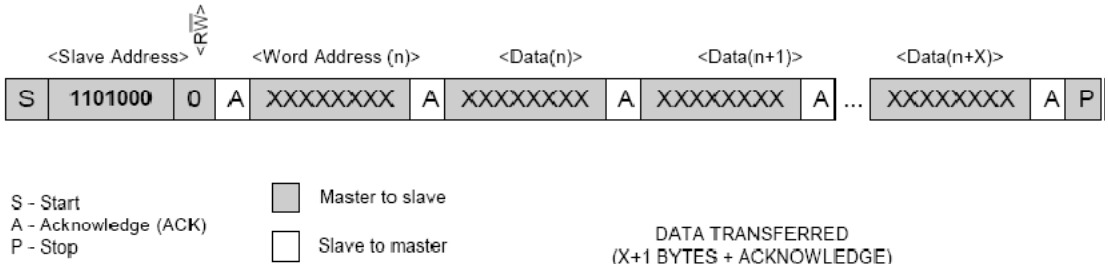


Figure 5. Data Read—Slave Transmitter Mode

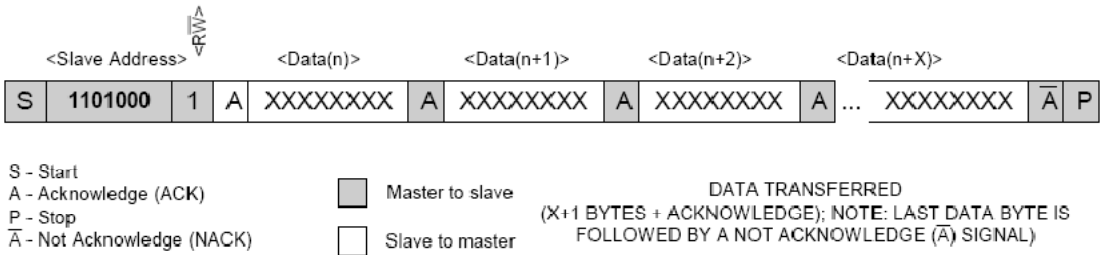
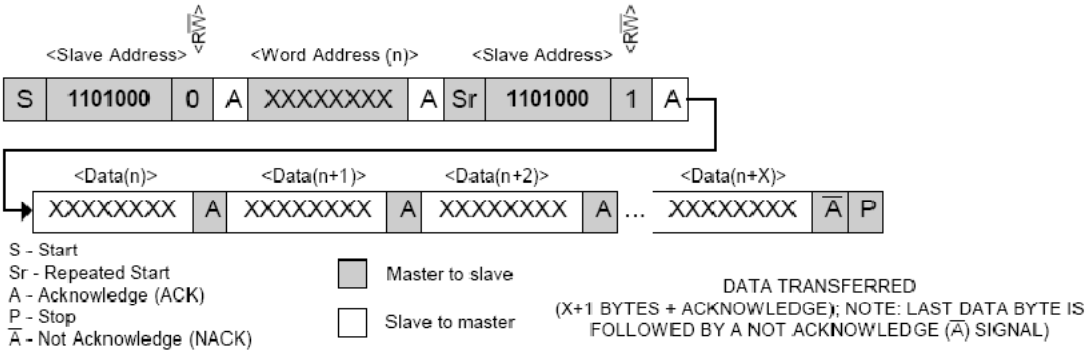
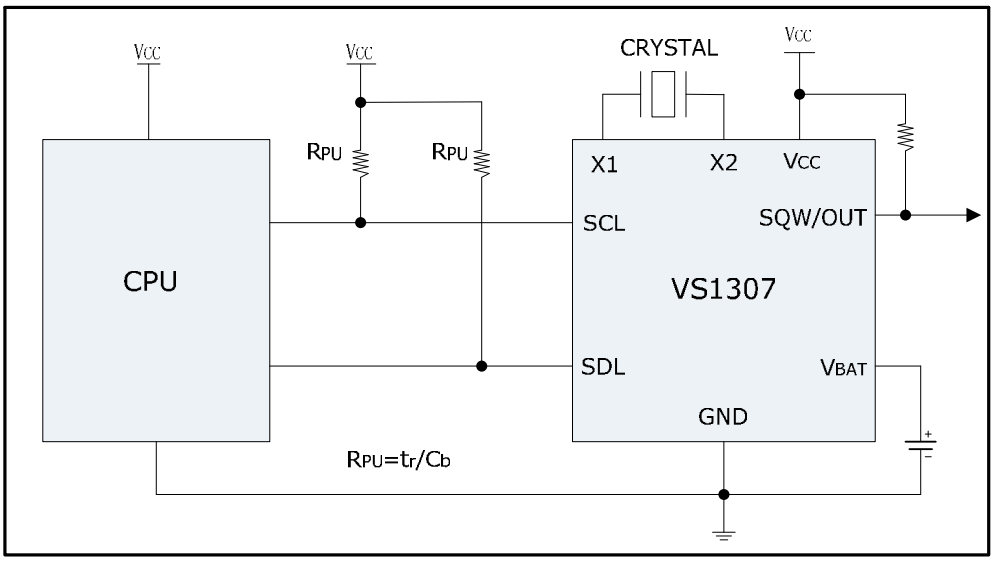


Figure 6. Data Read (Write Pointer, Then Read)—Slave Receive and Transmit



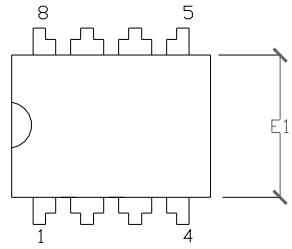
TYPICAL OPERATING CIRCUIT

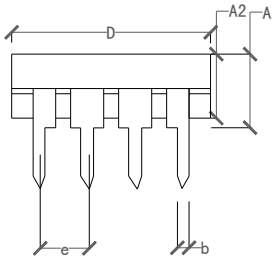


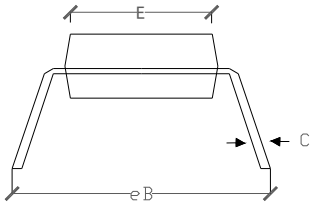
PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.vslun.com/)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NEW DRAWING	12/01	





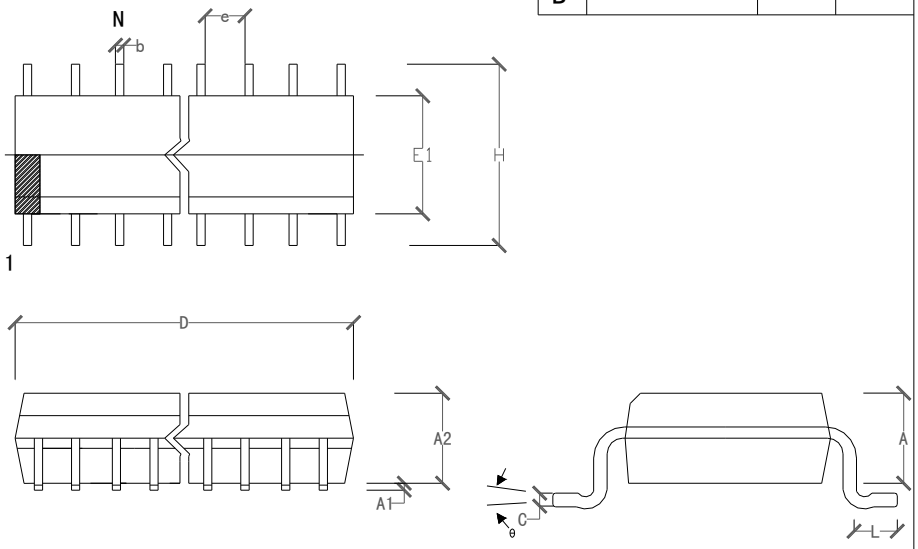


	8 PIN	
	MIN	MAX
A	——	0.170
A1	0.015	——
A2	0.115	0.195
b	0.015	0.022
c	0.008	0.012
D	0.360	0.380
E	0.300	0.325
E1	0.240	0.260
e	0.090	0.110
L	0.125	0.135
eB	——	0..430

ALL DIMENSIONS ARE IN INCHES

SIGNATURE	DATE	深圳弗赛尔电子设计有限公司 VOSSEL Electronic Design Co.,Ltd.			
DOC. CONTROL:					
ENGR. MGR:		TITLE MARKETING OUTLINE, 8 LEAD PLASTIC DUAL-IN-LINE PACKAGE (0.300")			
MFG. ENGR:					
CHECKED BY: TWM	12/01	SIZE A	FSCM NO	PART NO. 56-G5005-000	REV A
DRAWN BY: JFD	12/01				
DO NOT SCALE DWG		SCALE N/A		SHEET 1 OF 1	

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NEW DRAWING	2/95	J.W.
B	UPDATE DIMENSIONS		



PKG	8 PIN		14 PIN		16 PIN	
LTR	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.053	0.069	0.053	0.069	0.053	0.069
A MM	1.35	1.75	1.35	1.75	1.35	1.75
A1 IN.	0.004	0.010	0.004	0.010	0.004	0.010
A1 MM	0.10	0.25	0.10	0.25	0.10	0.25
A2 IN.	0.048	0.062	0.048	0.062	0.048	0.062
A2 MM	1.22	1.57	1.22	1.57	1.22	1.57
b IN.	0.012	0.020	0.012	0.020	0.012	0.020
b MM	0.030	0.51	0.30	0.51	0.30	0.51
c IN.	0.007	0.011	0.007	0.011	0.007	0.011
c MM	0.18	0.28	0.18	0.28	0.18	0.28
D IN.	0.188	0.196	0.337	0.344	0.386	0.393
D MM	4.78	4.98	8.56	8.74	9.80	9.98
e IN.	.050 BSC		.050 BSC		.050 BSC	
e MM	1.27 BSC		1.27 BSC		1.27 BSC	
E1 IN.	0.150	0.158	0.150	0.158	0.150	0.158
E1 MM	3.81	4.01	3.81	4.01	3.81	4.01
H IN.	0.230	0.244	0.230	0.244	0.230	0.244
H MM	5.84	6.20	5.84	6.20	5.84	6.20
L IN.	0.016	0.050	0.016	0.050	0.016	0.050
L MM	0.41	1.27	0.41	1.27	0.41	1.27
θ	0*	8*	0*	8*	0*	8*

THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A TERMINAL 1 IDENTIFIER MUST BE POSITIONED SO THAT 1/2 OR MORE OF IT'S AREA IS CONTAINED IN THE HATCHED ZONE.

ALL DIMENSIONS ARE IN INCHES

SIGNATURE	DATE
DOC. CONTROL:	
ENGR. MGR:	
MFG. ENGR:	
CHECKED BY:	
DRAWN BY: m.w.c	2/95
DO NOT SCALE DWG	

深圳弗赛尔电子设计有限公司
VOSSEL Electronic Design Co.,Ltd.

TITLE: PACKAGE OUTLINE .150" SOIC 8,14&16 LD.

SIZE	FSCM NO	PART NO.	REV
A		56-G2008-001	B

SCALE N/A SHEET 1 OF 1

ORDERING INFORMATION

PART	TEMP RANGE	VOLTAGE	PIN-PACKAGE	TOP MARK
VS1307	0°C to +70°C	5.0	8 PDIP (300 mils)	VS1307
VS1307+	0°C to +70°C	5.0	8 PDIP (300 mils)	VS1307
VS1307N	-40°C to +85°C	5.0	8 PDIP (300 mils)	VS1307N
VS1307N+	-40°C to +85°C	5.0	8 PDIP (300 mils)	VS1307N
VS1307Z	0°C to +70°C	5.0	8 SOIC (150 mils)	VS1307
VS1307Z+	0°C to +70°C	5.0	8 SOIC (150 mils)	VS1307
VS1307ZN	-40°C to +85°C	5.0	8 SOIC (150 mils)	VS1307N
VS1307ZN+	-40°C to +85°C	5.0	8 SOIC (150 mils)	VS1307N
VS1307Z/T&R	0°C to +70°C	5.0	8 SOIC (150 mils) Tape and Reel	VS1307
VS1307Z+T&R	0°C to +70°C	5.0	8 SOIC (150 mils) Tape and Reel	VS1307
VS1307ZN/T&R	-40°C to +85°C	5.0	8 SOIC (150 mils) Tape and Reel	VS1307N
VS1307ZN+T&R	-40°C to +85°C	5.0	8 SOIC (150 mils) Tape and Reel	VS1307N

+ Denotes a lead-free/RoHS-compliant device.

** A "+" anywhere on the top mark indicates a lead-free device.*

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