



## QUAD CHANNEL HIGH SIDE SOLID STATE RELAY

PRELIMINARY DATA

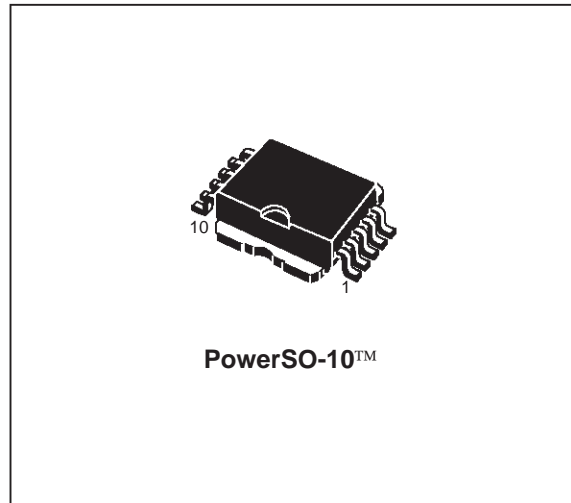
TYPE	R <sub>DS(on)</sub>	I <sub>OUT</sub>	V <sub>CC</sub>
VNQ660SP	50mΩ (*)	6A	36 V

(\*) Per each channel

- OUTPUT CURRENT PER CHANNEL: 6A
- CMOS COMPATIBLE INPUTS
- OPEN LOAD DETECTION (OFF STATE)
- UNDERVOLTAGE & OVERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT-DOWN
- CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- PROTECTION AGAINST:
  - LOSS OF GROUND & LOSS OF V<sub>CC</sub>
- REVERSE BATTERY PROTECTION (\*\*)

### DESCRIPTION

The VNQ660SP is a monolithic device made by using STMicroelectronics VIPower M0-3 Technology, intended for driving resistive or inductive loads with one side connected to ground.



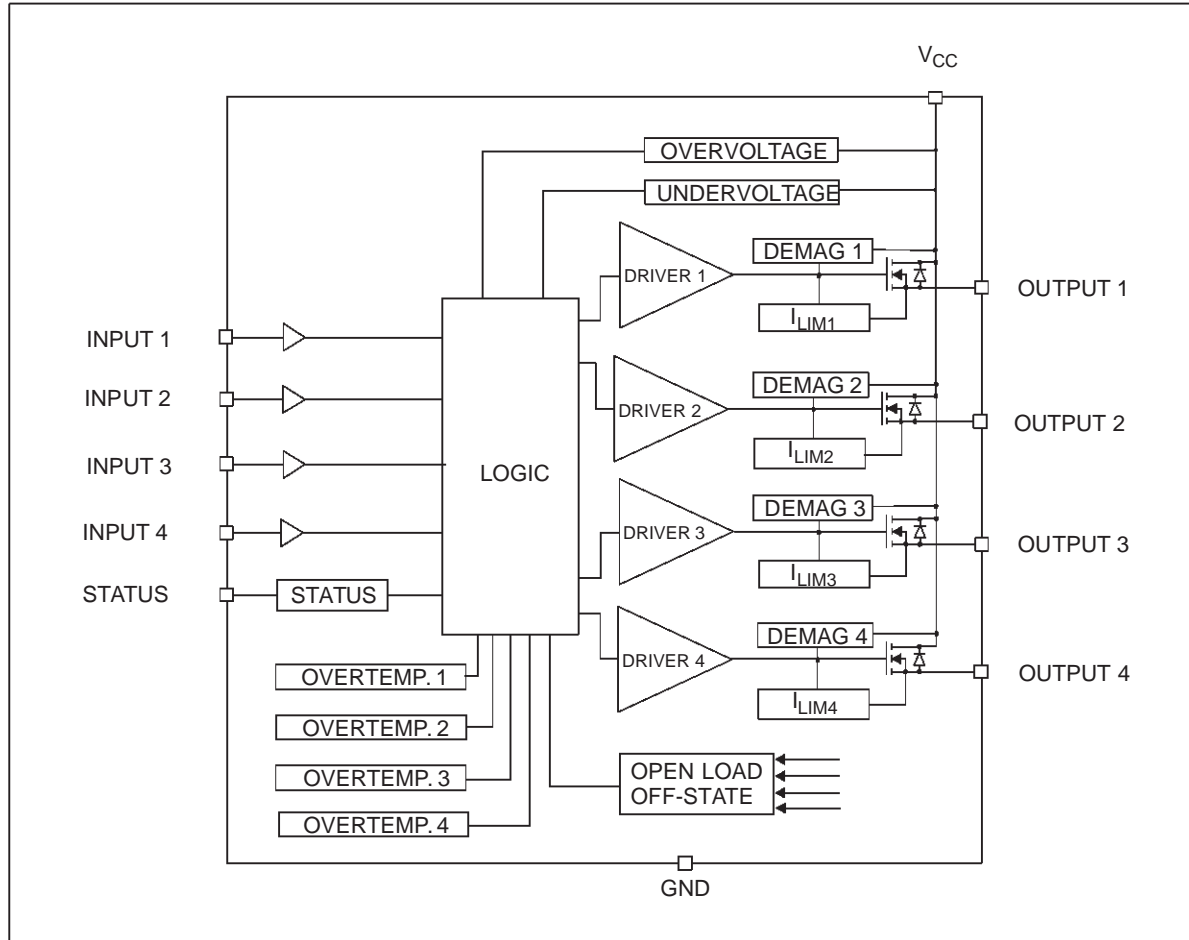
This device has four independent channels. Built-in thermal shut down and output current limitation protect the chip from over temperature and short circuit.

### ABSOLUTE MAXIMUM RATING

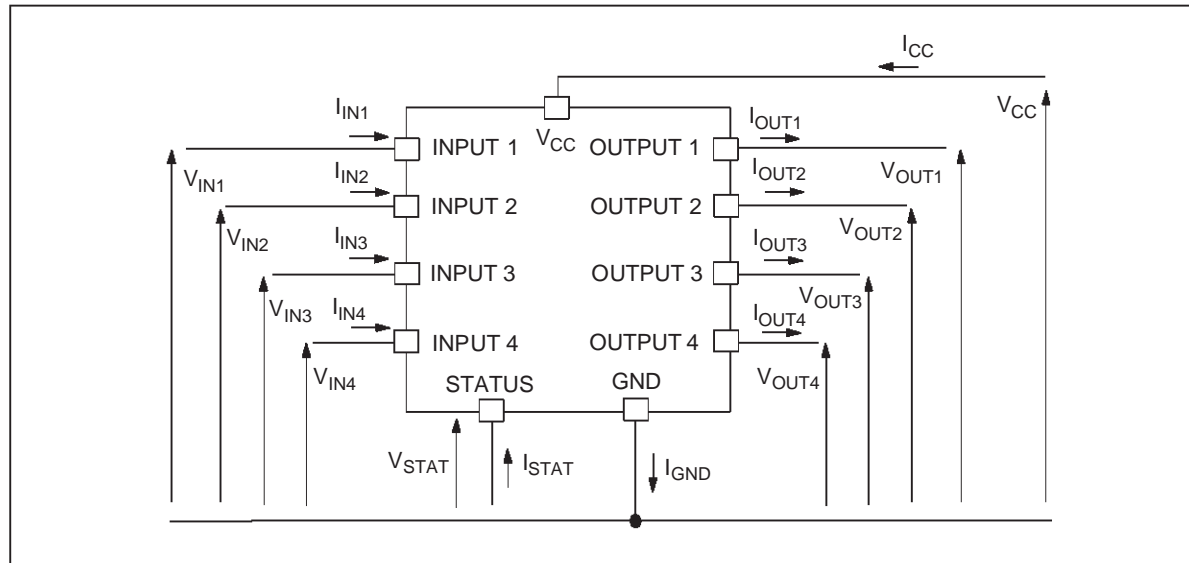
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage (continuous)	41	V
-V <sub>CC</sub>	Reverse supply voltage (continuous)	-0.3	V
I <sub>OUT</sub>	Output current (continuous), per each channel	Internally limited	A
I <sub>R</sub>	Reverse output current (continuous), per each channel	-15	A
I <sub>IN</sub>	Input current	+/- 10	mA
I <sub>STAT</sub>	Status current	+/- 10	mA
I <sub>GND</sub>	Ground current at T <sub>C</sub> ≤ 25°C (continuous)	-200	mA
V <sub>ESD</sub>	Electrostatic discharge (R=1.5kΩ; C=100pF)	2000	V
P <sub>tot</sub>	Power dissipation at T <sub>C</sub> =25°C	89	W
T <sub>j</sub>	Junction operating temperature	-40 to 150	°C
T <sub>stg</sub>	Storage temperature	-65 to 150	°C
E <sub>C</sub>	Non repetitive clamping energy at T <sub>C</sub> =25 deg.	150	mJ

(\*\*) See application schematic at page 8

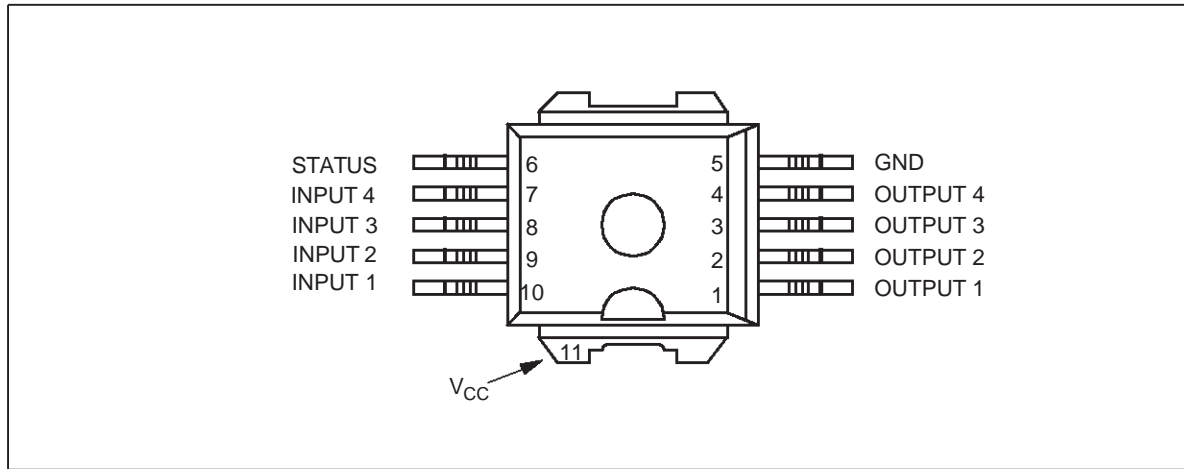
**BLOCK DIAGRAM**



**CURRENT AND VOLTAGE CONVENTIONS**



**CONNECTION DIAGRAM (TOP VIEW)**



**THERMAL DATA**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (MAX) per channel	2.0	°C/W
$R_{thj-case}$	Thermal resistance junction-case (MAX) (all channels on)	1.4	°C/W
$R_{tj-amb}$	Thermal resistance junction-ambient (MAX)	52 (*)	°C/W

(\*) When mounted on a standard single-sided FR-4 board with 50 mm of Cu (at least 35 μm thick).

**ELECTRICAL CHARACTERISTICS** ( $V_{CC}=6V$  up to 24V;  $-40^{\circ}C < T_j < 150^{\circ}C$  unless otherwise specified)

POWER (per each channel)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{CC}^{(**)}$	Operating supply voltage		5.5	13	36	V
$V_{USD}^{(**)}$	Undervoltage shutdown		3.5	4.6	5.5	V
$V_{UVhyst}^{(**)}$	Undervoltage hysteresis		0.2		1	V
$V_{OV}^{(**)}$	Overvoltage shutdown		36	42	48	V
$V_{OVhyst}^{(**)}$	Overvoltage hysteresis		0.25			V
$I_S^{(**)}$	Supply current	Off state; Input=0V; $V_{CC}=13.5V$		12	40	μA
		Off state; Input=0V; $V_{CC}=13.5V$		12	25	μA
		On state Input=3.25V; $9V < V_{CC} < 18V$		6	12	mA
$R_{DS(on)}$	On state resistance	$I_{OUT}=1A$ ; $T_j=25^{\circ}C$ ; $9V < V_{CC} < 18V$		40	50	mΩ
		$I_{OUT}=1A$ ; $T_j=150^{\circ}C$ ; $9V < V_{CC} < 18V$		85	100	mΩ
		$I_{OUT}=1A$ ; $V_{CC}=5.5V$			130	mΩ
$I_{L(off1)}$	Off state output current	Off state; Input=0V; $V_{OUT}=0V$			100	μA
$I_{L(off2)}$	Off state output current	Off state, Input=0V, $V_{OUT}=3.5V$	-75	-30	0	μA

**SWITCHING** ( $V_{CC}=13V$ )

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$R1=13\Omega$ channels 1,2,3,4		40	70	μs
$t_{d(off)}$	Turn-off delay time	$R1=13\Omega$ channels 1,2,3,4		40	140	μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R1=13\Omega$ channels 1,2,3,4	0.1	0.2	0.6	V/μs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R1=13\Omega$ channels 1,2,3,4	0.05	0.2	0.6	V/μs
$t_r$	Rise time of output voltage	$R1=13\Omega$ channels 1,2,3,4		110		μs

(\*\*) Per device.



**PROTECTIONS (per each channel)**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$T_{TSD}$	Shutdown temperature		150	170	200	°C
$T_R$	Reset temperature		135			°C
$T_{hyst}$	Thermal hysteresis		7	15	25	°C
$I_{LIM}$	DC Short circuit current	$9V < V_{CC} < 36V$ $5.5V < V_{CC} < 36V$	6	10	18 18	A A
$V_{demag}$	Turn-off output voltage clamp	$I_{OUT}=2A$ ; $V_{IN}=0V$ ; $L=6mH$	$V_{CC}-41$	$V_{CC}-48$	$V_{CC}-55$	V
$V_{STAT}$	Status low output voltage	$I_{STAT}=1.6mA$			0.5	V
$I_{LSTAT}$	Status leakage current	Normal operation; $V_{STAT}=5V$			10	μA
$C_{STAT}$	Status pin input capacitance	Normal operation; $V_{STAT}=5V$			25	pF
$V_{SCL}$	Status clamp voltage	$I_{STAT}=1mA$ $I_{STAT}=-1mA$	6	6.8 -0.7	8	V V

**LOGIC INPUT (per each channel)**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{IL}$	Input Low Level Voltage				1.25	V
$V_{IH}$	Input High Level Voltage		3.25			V
$V_{HYST}$	Input Hysteresis Voltage		0.5			V
$I_{IH}$	Input high level voltage	$V_{IN}=3.25V$			10	μA
$I_{IL}$	Input Current	$V_{IN}=1.25V$	1			μA
$C_{IN}$	Input Capacitance				40	pF
$V_{ICL}$	Input Clamp Voltage	$I_{IN}=1mA$ $I_{IN}=-1mA$	6	6.8 -0.7	8	V V

**OPENLOAD DETECTION (off state) per each channel**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{SDL}$	Status Delay	(*)			20	μs
$V_{OL}$	Openload Voltage Detection Threshold	$V_{IN}=0V$	1.5	2.5	3.5	V
$T_{DOL}$	Openload Detection Delay at Turn Off	$V_{CC}=18V$ (*)			300	μs

(\*) See Figure 1

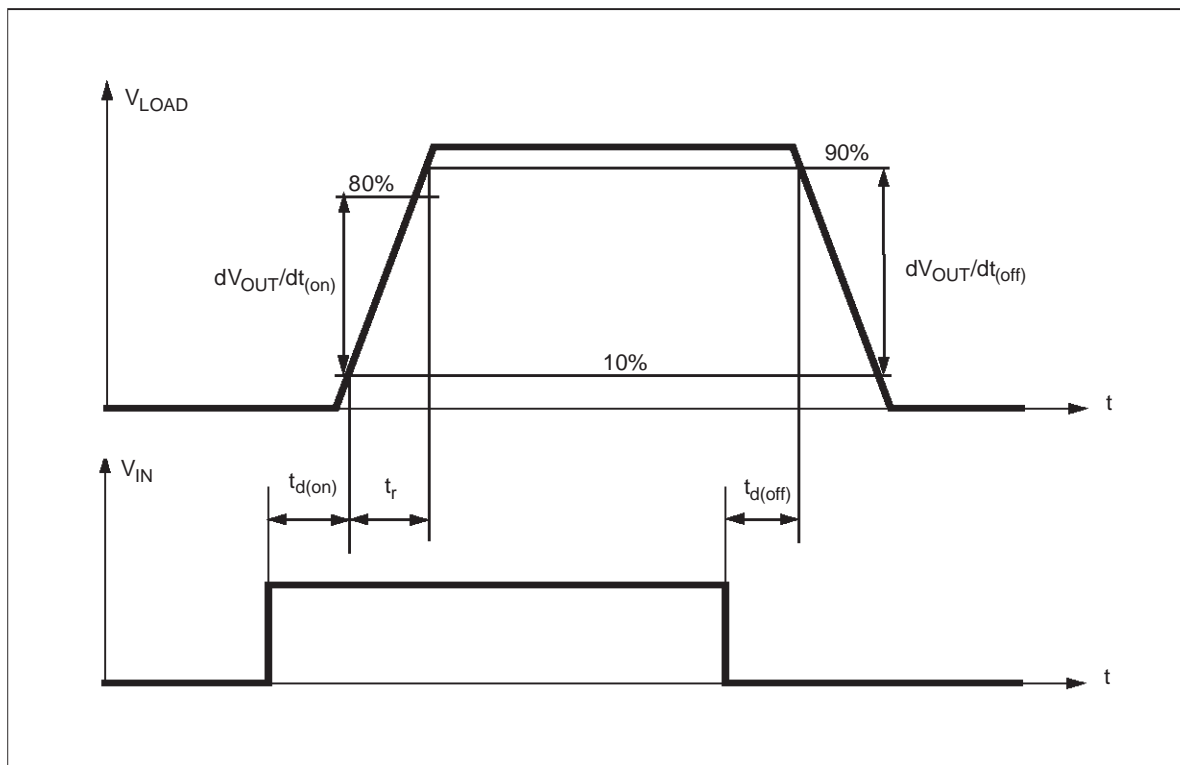
**ELECTRICAL TRANSIENT REQUIREMENTS**

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 μs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 μs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω

ISO T/R 7637/1 Test Pulse	Test Levels Result			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

**SWITCHING CHARACTERISTICS**



TRUTH TABLE (per each channel)

CONDITIONS	INPUT	OUTPUT	STATUS
Normal Operation	L	L	H
	H	H	H
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H
Current Limitation	L	L	H
	H	X	H
Output Voltage > $V_{OL}$	L	H	L
	H	H	H

Figure 1: Status timing waveforms

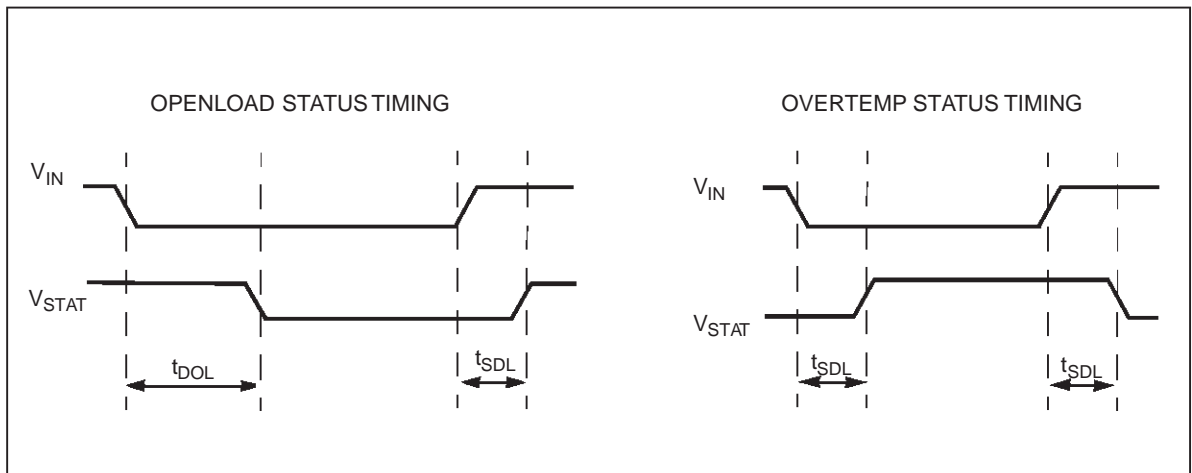
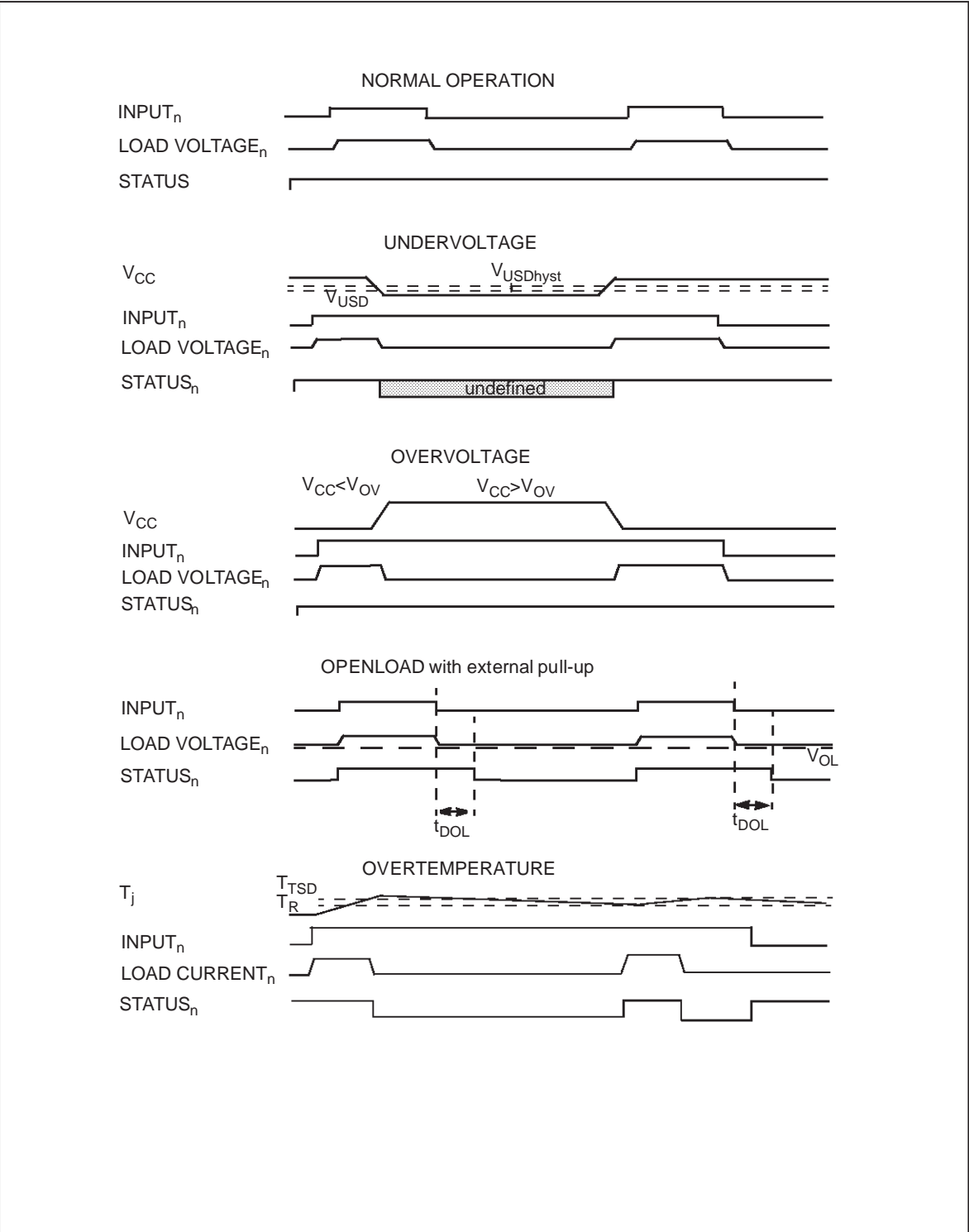
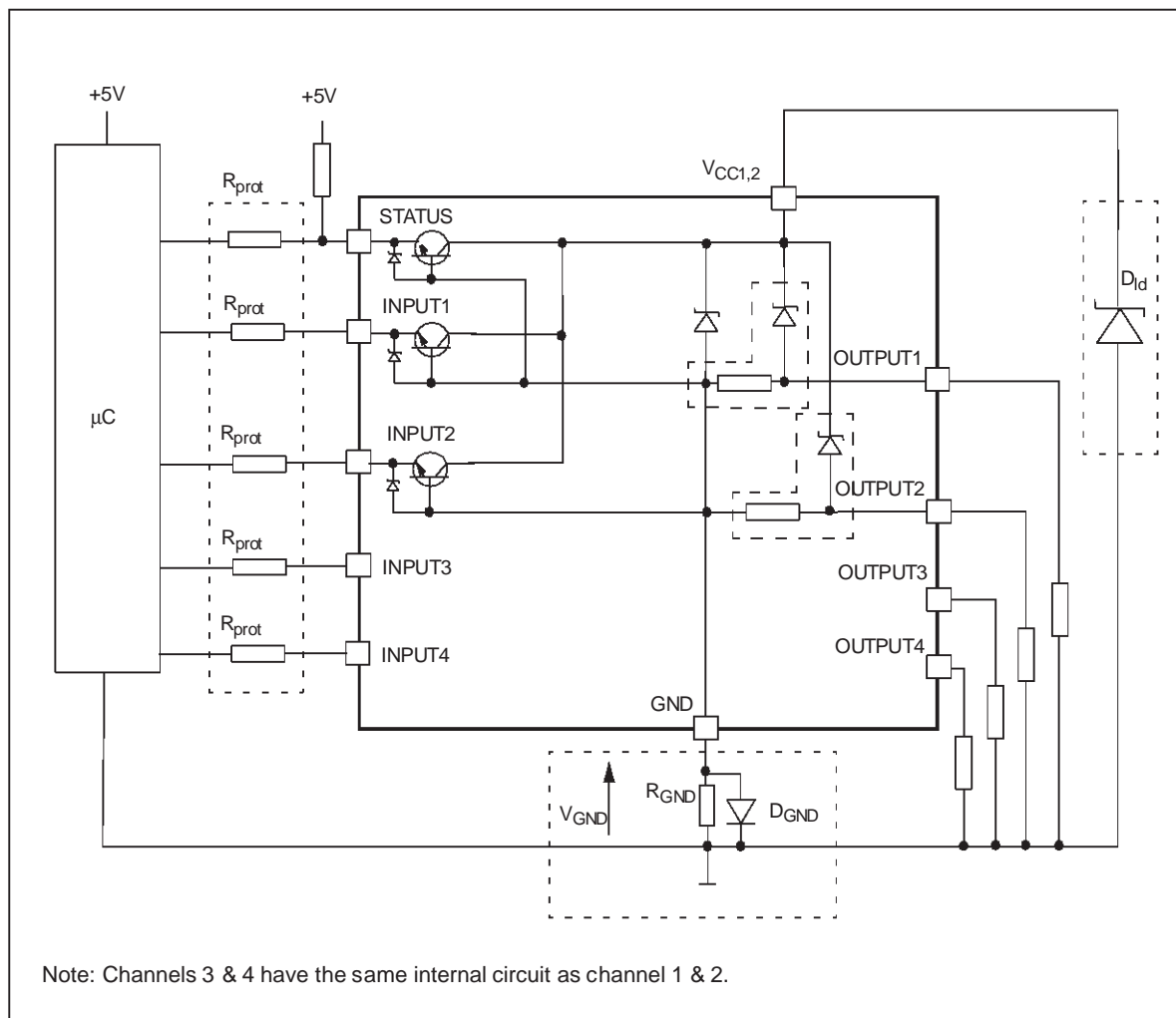


Figure1: Waveforms



APPLICATION SCHEMATIC



**GND PROTECTION NETWORK AGAINST REVERSE BATTERY**

Solution 1: Resistor in the ground line ( $R_{GND}$  only). This can be used with any type of load.

The following is an indication on how to dimension the  $R_{GND}$  resistor.

- 1)  $R_{GND} \leq 600mV / (I_{S(on)max})$ .
- 2)  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in  $R_{GND}$  (when  $V_{CC} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the

sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the  $R_{GND}$  will produce a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same  $R_{GND}$ .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode ( $D_{GND}$ ) in the ground line.

A resistor ( $R_{GND} = 1k\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j 600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device



ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

### LOAD DUMP PROTECTION

$D_{ld}$  is necessary (Transil or MOV) if the load dump peak voltage exceeds  $V_{CC}$  max DC rating. The same applies if the device will be subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO T/R 7637/1 table.

### $\mu C$ I/Os PROTECTION:

If a ground protection network is used and negative transient are present on the  $V_{CC}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu C$  I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of  $\mu C$  and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of  $\mu C$  I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

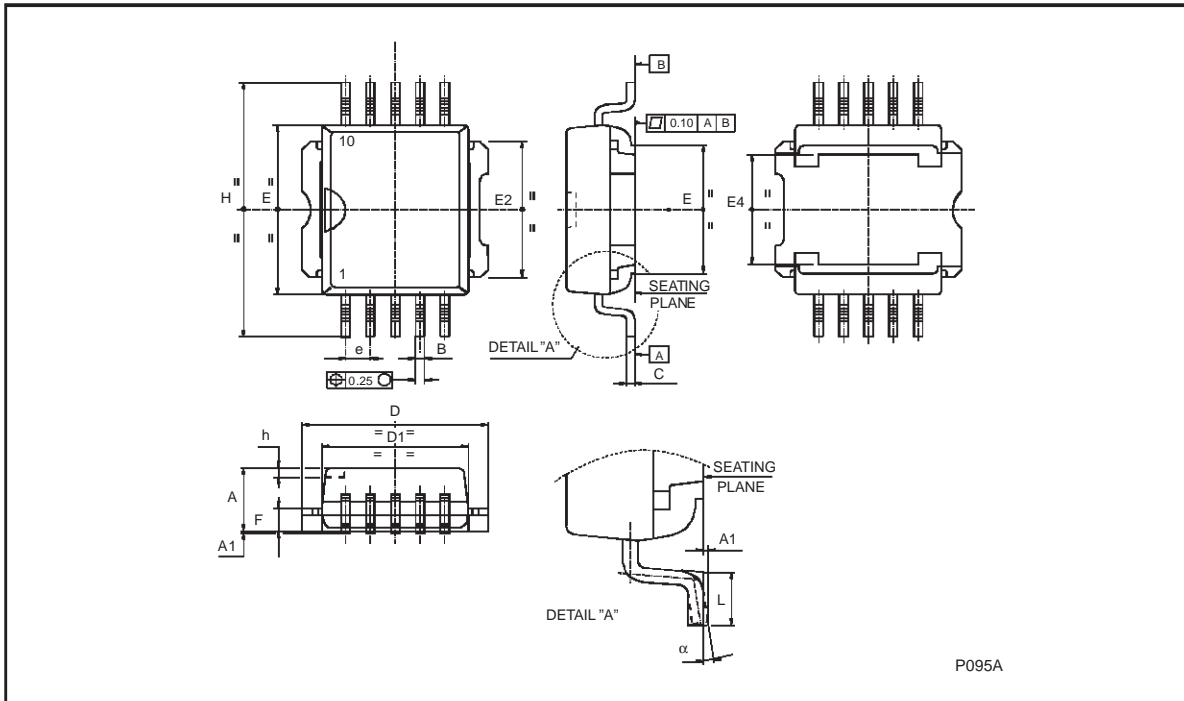
For  $V_{CCpeak} = -100V$  and  $I_{latchup} \geq 20mA$ ;  $V_{OH\mu C} \geq 4.5V$   
 $5k\Omega \leq R_{prot} \leq 65k\Omega$ .

Recommended  $R_{prot}$  value is  $10k\Omega$ .

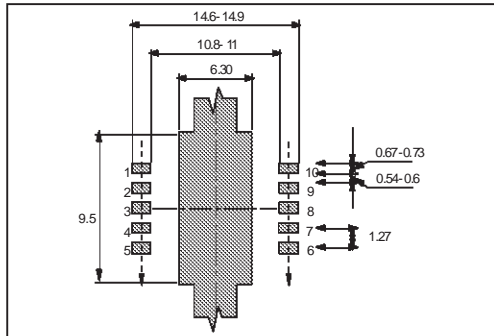
**PowerSO-10™ MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A (*)	3.4		3.6	0.134		0.142
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
B (*)	0.37		0.53	0.014		0.021
C	0.35		0.55	0.013		0.022
C (*)	0.23		0.32	0.009		0.0126
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E2	7.20		7.60	0.283		300
E2 (*)	7.30		7.50	0.287		0.295
E4	5.90		6.10	0.232		0.240
E4 (*)	5.90		6.30	0.232		0.248
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
F (*)	1.20		1.40	0.047		0.055
H	13.80		14.40	0.543		0.567
H (*)	13.85		14.35	0.545		0.565
h		0.50			0.002	
L	1.20		1.80	0.047		0.070
L (*)	0.80		1.10	0.031		0.043
α	0°		8°	0°		8°
α (*)	2°		8°	2°		8°

(\*) Muar only POA P013P



**PowerSO-10™ SUGGESTED PAD LAYOUT**



**TUBE SHIPMENT (no suffix)**

All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

**TAPE AND REEL SHIPMENT (suffix "13TR")**

40mm min. Access hole at slit inclination

Full radius

Tape slit in. for tape star: 2.5mm min width

C measured at sub

**REEL DIMENSIONS**

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / - 0)	24.4
N (min)	60
T (max)	30.4

All dimensions are in mm.

**TAPE DIMENSIONS**  
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	24
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	11.5
Compartment Depth	K (max)	6.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.

TOP COVER TAPE

User Direction of Feed

End

Start

No components

Components

No components

500mm min

Empty components pockets sealed with cover tape.

User direction of feed

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