VN920SP-E

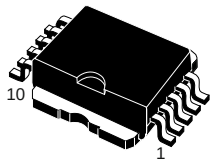
HIGH SIDE DRIVER

Table 1. General Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN920SP-E	15mΩ	30 A	36 V

- CMOS COMPATIBLE INPUT
- PROPORTIONAL LOAD CURRENT SENSE
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUTDOWN
- CURRENT LIMITATION
- PROTECTION AGAINST LOSS OF GROUND AND LOSS V_{CC}
- VERY LOW STAND-BY POWER DISSIPATION
- REVERSE BATTERY PROTECTION (*)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

Figure 1. Package



PowerSO-10™

DESCRIPTION

The VN920SP-E is a monolithic device designed in STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. The device integrates an analog current sense output which delivers a current proportional to the load current. Device automatically turns off in case of ground pin disconnection.

Table 2. Order Codes

Package	Tube	Tape and Reel
PowerSO-10™	VN920SP-E	VN920SPTR-E

Note: (*) See application schematic at page 9.

Figure 2. Block Diagram

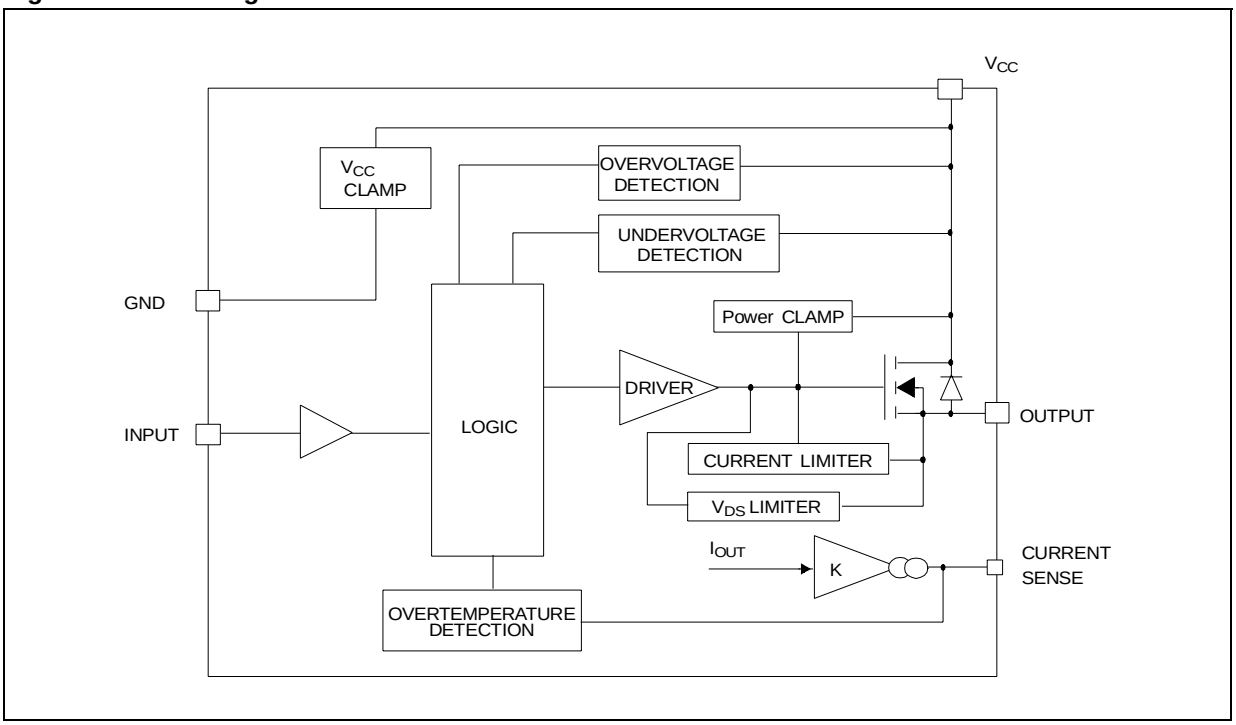
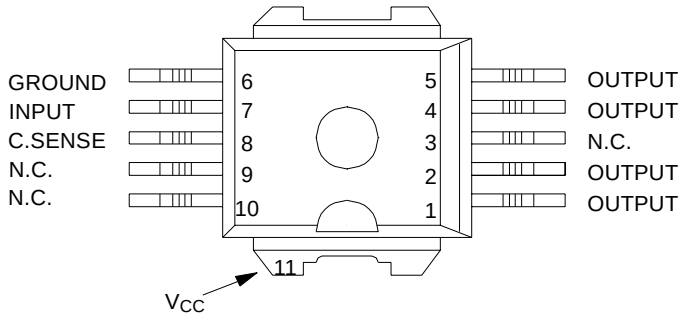


Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	41	V
- V_{CC}	Reverse DC Supply Voltage	- 0.3	V
- I_{GND}	DC Reverse Ground Pin Current	- 200	mA
I_{OUT}	DC Output Current	Internally Limited	A
- I_{OUT}	Reverse DC Output Current	- 40	A
I_{IN}	DC Input Current	+/- 10	mA
V_{CSENSE}	Current Sense Maximum Voltage	-3 +15	V V
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF) - INPUT - CURRENT SENSE - OUTPUT - V_{CC}	 4000 2000 5000 5000	 V V V V
E_{MAX}	Maximum Switching Energy (L=0.25mH; R_L=0Ω; V_{bat}=13.5V; T_{jstart}=150ºC; I_L=45A)	362	mJ
P_{tot}	Power Dissipation T_C≤25°C	96.1	W
T_j	Junction Operating Temperature	Internally limited	°C
T_c	Case Operating Temperature	- 40 to 150	°C
T_{STG}	Storage Temperature	- 55 to 150	°C

Figure 3. Configuration Diagram (Top View) & Suggested Connections for Unused and N.C. Pins



Connection / Pin	Current Sense	N.C.	Output	Input
Floating		X	X	X
To Ground	Through 1KΩ resistor	X		Through 10KΩ resistor

Figure 4. Current and Voltage Conventions

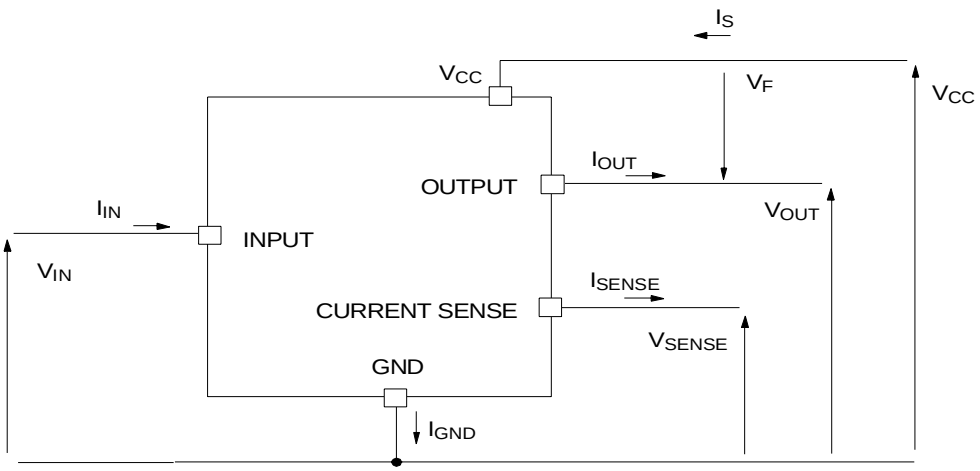


Table 4. Thermal Data

Symbol	Parameter		Value		Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	1.3		°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	51.3 (1)	37 (2)	°C/W

(1) When mounted on a standard single-sided FR-4 board with 0.5cm^2 of Cu (at least 35µm thick).
(2) When mounted on a standard single-sided FR-4 board with 6 cm^2 of Cu (at least 35µm thick).

ELECTRICAL CHARACTERISTICS (8V<V_{CC}<36V; -40°C<T_j<150°C unless otherwise specified)

Table 5. Power

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Operating Supply Voltage		5.5	13	36	V
V_{USD}	Undervoltage Shut-down		3	4	5.5	V
V_{OV}	Overvoltage Shut-down		36			V
R_{ON}	On State Resistance	I_{OUT}=10A; T_j =25°C I_{OUT}=10A I_{OUT}=3A; V_{CC}=6V			15 30 50	mΩ mΩ mΩ
V_{clamp}	Clamp Voltage	I_{CC}=20mA (See note 1)	41	48	55	V
I_S	Supply Current	Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V Off State; V_{CC}=13V; T_j=25°C; V_{IN}=V_{OUT}=0V On State; V_{CC}=13V; V_{IN}=5V; I_{OUT}=0; R_{SENSE}=3.9KΩ		10 10	25 20 5	µA µA mA
$I_{L(off1)}$	Off State Output Current	V_{IN}=V_{OUT}=0V	0		50	µA
$I_{L(off2)}$	Off State Output Current	V_{IN}=0V; V_{OUT}=3.5V	-75		0	µA
$I_{L(off3)}$	Off State Output Current	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j =125°C			5	µA
$I_{L(off4)}$	Off State Output Current	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j =25°C			3	µA

Note: 1. V_{clamp} and V_{OV} are correlated. Typical difference is 5V.

Table 6. Switching (V_{CC} =13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on Delay Time	R_L=1.3Ω (see figure 2)		50		µs
$t_{d(off)}$	Turn-off Delay Time	R_L=1.3Ω (see figure 2)		50		µs
$dV_{OUT}/dt_{(on)}$	Turn-on Voltage Slope	R_L=1.3Ω (see figure 2)		See relative diagram		V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off Voltage Slope	R_L=1.3Ω (see figure 2)		See relative diagram		V/µs

Table 7. Logic Input

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Level				1.25	V
I_{IL}	Low Level Input Current	V_{IN}=1.25V	1			µA
V_{IH}	Input High Level		3.25			V
I_{IH}	High Level Input Current	V_{IN}=3.25V			10	µA
$V_{I(hyst)}$	Input Hysteresis Voltage		0.5			V
V_{ICL}	Input Clamp Voltage	I_{IN}=1mA I_{IN}=-1mA	6	6.8 -0.7	8	V V

ELECTRICAL CHARACTERISTICS (continued)

Table 8. V_{CC} - Output Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_F	Forward on Voltage	$-I_{OUT}$=5.3A; T_j=150°C			0.6	V

Table 9. Protections (see note 2)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{TSD}	Shut-down Temperature		150	175	200	°C
T_R	Reset Temperature		135			°C
T_{hyst}	Thermal Hysteresis		7	15		°C
I_{lim}	DC Short Circuit Current	V_{CC}=13V 5V<V_{CC}<36V	30	45	75 75	A A
V_{demag}	Turn-off Output Clamp Voltage	I_{OUT}=2A; V_{IN}=0V; L=6mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V
V_{ON}	Output Voltage Drop Limitation	I_{OUT}=1A; T_j=-40°C....+150°C		50		mV

Note: 2. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Current Sense (9V≤V_{CC}≤16V) (See Fig. 5)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT}=1A; V_{SENSE}=0.5V; T_j= -40°C...150°C	3300	4400	6000	
dK_1/K_1	Current Sense Ratio Drift	I_{OUT}=1A; V_{SENSE}=0.5V; T_j= -40°C...+150°C	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT}=10A; V_{SENSE}=4V; T_j=-40°C T_j=25°C...150°C	4200 4400	4900 4900	6000 5750	
dK_2/K_2	Current Sense Ratio Drift	I_{OUT}=10A; V_{SENSE}=4V; T_j=-40°C...+150°C	-8		+8	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT}=30A; V_{SENSE}=4V; T_j=-40°C T_j=25°C...150°C	4200 4400	4900 4900	5500 5250	
dK_3/K_3	Current Sense Ratio Drift	I_{OUT}=30A; V_{SENSE}=4V; T_j=-40°C...+150°C	-6		+6	%
I_{SENSEO}	Analog Sense Leakage Current	V_{CC}=6...16V; I_{OUT}=0A;V_{SENSE}=0V; T_j=-40°C...+150°C	0		10	µA
V_{SENSE}	Max Analog Sense Output Voltage	V_{CC}=5.5V; I_{OUT}=5A; R_{SENSE}=10KΩ V_{CC}>8V; I_{OUT}=10A; R_{SENSE}=10KΩ	2 4			V V
V_{SENSEH}	Sense Voltage in Overtemperature conditions	V_{CC}=13V; R_{SENSE}=3.9KΩ		5.5		V
$R_{VSENSEH}$	Analog sense output impedance in overtemperature condition	V_{CC}=13V; T_j>T_{TSD}; Output Open		400		Ω
t_{DSENSE}	Current sense delay response	to 90% I_{SENSE} (see note 3)			500	µs

Note: 3. Current sense signal delay after positive input slope

Figure 5. I_{OUT}/I_{SENSE} **versus** I_{OUT}

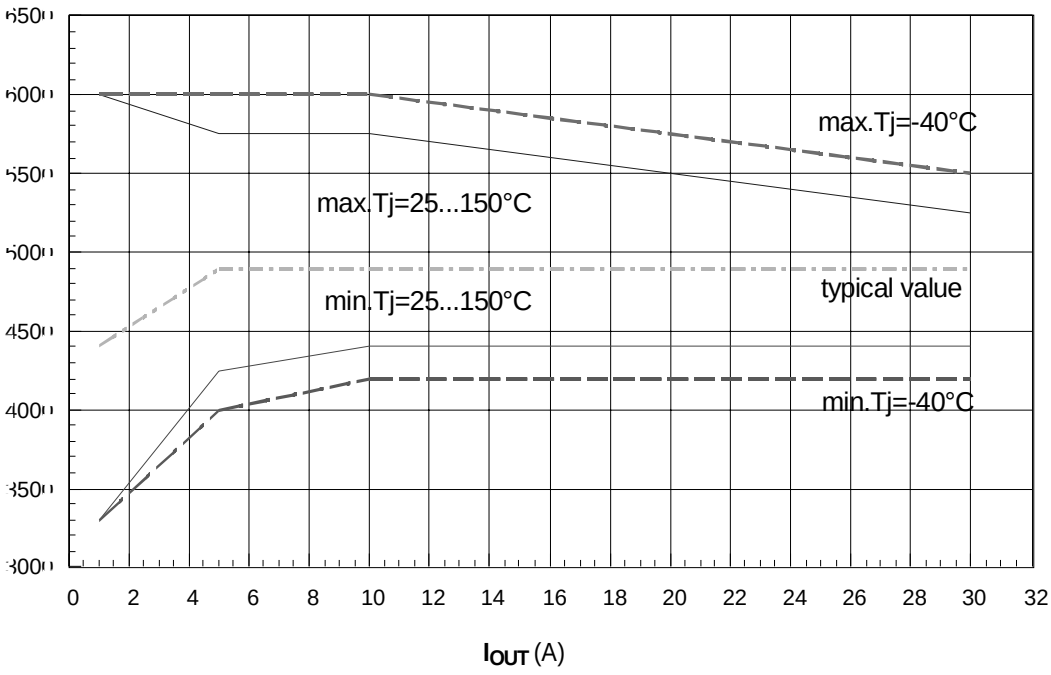


Figure 6. Switching Characteristics (Resistive load R_L=1.3Ω)

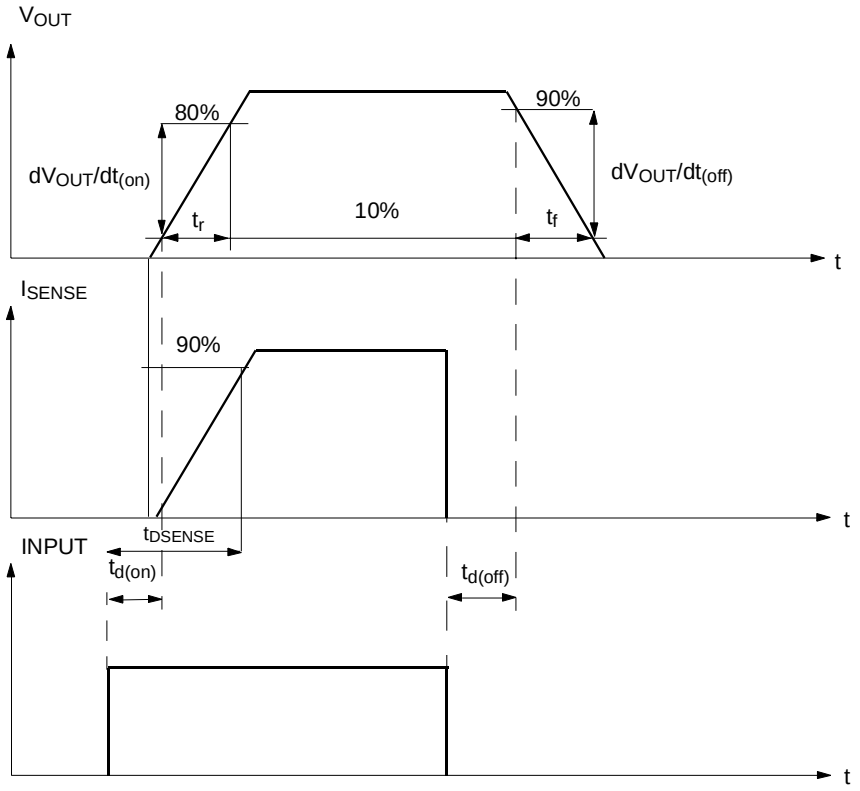


Table 11. Truth Table

CONDITIONS	INPUT	OUTPUT	SENSE
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overvoltage	L H	L L	0 0
Short circuit to GND	L H H	L L L	0 (T_j<T_{TSD}) 0 (T_j>T_{TSD}) V_{SENSEH}
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

Table 12. Electrical Transient Requirements On V_{CC} Pin

ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 7. Waveforms

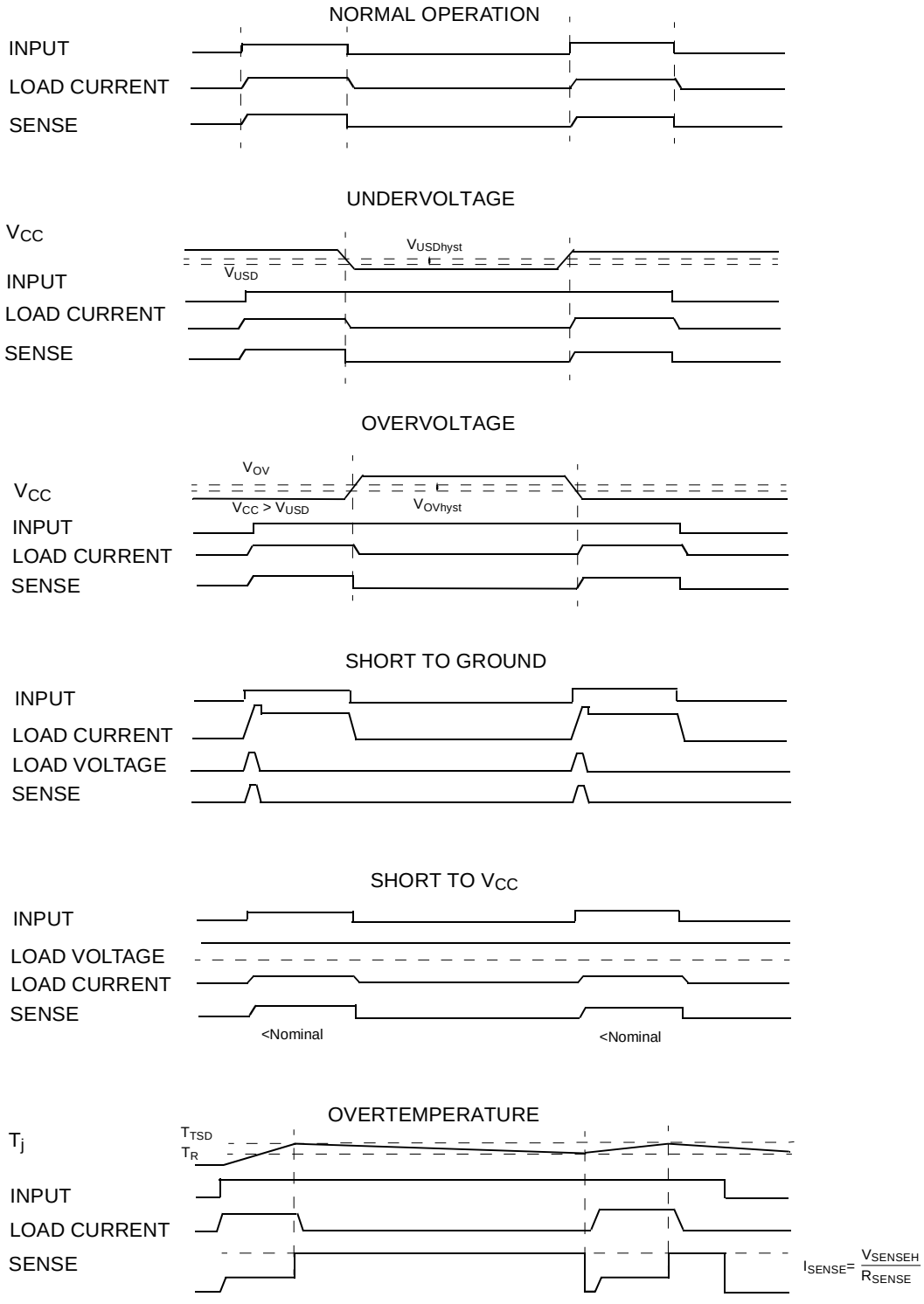
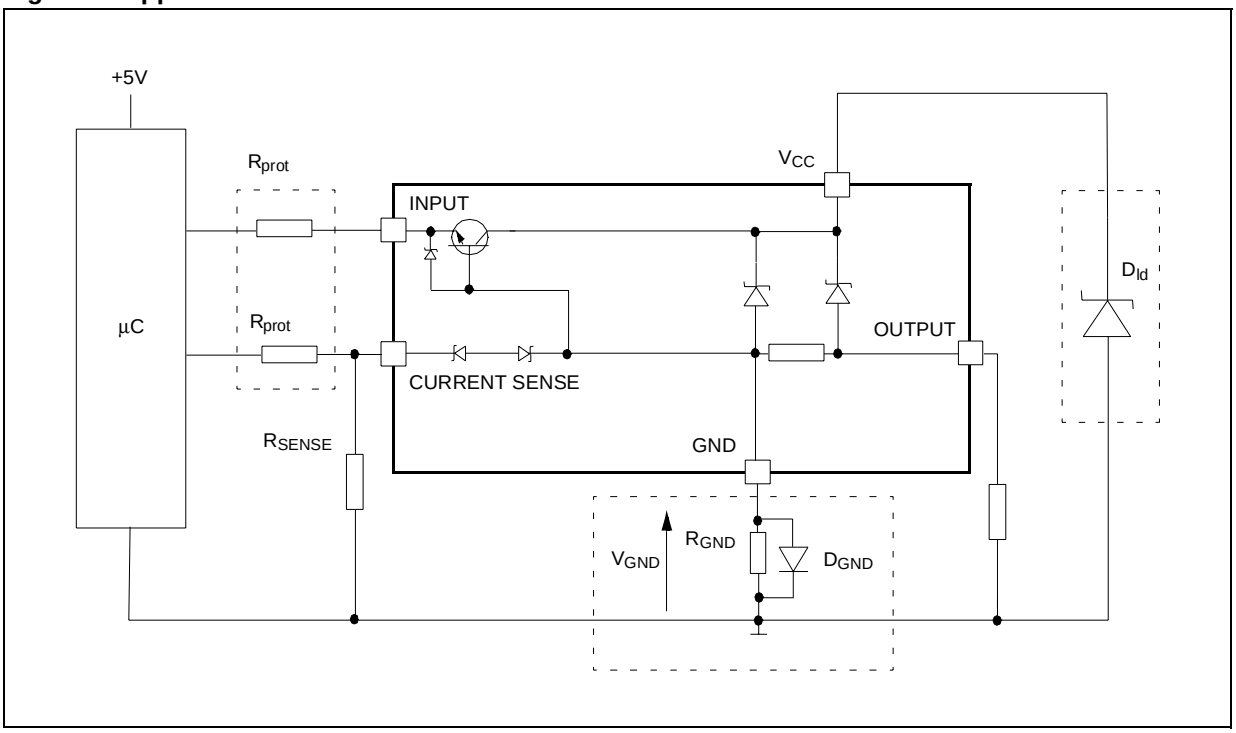


Figure 8. Application Schematic



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1) $R_{GND} \leq 600mV / (I_{S(on)max})$.

2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when $V_{CC}<0$: during reverse battery situations) is:

$P_D= (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT line is also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT pin is to leave it unconnected, while unused SENSE pin has to be connected to Ground pin.

LOAD DUMP PROTECTION

D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

µC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak}= - 100V and $I_{latchup} \geq 20mA$; $V_{OH\mu C} \geq 4.5V$

$5k\Omega \leq R_{prot} \leq 65k\Omega$.

Recommended R_{prot} value is 10kΩ.

Figure 9. Off State Output Current

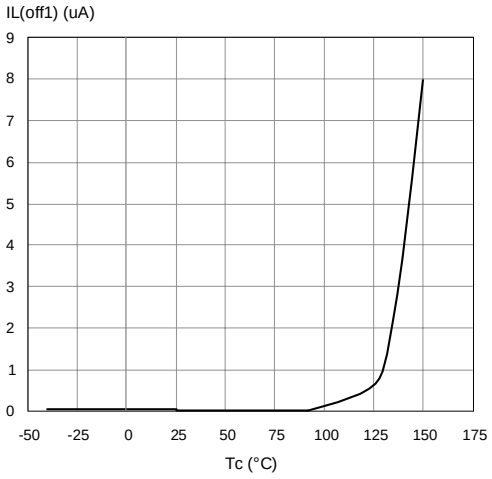


Figure 10. High Level Input Current

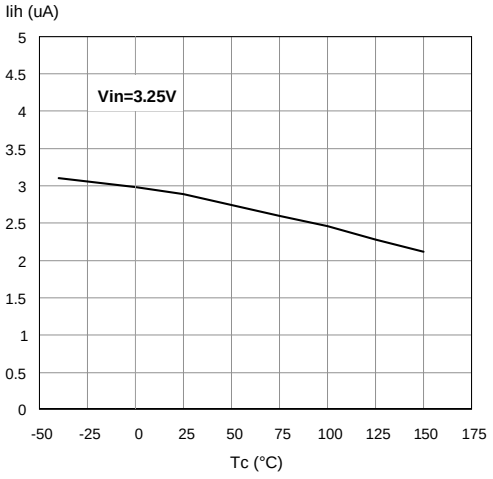


Figure 11. Input Clamp Voltage

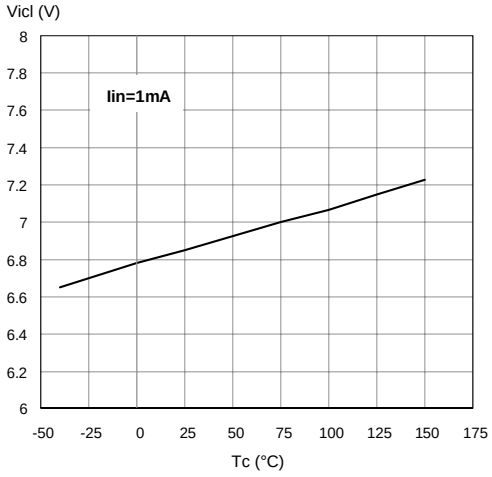


Figure 13. On State Resistance Vs V_{CC}

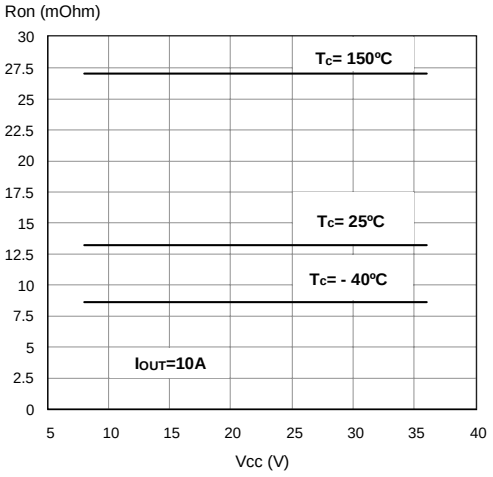


Figure 12. On State Resistance Vs T_{case}

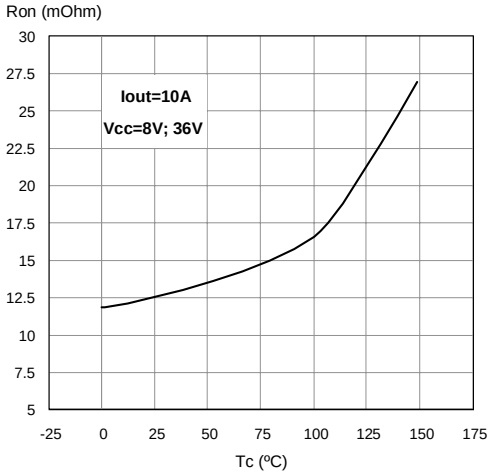


Figure 14. Input High Level

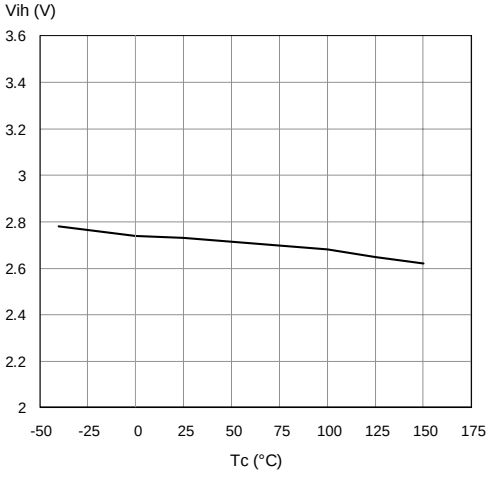


Figure 15. Input Low Level

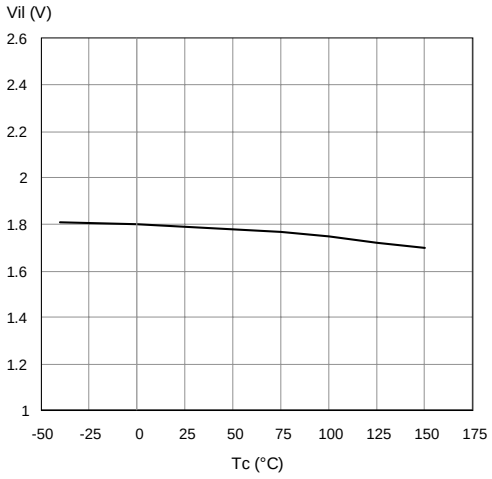


Figure 16. Turn-on Voltage Slope

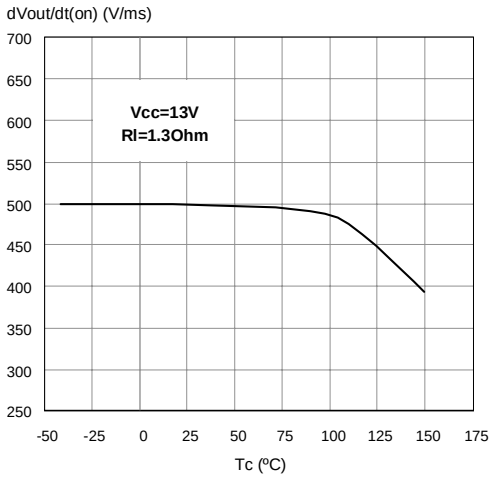


Figure 17. Overvoltage Shutdown

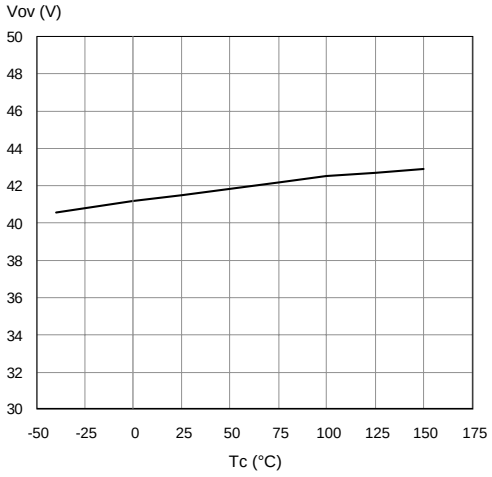


Figure 18. Input Hysteresis Voltage

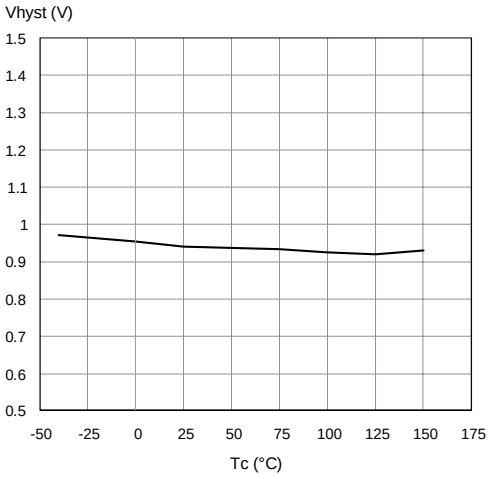


Figure 19. Turn-off Voltage Slope

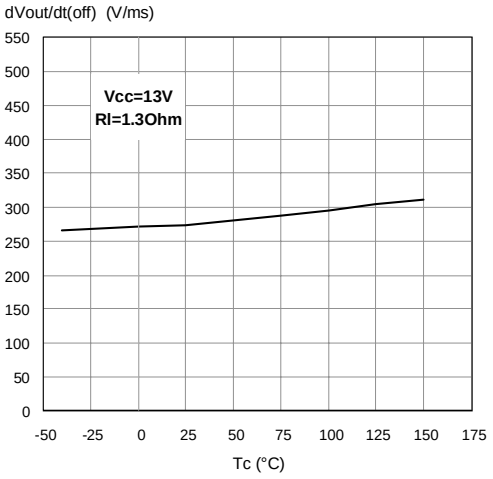


Figure 20. I_{LIM} Vs T_{case}

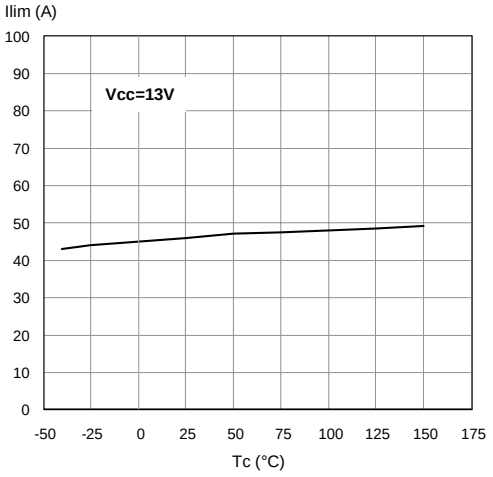
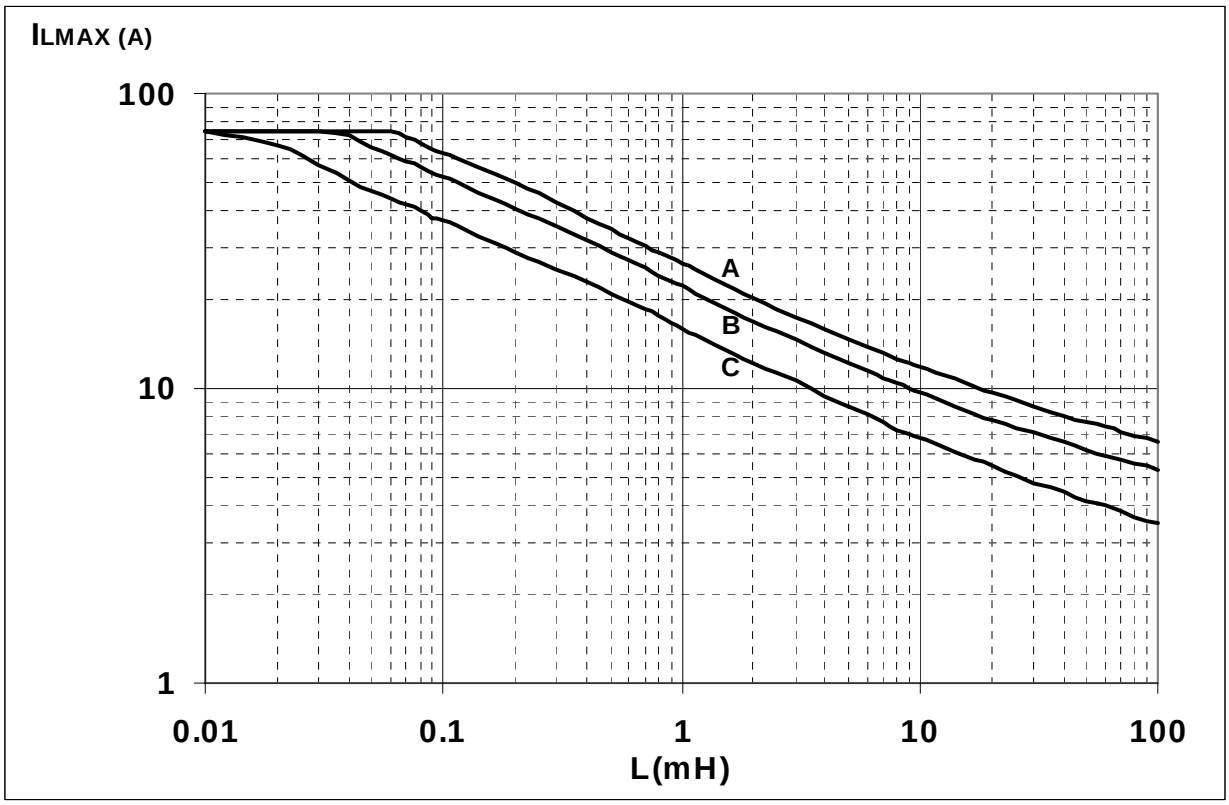


Figure 21. Maximum turn off current versus load inductance



A = Single Pulse at T_{Jstart}=150ºC

B= Repetitive pulse at T_{Jstart}=100ºC

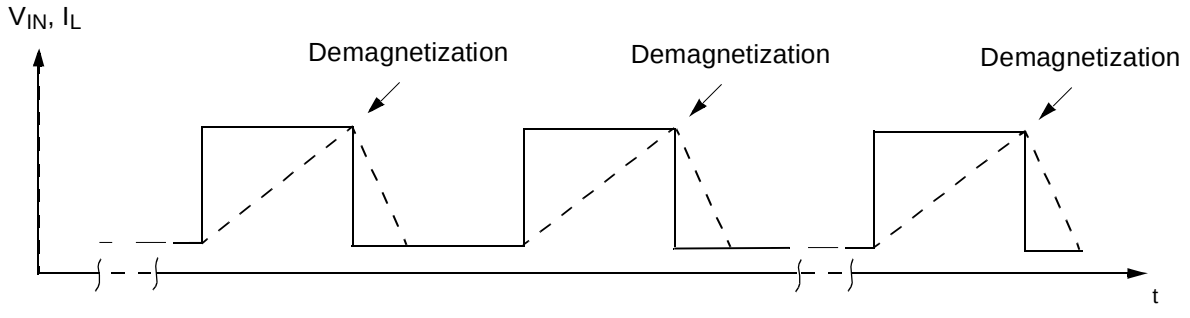
C= Repetitive Pulse at T_{Jstart}=125ºC

Conditions:

V_{CC}=13.5V

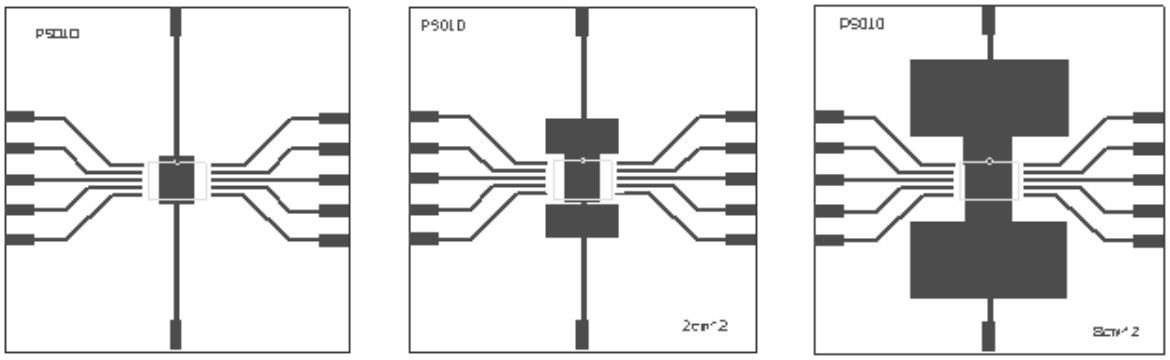
Values are generated with R_L=0Ω

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



PowerSO-10™ Thermal Data

Figure 22. PowerSO-10™ PC Board



Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35µm, Copper areas: from minimum pad lay-out to 8cm^2).

Figure 23. $R_{thj\text{-}amb}$ Vs PCB copper area in open box free air condition

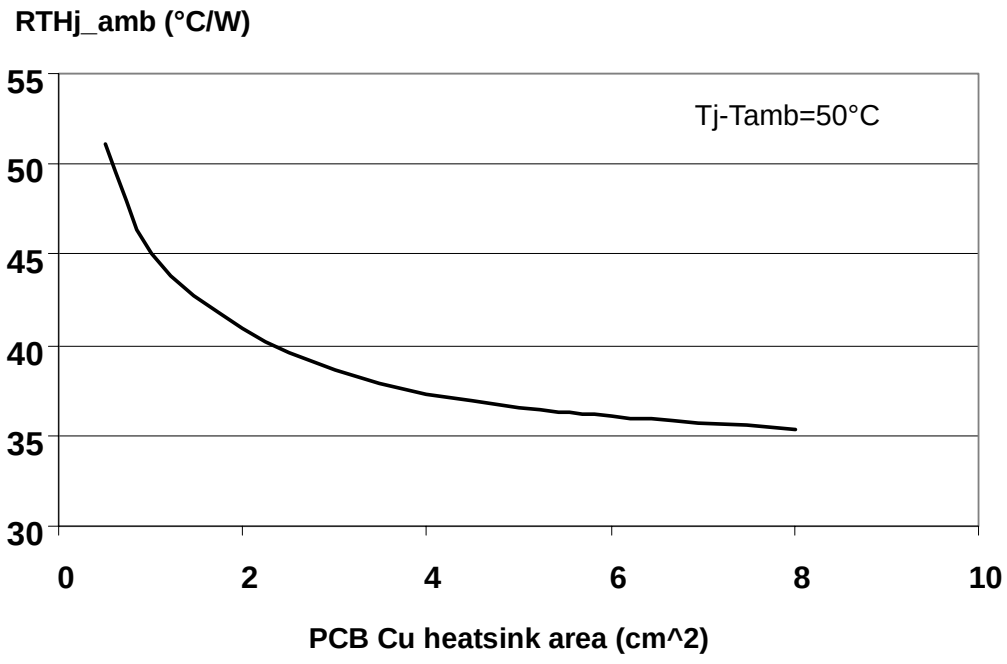


Figure 24. PowerSO-10 Thermal Impedance Junction Ambient Single Pulse

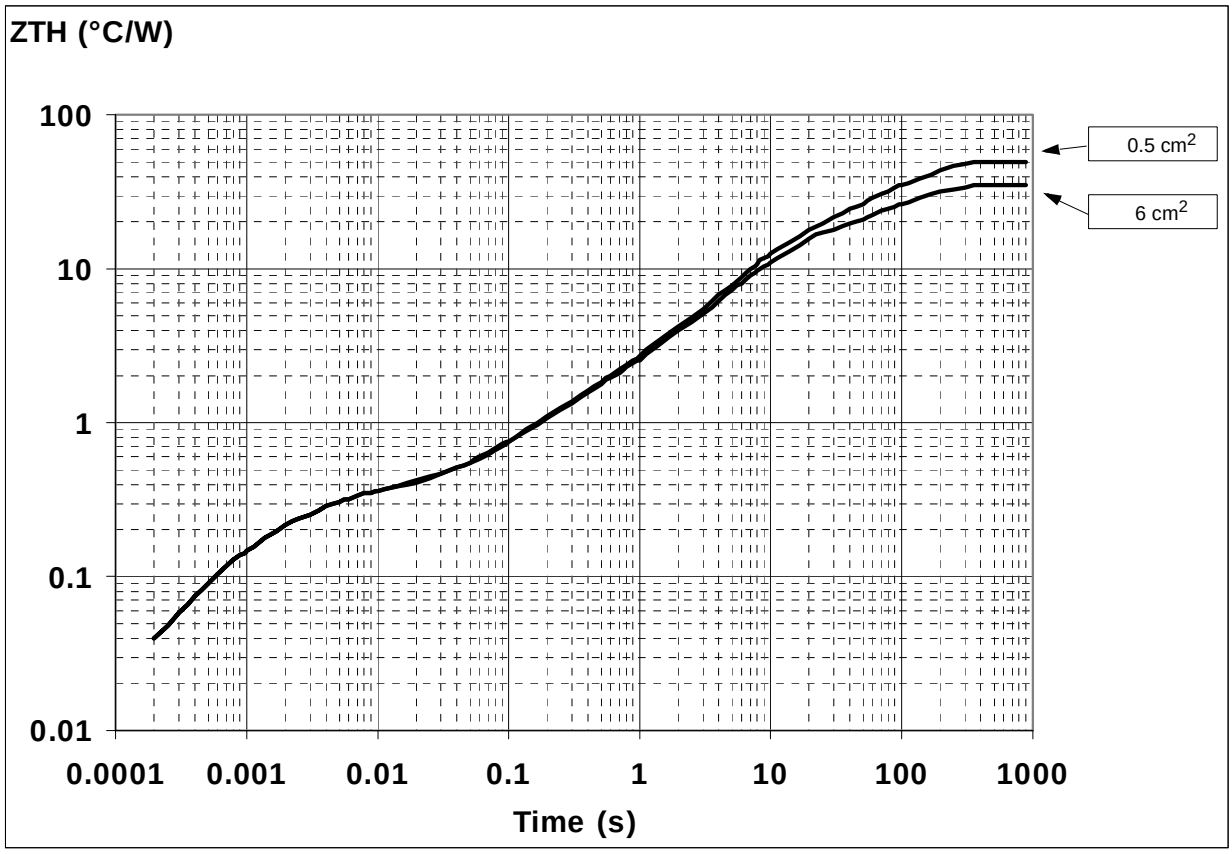
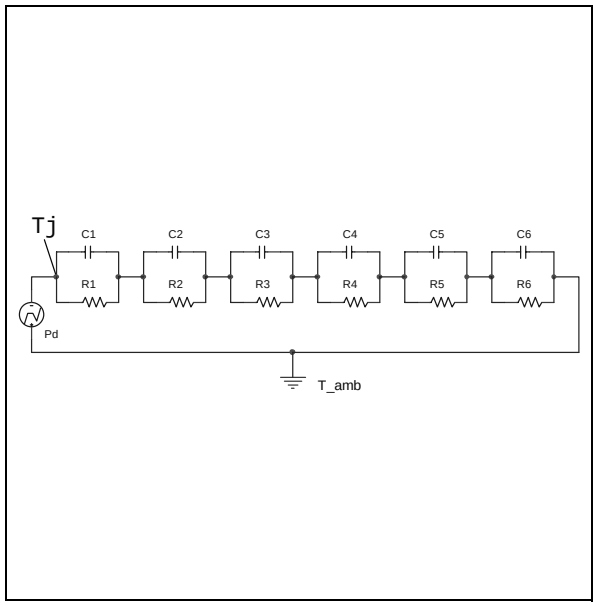


Figure 25. Thermal fitting model of a single channel HSD in PowerSO-10



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where $\delta = t_p / T$

Table 13. Thermal Parameter

Area/island (cm^2)	Footprint	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3(°C/W)	0.2	
R4 (°C/W)	0.8	
R5 (°C/W)	12	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0015	
C2 (W.s/°C)	7.00E-03	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.75	
C6 (W.s/°C)	3	5

PACKAGE MECHANICAL

Table 14. PowerSO-10™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	3.35		3.65
A (*)	3.4		3.6
A1	0.00		0.10
B	0.40		0.60
B (*)	0.37		0.53
C	0.35		0.55
C (*)	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2 (*)	7.30		7.50
E4	5.90		6.10
E4 (*)	5.90		6.30
e		1.27	
F	1.25		1.35
F (*)	1.20		1.40
H	13.80		14.40
H (*)	13.85		14.35
h		0.50	
L	1.20		1.80
L (*)	0.80		1.10
a	0º		8º
α (*)	2º		8º

Note: (*) Muar only POA P013P

Figure 26. PowerSO-10™ Package Dimensions

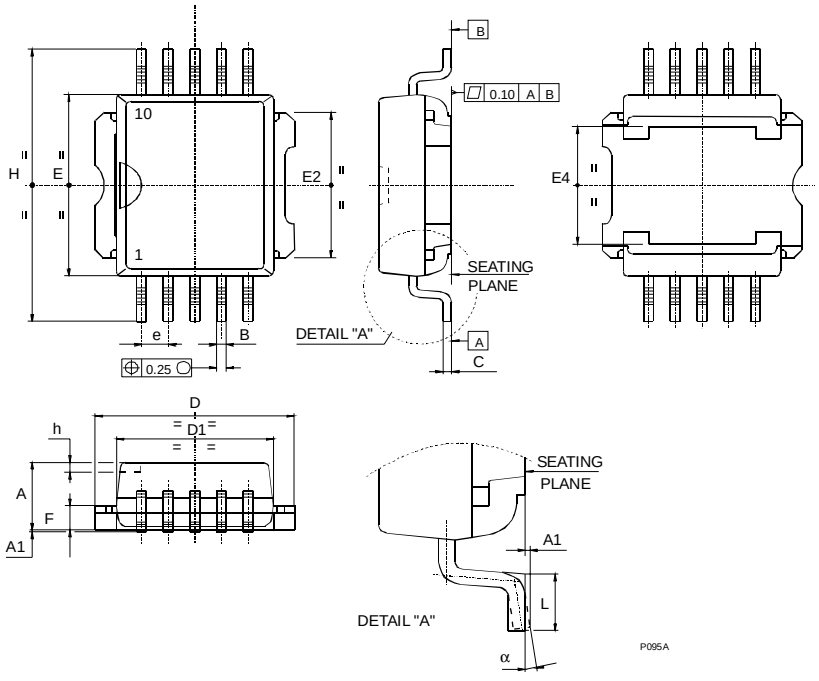
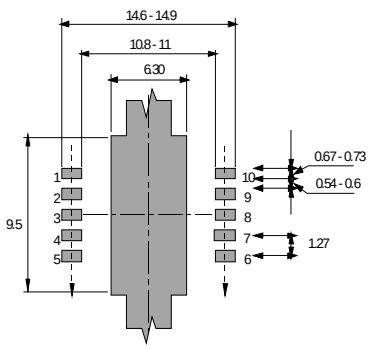
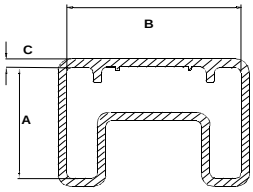
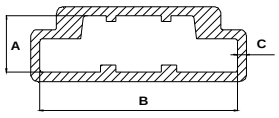


Figure 27. PowerSO-10™ Suggested Pad Layout And Tube Shipment (No Suffix)





CASABLANCA

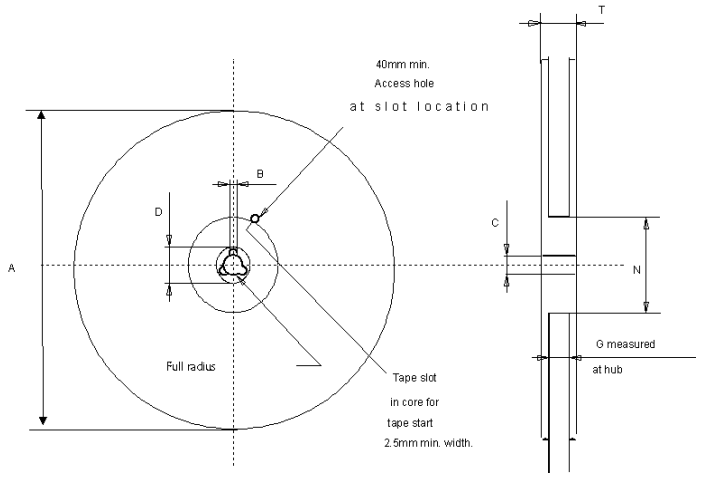


MUAR

All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

Figure 28. Tape And Reel Shipment (suffix "TR")



REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

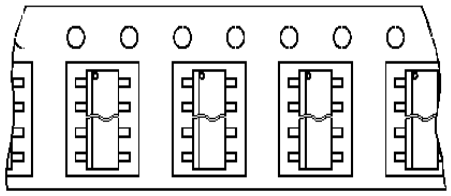
All dimensions are in mm.

TAPE DIMENSIONS

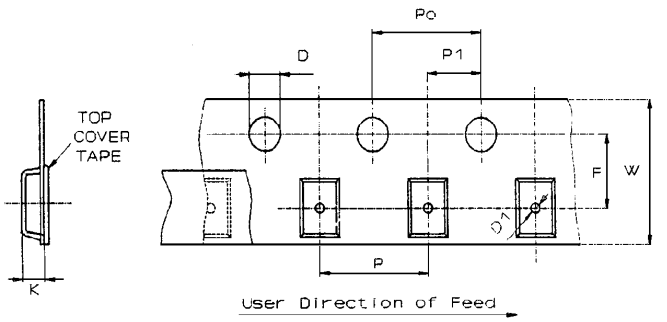
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

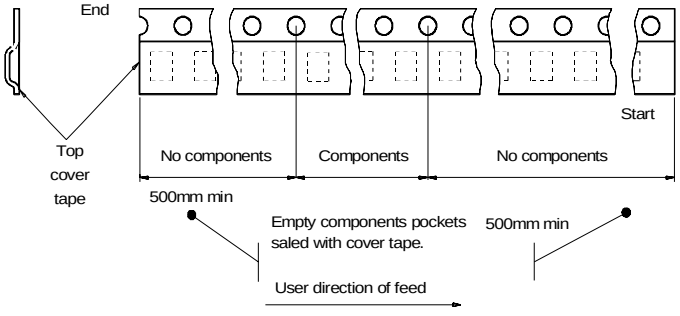
Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	24
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.



User Direction of Feed





REVISION HISTORY

Table 15. Revision History

Date	Revision	Description of Changes
Oct. 2004	1	- First Issue.