



# VN5016AJ-E

## SINGLE CHANNEL HIGH SIDE DRIVER WITH ANALOG CURRENT SENSE FOR AUTOMOTIVE APPLICATIONS

ADVANCE DATA

Table 1. General Features

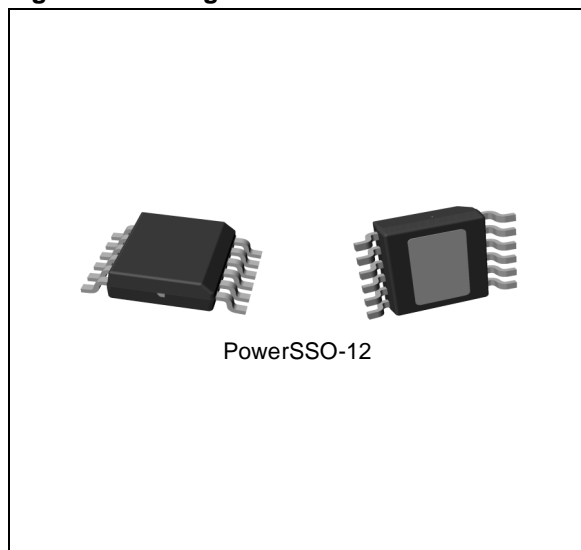
TYPE	V <sub>CC</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
VN5016AJ-E	41V	16mΩ	40A

- OUTPUT CURRENT: 40A
- 3.0V CMOS COMPATIBLE INPUT
- CURRENT SENSE DISABLE
- PROPORTIONAL LOAD CURRENT SENSE
- UNDERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT DOWN
- CURRENT AND POWER LIMITATION
- VERY LOW STAND-BY CURRENT
- PROTECTION AGAINST LOSS OF GROUND AND LOSS OF V<sub>CC</sub>
- VERY LOW ELECTROMAGNETIC SUSCEPTIBILITY
- OPTIMIZED ELECTROMAGNETIC EMISSION
- REVERSE BATTERY PROTECTION (\*)
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

### DESCRIPTION

The VN5016AJ-E is a monolithic device made using STMicroelectronics VIPower technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V<sub>CC</sub> pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

Figure 1. Package



This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS\_DIS is driven low or left open. When CS\_DIS is driven high, the CURRENT SENSE pin is in a high impedance condition. Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shut-down intervention. Thermal shut-down with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

Table 2. Order Codes

Package	Tube	Tape and Reel
PowerSSO-12	VN5016AJ-E	VN5016AJTR-E

Note: (\*) See application schematic at page 8

Rev. 2

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This is preliminary information on a new product now in development. Details are subject to change without notice.

Figure 2. Block Diagram

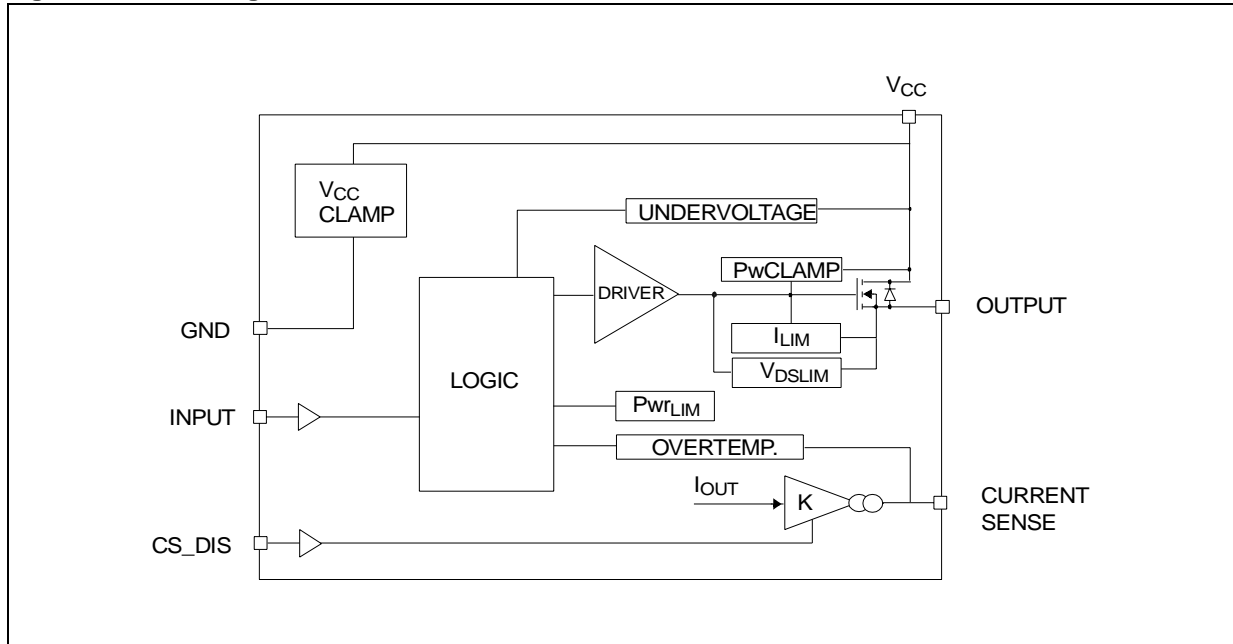
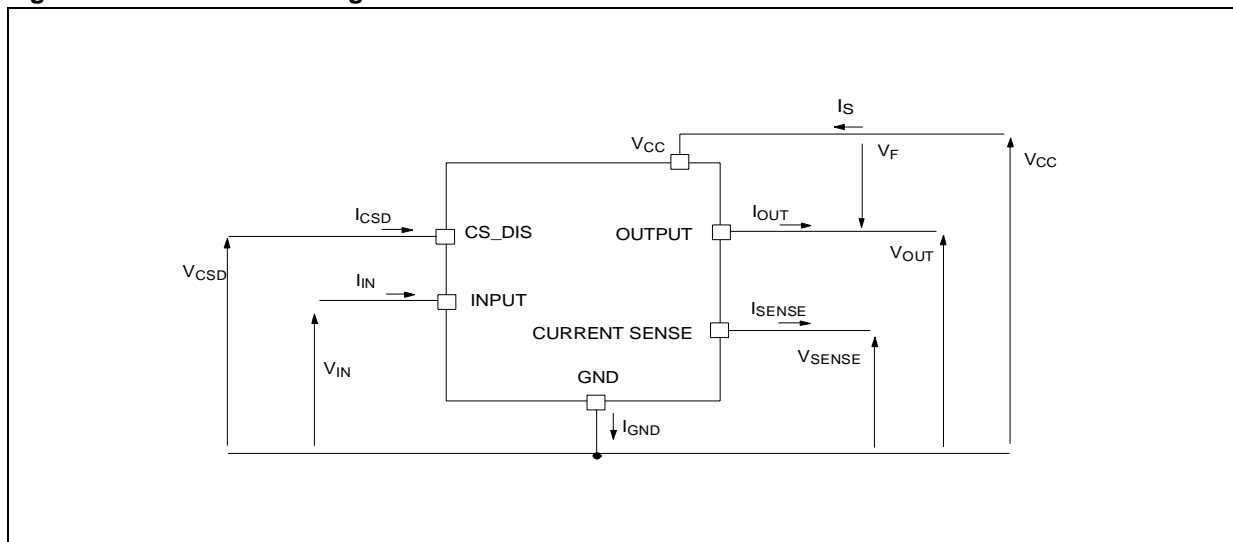
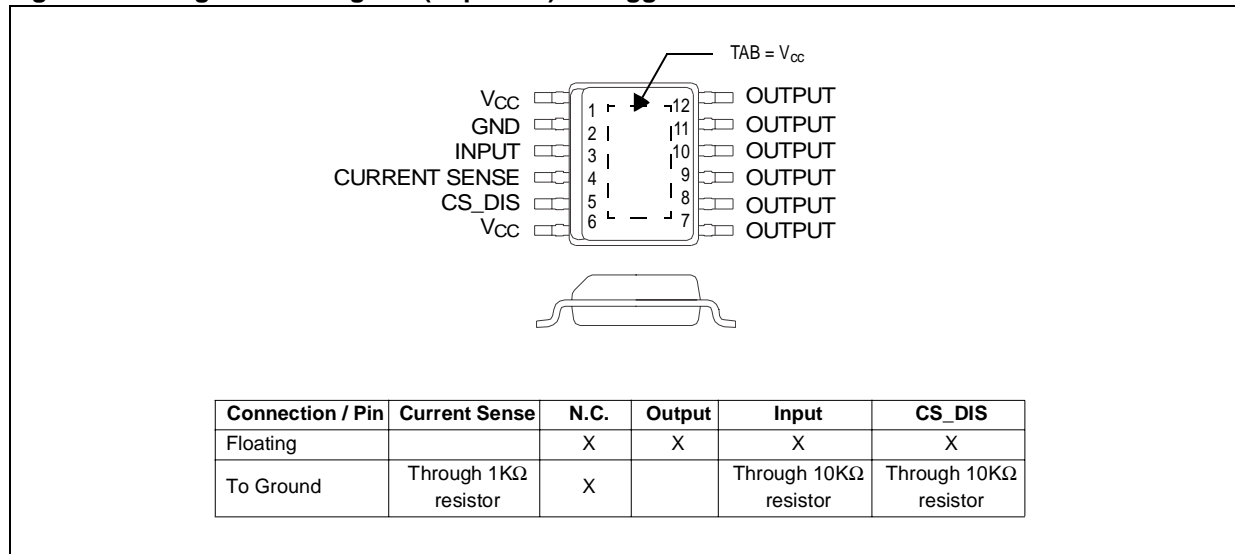


Table 3. Pin Function

Name	Function
V <sub>CC</sub>	Battery connection
OUTPUT	Power output
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state
CURRENT SENSE	Analog current sense pin, delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin

Figure 3. Current and Voltage Conventions



**Figure 4. Configuration Diagram (Top View) & Suggested Connections For Unused and n.c. Pins****Table 4. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
$I_{OUT}$	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-30	A
$I_{IN}$	DC input current	-1 to 10	mA
$I_{CSD}$	DC current sense disable input current	-1 to 10	mA
$V_{CSSENSE}$	Current sense maximum voltage	$V_{CC}-41$	V
		$+V_{CC}$	V
$V_{ESD}$	Electrostatic discharge ( $R=1.5k\Omega$ ; $C=100pF$ )	2000	V
$T_j$	Junction operating temperature	-40 to 150	$^{\circ}C$
$T_{stg}$	Storage temperature	-55 to 150	$^{\circ}C$

**Table 5. Thermal Data**

Symbol	Parameter	Max Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.3	$^{\circ}C/W$
$R_{thj-amb}$	Thermal resistance junction-ambient	75 (see note 1)	$^{\circ}C/W$

Note: 1. When mounted on a standard single-sided FR4 board with 0.5cm<sup>2</sup> of Cu (at least 35  $\mu$ m thick) connected to TAB.

**ELECTRICAL CHARACTERISTICS** ( $8V < V_{CC} < 36V$ ;  $-40^{\circ}C < T_j < 150^{\circ}C$ , unless otherwise specified)

**Table 6. Power Section**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating supply voltage		4.5	13	36	V
$V_{USD}$	Undervoltage shutdown			3	4.5	V
$V_{USDhyst}$	Undervoltage Shut-down hysteresis			0.5		V
$R_{ON}$	On state resistance	$I_{OUT}=5A$ ; $T_j=25^{\circ}C$			16	m $\Omega$
		$I_{OUT}=5A$ ; $T_j=150^{\circ}C$			32	m $\Omega$
		$I_{OUT}=5A$ ; $V_{CC}=5V$ ; $T_j=25^{\circ}C$			20	m $\Omega$
$V_{clamp}$	Clamp Voltage	$I_S=20mA$	41	46	52	V
$I_S$	Supply current	Off State; $V_{CC}=13V$ ; $T_j=25^{\circ}C$ ; $V_{IN}=V_{OUT}=V_{SENSE}=V_{CSD}=0V$		2(**)	5(**)	$\mu A$
		On State; $V_{CC}=13V$ ; $V_{IN}=5V$ ; $I_{OUT}=0A$		1.5	3	mA
$I_{L(off)}$	Off state output current	$V_{IN}=V_{OUT}=0V$ ; $V_{CC}=13V$ ; $T_j=25^{\circ}C$	0		3	$\mu A$
		$V_{IN}=V_{OUT}=0V$ ; $V_{CC}=13V$ ; $T_j=125^{\circ}C$	0		5	$\mu A$

Note: (\*\*) PowerMOS leakage included

**Table 7. Switching** ( $V_{CC}=13V$ )

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L=2.6\Omega$		15		$\mu s$
$t_{d(off)}$	Turn-off delay time	$R_L=2.6\Omega$		40		$\mu s$
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	$R_L=2.6\Omega$		0.3		V/ $\mu s$
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	$R_L=2.6\Omega$		0.35		V/ $\mu s$
$W_{ON}$	Switching losses energy at turn-on	$R_L=2.6\Omega$		TBD		mJ
$W_{OFF}$	Switching losses energy at turn-off	$R_L=2.6\Omega$		TBD		mJ

**ELECTRICAL CHARACTERISTICS** (continued)**Table 8. Logic Input**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>IL</sub>	Input low level voltage				0.9	V
I <sub>IL</sub>	Low level input current	V <sub>IN</sub> =0.9V	1			μA
V <sub>IH</sub>	Input high level voltage		2.1			V
I <sub>IH</sub>	High level input current	V <sub>IN</sub> =2.1V			10	μA
V <sub>I(hyst)</sub>	Input hysteresis voltage		0.25			V
V <sub>ICL</sub>	Input clamp voltage	I <sub>IN</sub> =1mA I <sub>IN</sub> =-1mA	5.5		TBD	V
				-0.7		V
V <sub>CS<sub>DL</sub></sub>	CS_DIS low level voltage				0.9	V
I <sub>CS<sub>DL</sub></sub>	Low level CS_DIS current	V <sub>CS<sub>D</sub></sub> =0.9V	1			μA
V <sub>CS<sub>DH</sub></sub>	CS_DIS high level voltage		2.1			V
I <sub>CS<sub>DH</sub></sub>	High level CS_DIS current	V <sub>CS<sub>D</sub></sub> =2.1V			10	μA
V <sub>CS<sub>D(hyst)</sub></sub>	CS_DIS hysteresis voltage		0.25			V
V <sub>CS<sub>CL</sub></sub>	CS_DIS clamp voltage	I <sub>CS<sub>D</sub></sub> =1mA I <sub>CS<sub>D</sub></sub> =-1mA	5.5		TBD	V
				-0.7		V

**Table 9. Protections and Diagnostics** (see note 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I <sub>limH</sub>	DC Short circuit current	V <sub>CC</sub> =13V 5V<V <sub>CC</sub> <36V	40	60	80	A
					80	A
I <sub>limL</sub>	Short circuit current during thermal cycling	V <sub>CC</sub> =13V T <sub>R</sub> <T <sub>j</sub> <T <sub>TSD</sub>		24		A
T <sub>TSD</sub>	Shutdown temperature		150	175	200	°C
T <sub>R</sub>	Reset temperature		T <sub>RS</sub> + 1	T <sub>RS</sub> + 5		°C
T <sub>RS</sub>	Thermal reset of STATUS		135			°C
T <sub>HYST</sub>	Thermal hysteresis (T <sub>TSD</sub> -T <sub>R</sub> )			7		°C
V <sub>DEMAG</sub>	Turn-off output voltage clamp	I <sub>OUT</sub> =2A; V <sub>IN</sub> =0; L=6mH	V <sub>CC</sub> -41	V <sub>CC</sub> -46	V <sub>CC</sub> -52	V
V <sub>ON</sub>	Output voltage drop limitation	I <sub>OUT</sub> =0.3A; T <sub>j</sub> = -40°C...+150°C (see figure 9)		25		mV

Note: 2. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

**ELECTRICAL CHARACTERISTICS** (continued)

**Table 10. Current Sense** ( $8V < V_{CC} < 16V$ )

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
K <sub>1</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> =1.5A; V <sub>SENSE</sub> =0.5V; V <sub>CSD</sub> =0V; T <sub>j</sub> = -40°C...150°C	TBD	5000	TBD	
K <sub>2</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> =10A; V <sub>SENSE</sub> =4V; V <sub>CSD</sub> =0V; T <sub>j</sub> =-40°C T <sub>j</sub> =25°C...150°C	TBD TBD	5000 5000	TBD TBD	
K <sub>3</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> =25A; V <sub>SENSE</sub> =4V; V <sub>CSD</sub> =0V; T <sub>j</sub> =-40°C T <sub>j</sub> =25°C...150°C	TBD TBD	5000 5000	TBD TBD	
I <sub>SENSE0</sub>	Analog sense current	I <sub>OUT</sub> =0A; V <sub>SENSE</sub> =0V; V <sub>CSD</sub> =5V; V <sub>IN</sub> =0V; T <sub>j</sub> =-40°C...150°C V <sub>CSD</sub> =0V; V <sub>IN</sub> =5V; T <sub>j</sub> =-40°C...150°C	0 0		5 10	μA μA
V <sub>SENSE</sub>	Max analog sense output voltage	I <sub>OUT</sub> =15A; V <sub>CSD</sub> =0V; R <sub>SENSE</sub> =3.9KΩ	5			V
V <sub>SENSEH</sub>	Analog sense output voltage in overtemperature condition	V <sub>CC</sub> =13V; R <sub>SENSE</sub> =3.9KΩ		9		V
I <sub>SENSEH</sub>	Analog sense output current in overtemperature condition	V <sub>CC</sub> =13V, V <sub>SENSE</sub> =5V		8		mA
t <sub>DSENSE1H</sub>	Delay Response time from falling edge of CS_DIS pin	V <sub>SENSE</sub> <4V, 1.5A<I <sub>OUT</sub> <25A I <sub>SENSE</sub> =90% of I <sub>SENSE max</sub> (see fig 5)		50	100	μs
t <sub>DSENSE1L</sub>	Delay Response time from rising edge of CS_DIS pin	V <sub>SENSE</sub> <4V, 1.5A<I <sub>OUT</sub> <25A I <sub>SENSE</sub> =10% of I <sub>SENSE max</sub> (see fig 5)		5	20	μs
t <sub>DSENSE2H</sub>	Delay Response time from rising edge of INPUT pin	V <sub>SENSE</sub> <4V, 1.5A<I <sub>OUT</sub> <25A I <sub>SENSE</sub> =90% of I <sub>SENSE max</sub> (see fig 5)		270	600	μs
t <sub>DSENSE2L</sub>	Delay Response time from falling edge of INPUT pin	V <sub>SENSE</sub> <4V, 1.5A<I <sub>OUT</sub> <25A I <sub>SENSE</sub> =10% of I <sub>SENSE max</sub> (see fig 5)		100	250	μs

**Table 11. Truth Table**

CONDITIONS	INPUT	OUTPUT	SENSE (V <sub>CSD</sub> =0V) (see note 3)
Normal operation	L	L	0
	H	H	Nominal
Overtemperature	L	L	0
	H	L	V <sub>SENSEH</sub>
Undervoltage	L	L	0
	H	L	0
Short circuit to GND	L	L	0
	H	L	0
Short circuit to V <sub>CC</sub>	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

Note: 3. If the V<sub>CSD</sub> is high, the SENSE output is at a high impedance.

Figure 5.

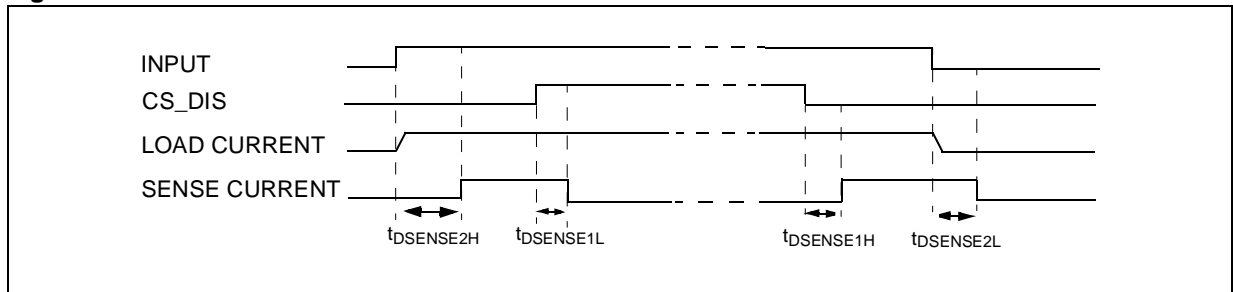


Figure 6. Switching Characteristics

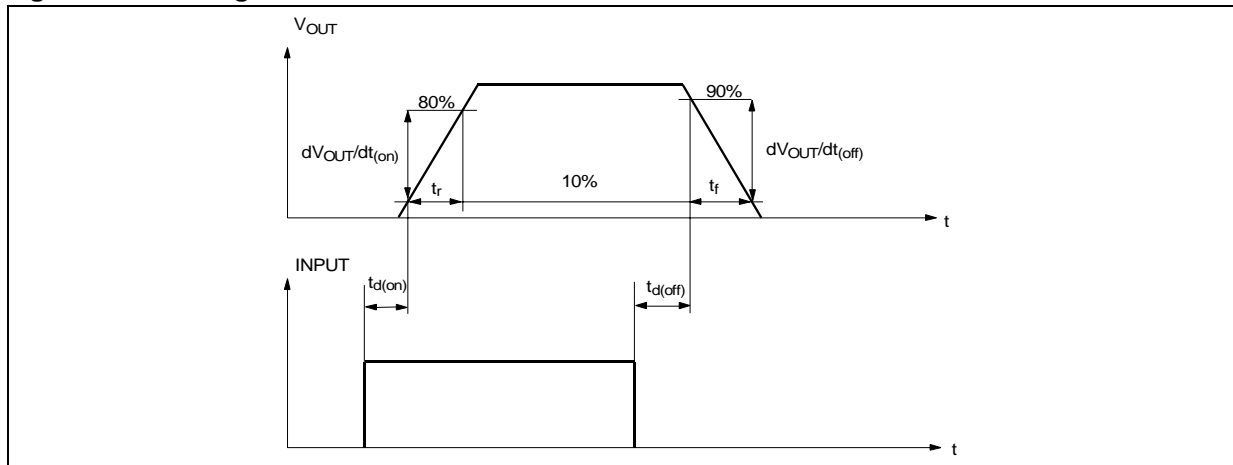


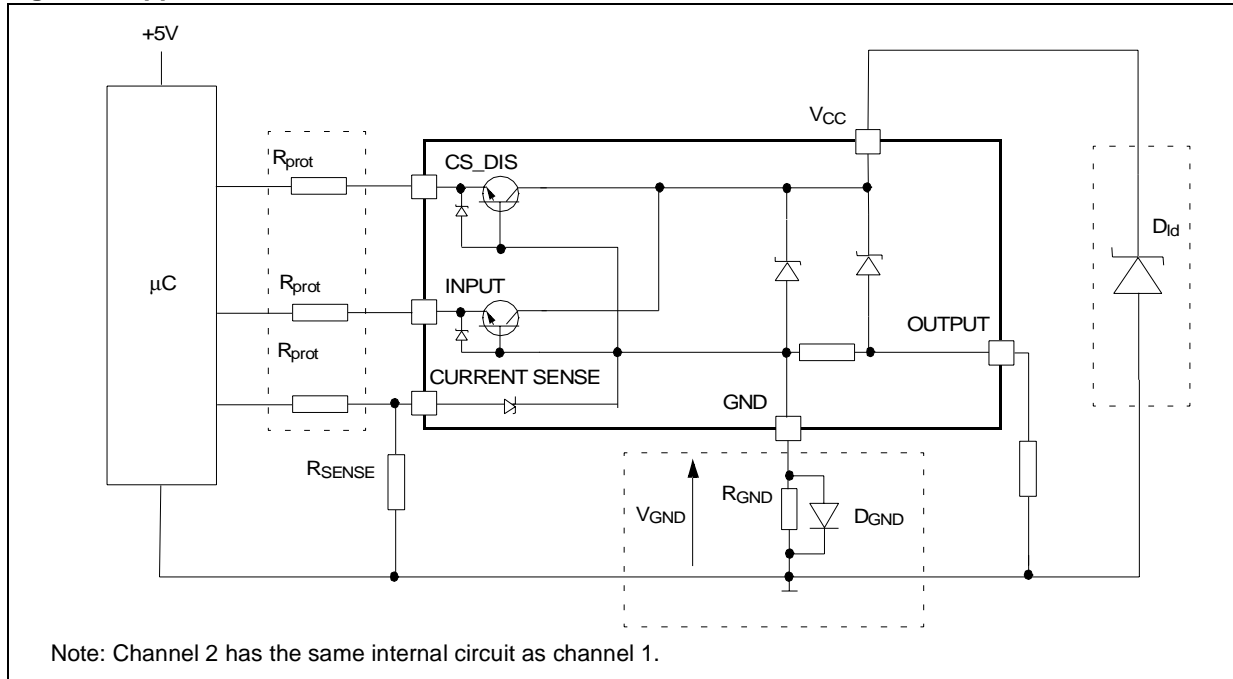
Table 12. Electrical Transient Requirements

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 $\Omega$
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 $\Omega$
3a	-25 V	-50 V	-100 V	-150 V	0.1 $\mu$ s 50 $\Omega$
3b	+25 V	+50 V	+75 V	+100 V	0.1 $\mu$ s 50 $\Omega$
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 $\Omega$
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 $\Omega$

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 7. Application Schematic



**GND PROTECTION NETWORK AGAINST REVERSE BATTERY**

Solution 1: Resistor in the ground line (R<sub>GND</sub> only). This can be used with any type of load.

The following is an indication on how to dimension the R<sub>GND</sub> resistor.

- 1)  $R_{GND} \leq 600mV / (I_{S(on)max})$ .
- 2)  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where -I<sub>GND</sub> is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R<sub>GND</sub> (when V<sub>CC</sub><0: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where I<sub>S(on)max</sub> becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R<sub>GND</sub> will produce a shift (I<sub>S(on)max</sub> \* R<sub>GND</sub>) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R<sub>GND</sub>.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D<sub>GND</sub>) in the ground line.

A resistor (R<sub>GND</sub>=1kΩ) should be inserted in parallel to D<sub>GND</sub> if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift (j600mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

**LOAD DUMP PROTECTION**

D<sub>id</sub> is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V<sub>CC</sub> max DC rating. The same applies if the device is subject to transients on the V<sub>CC</sub> line that are greater than the ones shown in the ISO T/R 7637/1 table.

**µC I/Os PROTECTION:**

If a ground protection network is used and negative transient are present on the V<sub>CC</sub> line, the control pins will be pulled negative. ST suggests to insert a resistor (R<sub>prot</sub>) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OHµC} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For V<sub>CCpeak</sub>= - 100V and I<sub>latchup</sub> ≥ 20mA; V<sub>OHµC</sub> ≥ 4.5V  
 $5k\Omega \leq R_{prot} \leq 65k\Omega$ .

Recommended R<sub>prot</sub> value is 10kΩ.



Figure 8. Waveforms

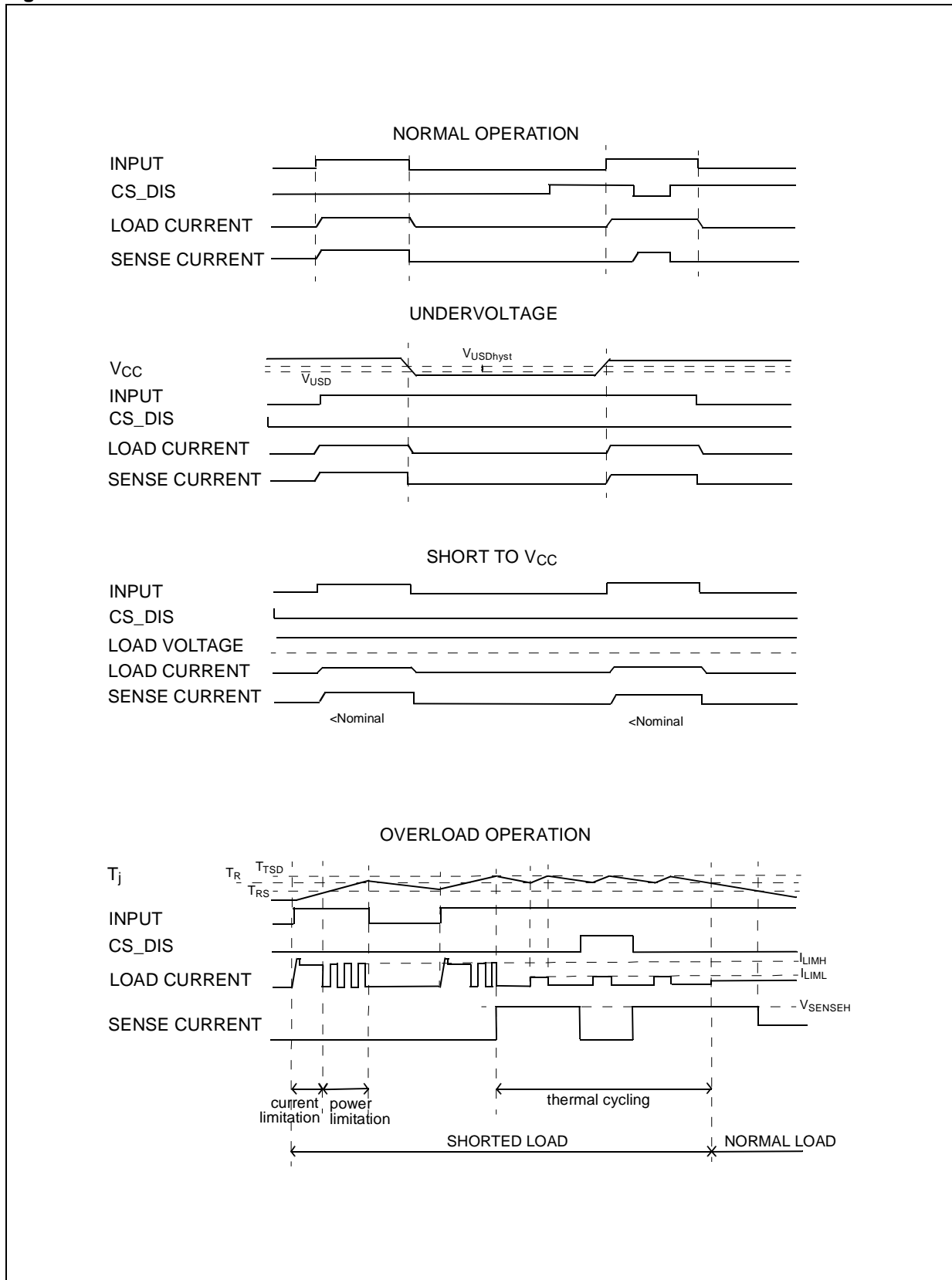
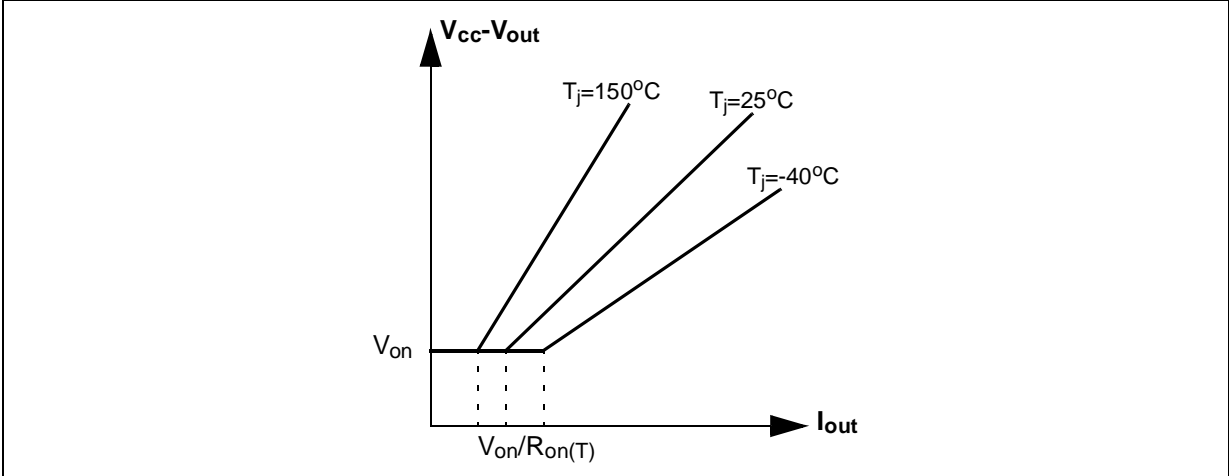


Figure 9.

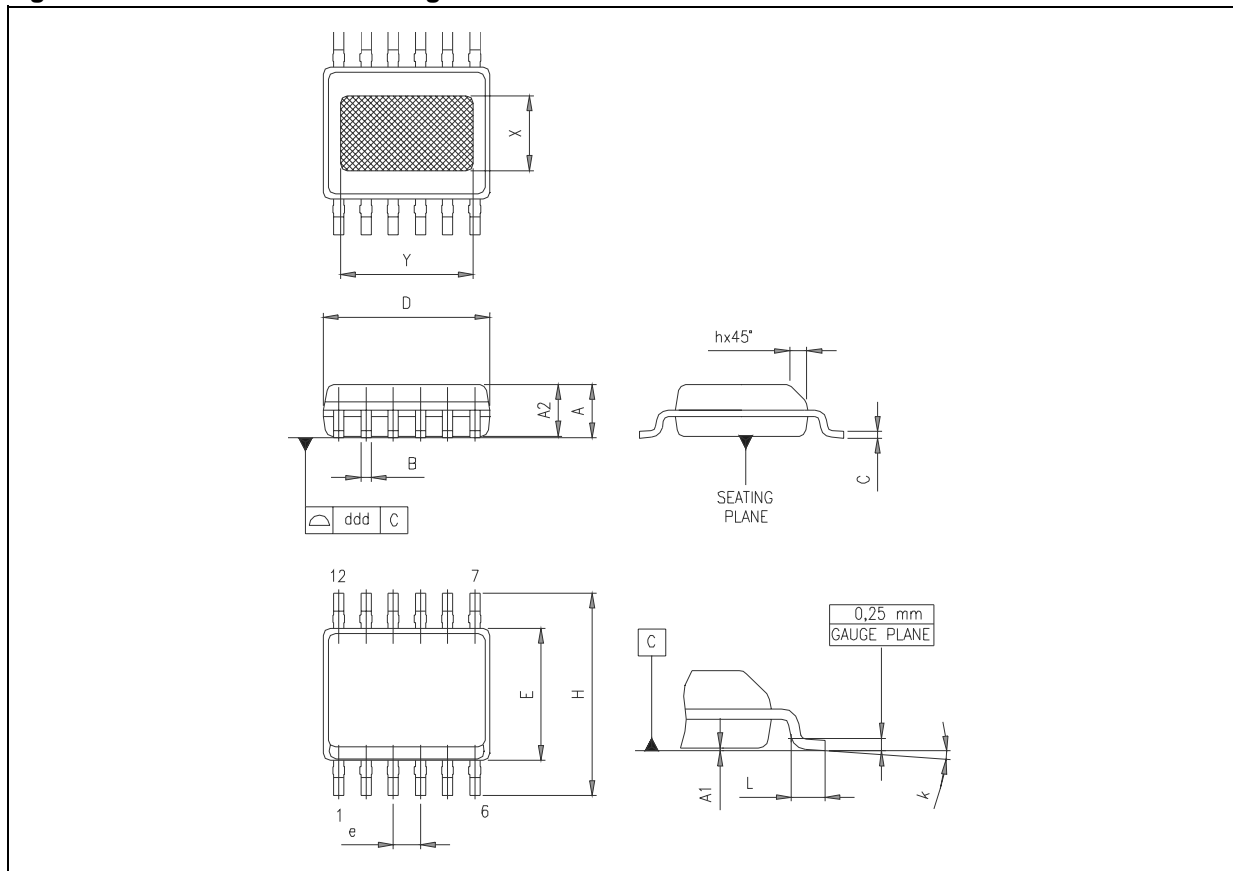


## PACKAGE MECHANICAL

Table 13. PowerSSO-12™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	1.900		2.500
Y	3.600		4.200
ddd			0.100

Figure 10. PowerSSO-12™ Package Dimensions



**REVISION HISTORY**

**Table 14. Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
Oct. 2004	1	- First issue.
Jan. 2005	2	- Minor text changes.

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