

features

- Power-On Reset Generator With Fixed Delay Time of 200 ms (TPS3823/4/5/8) or 25 ms (TPS3820)
- Manual Reset Input (TPS3820/3/5/8)
- Reset Output Available in Active-Low (TPS3820/3/4/5), Active-High (TPS3824) and Open-Drain (TPS3828)
- Supply Voltage Supervision Range 2.5 V, 3 V, 3.3 V, 5 V
- Watchdog Timer (TPS3820/3/4/8)
- Supply Current of 15 μ A (Typ)
- SOT23-5 Package
- Temperature Range . . . -40°C to 85°C

applications

- Applications Using DSPs, Microcontrollers, or Microprocessors
- Industrial Equipment
- Programmable Controls
- Automotive Systems
- Portable/Battery-Powered Equipment
- Intelligent Instruments
- Wireless Communications Systems
- Notebook/Desktop Computeres

description

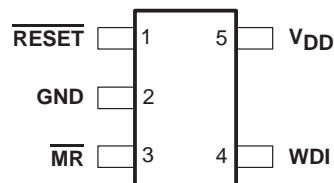
The TPS382x family of supervisors provides circuit initialization and timing supervision, primarily for DSP and processor-based systems.

During power-on, $\overline{\text{RESET}}$ is asserted when supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors V_{DD} and keeps $\overline{\text{RESET}}$ active as long as V_{DD} remains below the threshold voltage $V_{\text{IT-}}$.

An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, t_{d} , starts after V_{DD} has risen above the threshold voltage $V_{\text{IT-}}$. When the supply voltage drops below the threshold voltage $V_{\text{IT-}}$, the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage $V_{\text{IT-}}$ set by an internal voltage divider.

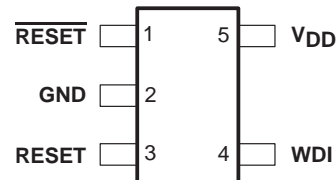
TPS3820, TPS3823, TPS3828 . . . DBV PACKAGE

(TOP VIEW)



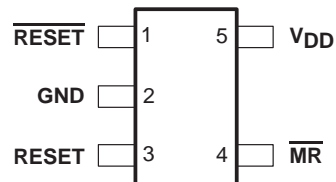
TPS3824 . . . DBV PACKAGE

(TOP VIEW)

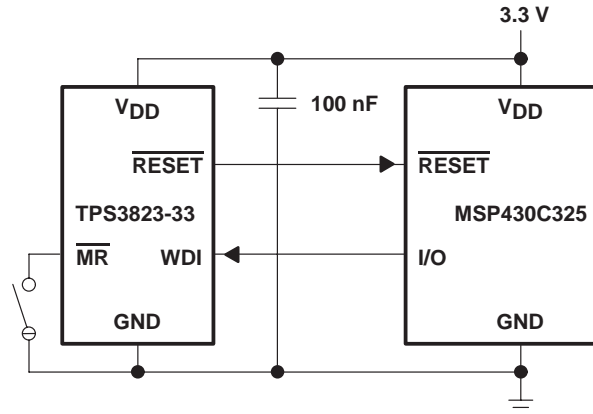


TPS3825 . . . DBV PACKAGE

(TOP VIEW)



typical application



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TPS3820-xx, TPS3823-xx, TPS3824-xx, TPS3825-xx, TPS3828-xx PROCESSOR SUPERVISORY CIRCUITS

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description (continued)

The TPS3820/3/5/8 devices incorporate a manual reset input, \overline{MR} . A low level at \overline{MR} causes \overline{RESET} to become active. The TPS3824/5 devices include a high-level output RESET. TPS3820/3/4/8 have a watchdog timer that is periodically triggered by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, t_{out} , \overline{RESET} becomes active for the time period t_d . This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 5-pin SOT23-5 package. The TPS382x devices are characterized for operation over a temperature range of -40°C to 85°C.

PACKAGE INFORMATION

DEVICE NAME	DEVICE NAME	THRESHOLD VOLTAGE	MARKING
TPS3820-25DBVT†	TPS3820-25DBVR‡§	2.25 V	
TPS3820-30DBVT†	TPS3820-30DBVR‡§	2.63 V	
TPS3820-33DBVT†	TPS3820-33DBVR‡	2.93 V	PDEI
TPS3820-50DBVT†	TPS3820-50DBVR‡	4.55 V	PDDI
TPS3823-25DBVT†	TPS3823-25DBVR‡	2.25 V	PAPI
TPS3823-30DBVT†	TPS3823-30DBVR‡	2.63 V	PAQI
TPS3823-33DBVT†	TPS3823-33DBVR‡	2.93 V	PARI
TPS3823-50DBVT†	TPS3823-50DBVR‡	4.55 V	PASI
TPS3824-25DBVT†	TPS3824-25DBVR‡	2.25 V	PATI
TPS3824-30DBVT†	TPS3824-30DBVR‡	2.63 V	PAUI
TPS3824-33DBVT†	TPS3824-33DBVR‡	2.93 V	PAVI
TPS3824-50DBVT†	TPS3824-50DBVR‡	4.55 V	PAWI
TPS3825-25DBVT†	TPS3825-25DBVR‡§	2.25 V	
TPS3825-30DBVT†	TPS3825-30DBVR‡§	2.63 V	
TPS3825-33DBVT†	TPS3825-33DBVR‡	2.93 V	PDGI
TPS3825-50DBVT†	TPS3825-50DBVR‡	4.55 V	PDFI
TPS3828-25DBVT†	TPS3828-25DBVR‡§	2.25 V	
TPS3828-30DBVT†	TPS3828-30DBVR‡§	2.63 V	
TPS3828-33DBVT†	TPS3828-33DBVR‡	2.93 V	PDII
TPS3828-50DBVT†	TPS3828-50DBVR‡	4.55 V	PDHI

† The DBVT package indicates tape and reel of 250 parts.

‡ The DBVR package indicates tape and reel of 3000 parts.

§ This device is in the Product Preview stage of development. Contact the local TI sales office for availability

FUNCTION/TRUTH TABLE

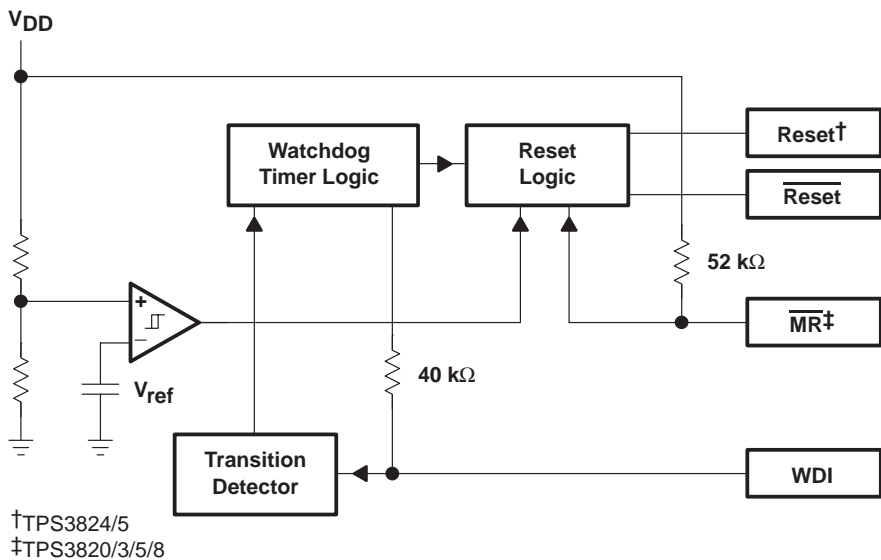
INPUTS		OUTPUTS	
\overline{MR} ‡	$V_{DD} > V_{IT}$	\overline{RESET}	RESET†
L	0	L	H
L	1	L	H
H	0	L	H
H	1	H	L

† TPS3824/5

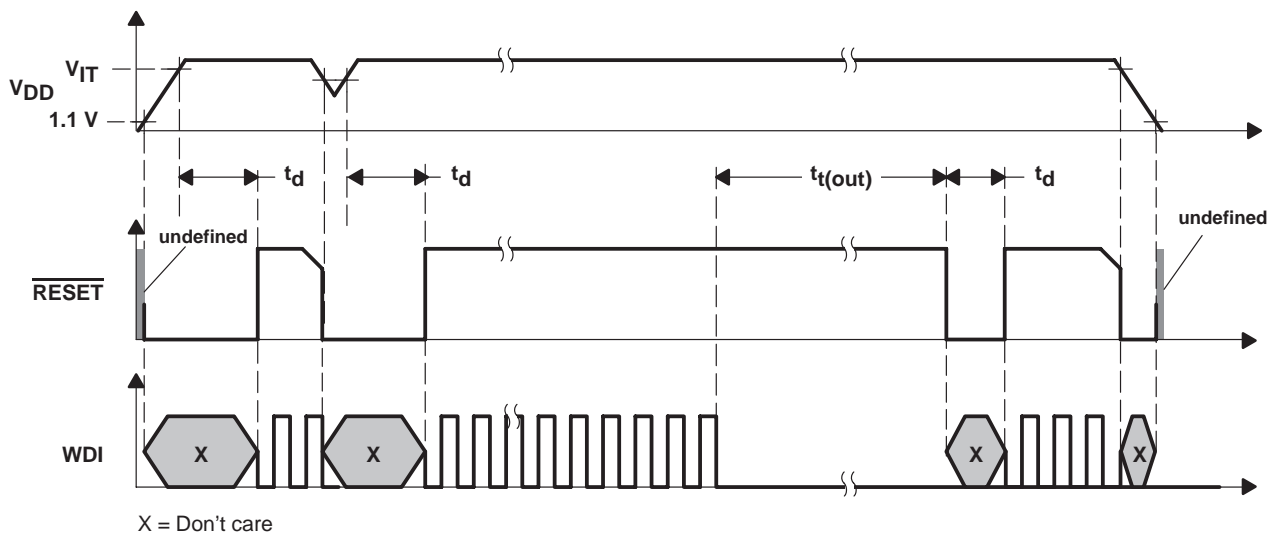
‡ TPS3820/3/5/8



functional block diagram



timing diagram



TPS3820-xx, TPS3823-xx, TPS3824-xx, TPS3825-xx, TPS3828-xx PROCESSOR SUPERVISORY CIRCUITS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	6 V
Input voltage, \overline{MR} , WDI (see Note 1)	-0.3 V to ($V_{DD} + 0.3$ V)
Maximum low output current, I_{OL}	5 mA
Maximum high output current, I_{OH}	-5 mA
Input clamp current range, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	± 10 mA
Output clamp current range, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	± 10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Soldering temperature	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.1	5.5	V
Input voltage, V_I	0	$V_{DD} + 0.3$	V
High-level input voltage at \overline{MR} and WDI , V_{IH}	$0.7 \times V_{DD}$		V
Low-level input voltage, V_{IL}		$0.3 \times V_{DD}$	V
Input transition rise and fall rate at \overline{MR} or WDI , $\Delta t/\Delta V$		100	ns/V
Operating free-air temperature range, T_A	-40	85	°C



TPS3820-xx, TPS3823-xx, TPS3824-xx, TPS3825-xx, TPS3828-xx
PROCESSOR SUPERVISORY CIRCUITS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V _{OH}	$\overline{\text{RESET}}$	TPS382x-25	0.8 × V _{DD}			V	
		TPS382x-30					
		TPS382x-33					
	TPS382x-50	V _{DD} – 1.5 V					
	RESET	TPS3824-25	V _{DD} ≥ 1.8 V, I _{OH} = –100 μA	0.8 × V _{DD}			V
		TPS3825-25					
		TPS3824-30					
		TPS3825-30					
TPS3824-33	V _{DD} ≥ 1.8 V, I _{OH} = –150 μA						
TPS3825-33							
TPS3824-50							
TPS3825-50							
V _{OL}	RESET	TPS3824-25			0.4	V	
		TPS3825-25					
		TPS3824-30					
		TPS3825-30					
	TPS3824-33	V _{DD} = V _{IT–} + 0.2 V I _{OL} = 1.2 mA					
	TPS3825-33						
	TPS3824-50	V _{DD} = V _{IT–} + 0.2 V I _{OL} = 3 mA					
	TPS3825-50						
$\overline{\text{RESET}}$	TPS382x-25	V _{DD} = V _{IT–} – 0.2 V I _{OL} = 1 mA			0.4	V	
	TPS382x-30						
	TPS382x-33						
	TPS382x-50						
Power-up reset voltage (see Note 2)		V _{DD} ≥ 1.1 V, I _{OL} = 20 μA			0.4	V	
V _{IT–}		TPS382x-25	T _A = 0°C – 85°C			V	
		TPS382x-30					
		TPS382x-33					
		TPS382x-50					
		TPS382x-25	T _A = –40°C – 85°C				V
		TPS382x-30					
		TPS382x-33					
		TPS382x-50					
V _{hys}	TPS382x-25			30		mV	
	TPS382x-30						
	TPS382x-33						
	TPS382x-50						

NOTES: 2. The lowest supply voltage at which RESET becomes active. t_r, V_{DD} ≥ 15 μs/V
3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near the supply terminals.



TPS3820-xx, TPS3823-xx, TPS3824-xx, TPS3825-xx, TPS3828-xx PROCESSOR SUPERVISORY CIRCUITS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
I _{IH(AV)}	Average high-level input current	WDI	WDI = V _{DD} , time average (dc = 88%)			120	μA
			WDI = 0.3 V, V _{DD} = 5.5 V time average (dc = 12%)			-15	
I _{IH}	High-level input current	WDI	WDI = V _{DD}			140 190	
		$\overline{\text{MR}}$	$\overline{\text{MR}} = V_{DD} \times 0.7$, V _{DD} = 5.5 V			-40 -60	
I _{IL}	Low-level input current	WDI	WDI = 0.3 V, V _{DD} = 5.5 V			140 190	
		$\overline{\text{MR}}$	$\overline{\text{MR}} = 0.3 \text{ V}$, V _{DD} = 5.5 V			-110 -160	
I _{OS}	Output short-circuit current (see Note 4)	$\overline{\text{RESET}}$	TPS382x-25	V _{DD} = V _{IT, max} + 0.2 V, V _O = 0 V			μA
			TPS382x-30				
			TPS382x-33				
			TPS382x-50				
I _{DD}	Supply current	WDI and $\overline{\text{MR}}$ unconnected, Outputs unconnected			15 25	μA	
	Internal pullup resistor at $\overline{\text{MR}}$				52	kΩ	
C _i	Input capacitance at $\overline{\text{MR}}$, WDI	V _I = 0 V to 5.5 V			5	pF	

NOTE 4: The $\overline{\text{RESET}}$ short-circuit current is the maximum pullup current when $\overline{\text{RESET}}$ is driven low by a μP bidirectional reset pin.

timing requirements at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT	
t _w	Pulse width	at V _{DD}	V _{DD} = V _{IT-} + 0.2 V, V _{DD} = V _{IT-} - 0.2 V		6	μs
		at $\overline{\text{MR}}$	V _{DD} ≥ V _{IT-} + 0.2 V, V _{IL} = 0.3 × V _{DD} , V _{IH} = 0.7 × V _{DD}		1	μs
		at WDI	V _{DD} ≥ V _{IT-} + 0.2 V, V _{IL} = 0.3 × V _{DD} , V _{IH} = 0.7 × V _{DD}		100	ns

switching characteristics at R_L = 1 MΩ, C_L = 50 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t _{tout}	Watchdog time out	TPS3820	112	200	310	ms	
		TPS3823/4/8	0.9	1.6	2.5	s	
t _d	Delay time	TPS3820	15	25	37	ms	
		TPS3823/4/5/8	120	200	300		
t _{PHL}	Propagation (delay) time, high-to-low-level output	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ delay (TPS3820/3/5/8)	V _{DD} ≥ V _{IT-} + 0.2 V, V _{IL} = 0.3 × V _{DD} , V _{IH} = 0.7 × V _{DD}			0.1	μs
		V _{DD} to $\overline{\text{RESET}}$ delay	V _{IL} = V _{IT-} - 0.2 V, V _{IH} = V _{IT-} + 0.2 V			25	
t _{PLH}	Propagation (delay) time, low-to-high-level output	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ delay (TPS3824/5)	V _{DD} ≥ V _{IT-} + 0.2 V, V _{IL} = 0.3 × V _{DD} , V _{IH} = 0.7 × V _{DD}			0.1	μs
		V _{DD} to $\overline{\text{RESET}}$ delay (TPS3824/5)	V _{IL} = V _{IT-} - 0.2 V, V _{IH} = V _{IT-} + 0.2 V			25	



TYPICAL CHARACTERISTICS

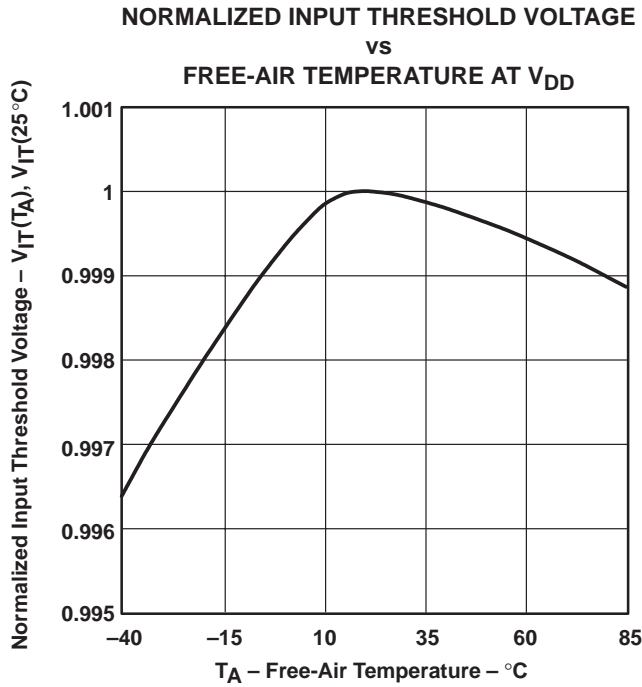


Figure 1

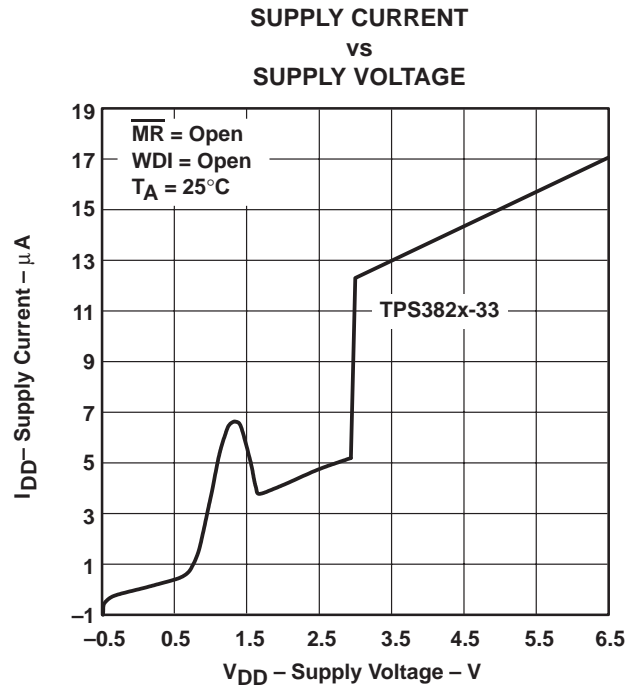


Figure 2

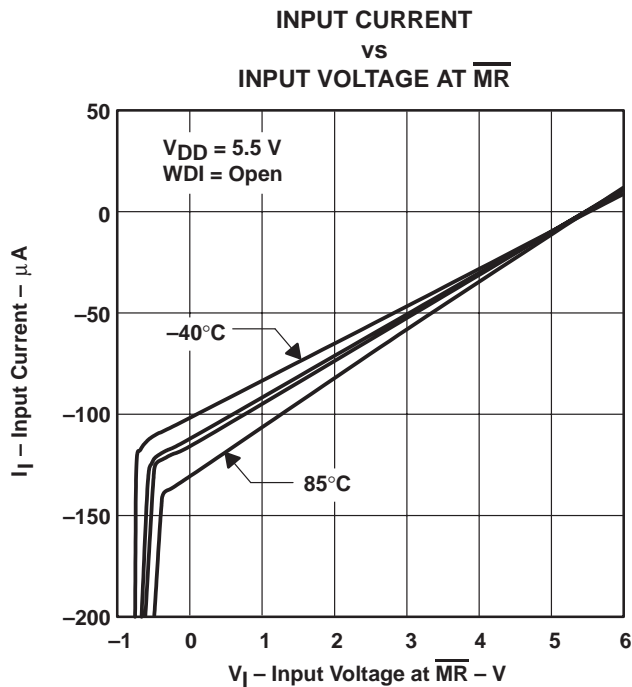


Figure 3

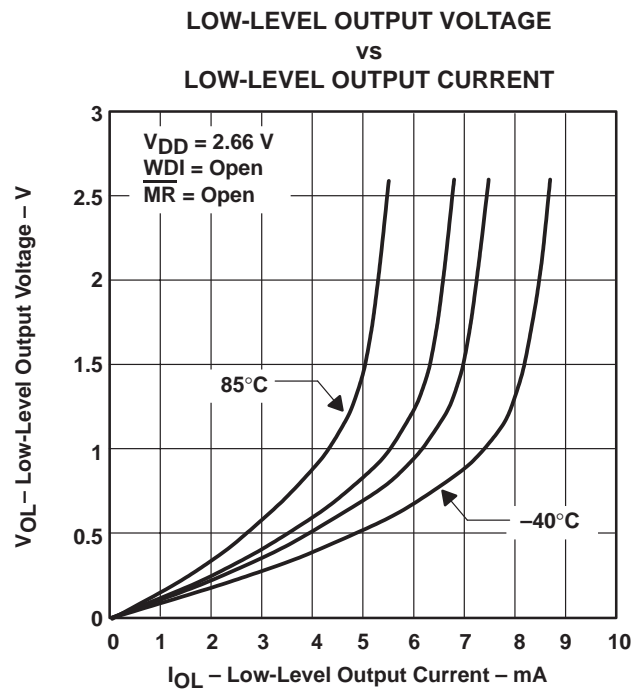


Figure 4

TYPICAL CHARACTERISTICS

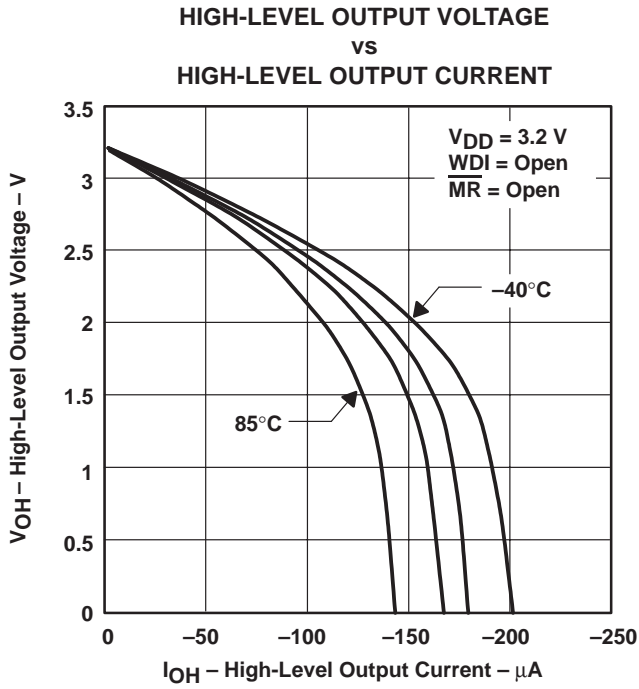


Figure 5

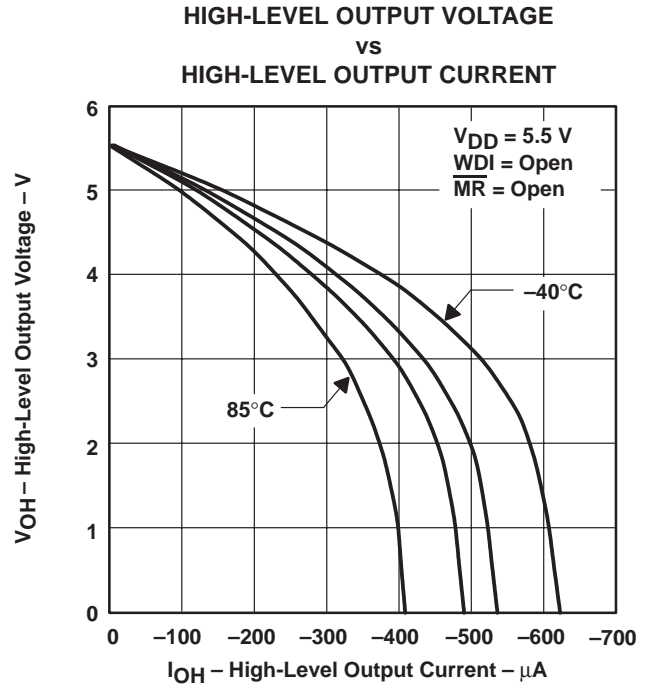


Figure 6

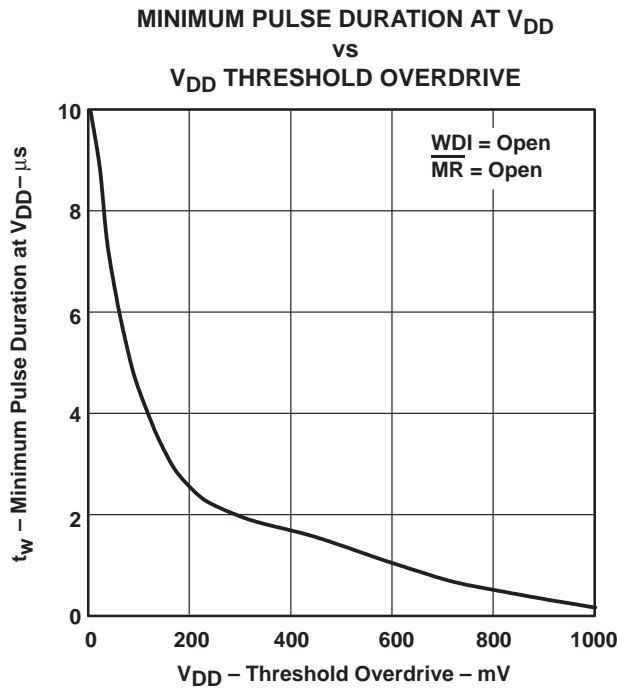


Figure 7

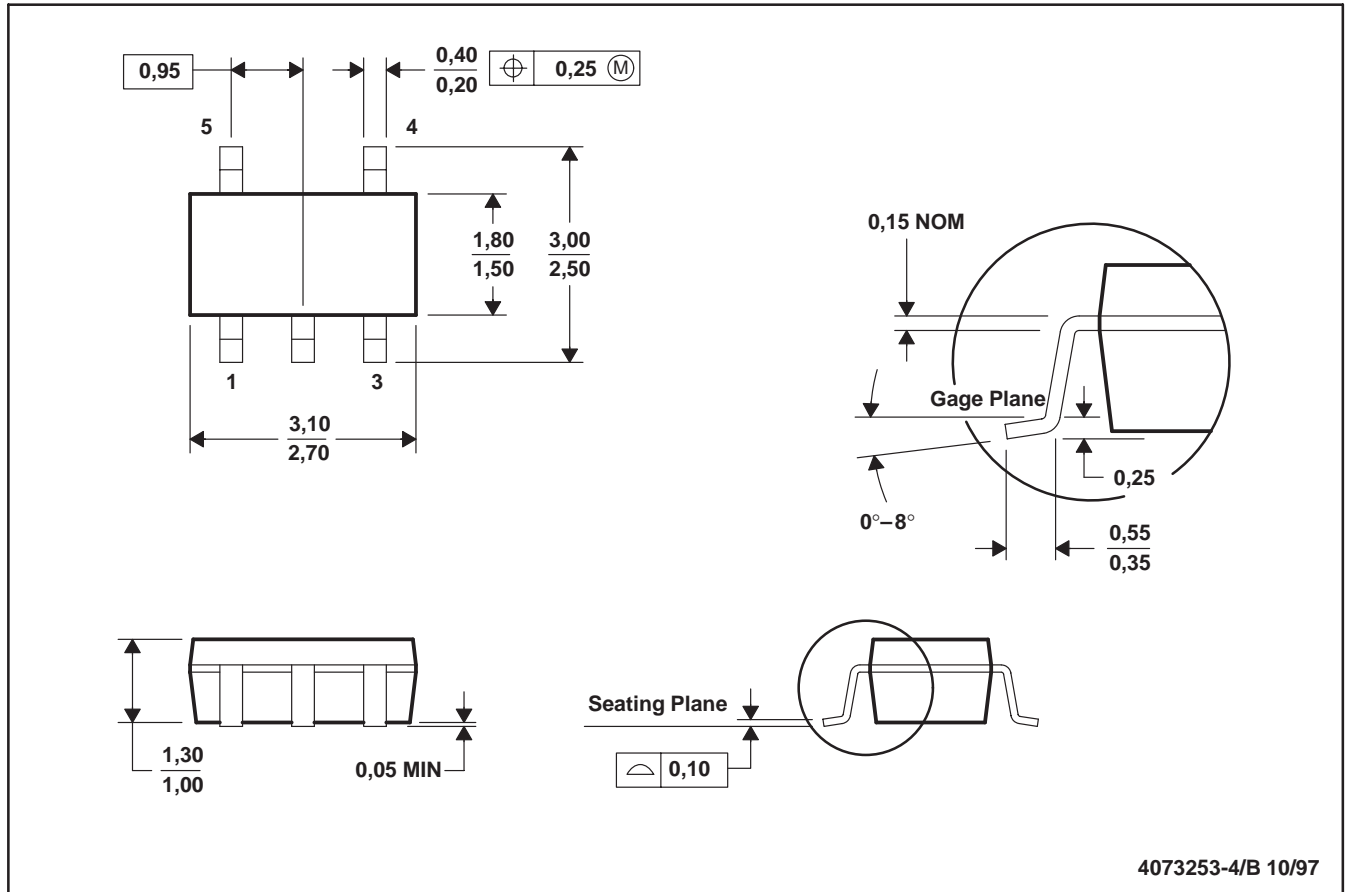
TPS3820-xx, TPS3823-xx, TPS3824-xx, TPS3825-xx, TPS3828-xx
 PROCESSOR SUPERVISORY CIRCUITS

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MECHANICAL DATA

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions include mold flash or protrusion.

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