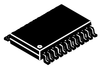


3-W STEREO CLASS-D AUDIO POWER AMPLIFIER WITH DC VOLUME CONTROL

FEATURES

- **3 W Per Channel into 3-Ω Speakers (THD+N = 10%)**
  - **< 0.045% THD at 1.5 W, 1 kHz, 3-Ω Load**
- **DC Volume Control With 2-dB Steps From –38 dB to 20 dB**
- **Filter Free Modulation Scheme Operates Without a Large and Expensive LC Output Filter**
- **Extremely Efficient Third Generation 5-V Class-D Technology**
  - **Low Supply Current, 7 mA**
  - **Low Shutdown Control, 1 µA**
  - **Low Noise Floor, –80 dBV**
  - **Maximum Efficiency into 3 Ω, 78%**
  - **Maximum Efficiency into 8 Ω, 88%**
  - **PSRR, –70 dB**
- **Integrated Depop Circuitry**
- **Operating Temperature Range, –40°C to 85°C**
- **Space-Saving, Surface Mount PowerPAD Package**

APPLICATIONS

- **LCD Projectors**
- **LCD Monitors**
- **Powered Speakers**
- **Battery Operated and Space Constrained Systems**

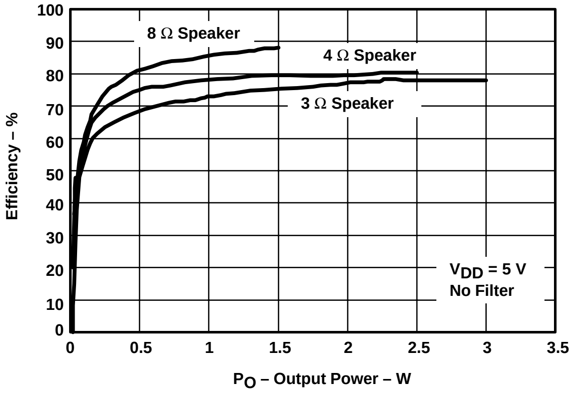
DESCRIPTION

The TPA2008D2 is a third generation 5-V class-D amplifier from Texas Instruments. Improvements to previous generation devices include: dc volume control, lower supply current, lower noise floor, higher efficiency, smaller packaging, and fewer external components. Most notably, a new filter-free class-D modulation technique allows the TPA2008D2 to directly drive the speakers, without needing a low-pass output filter consisting of two inductors and three capacitors per channel. Eliminating this output filter saves approximately 30% in system cost and 75% in PCB area.

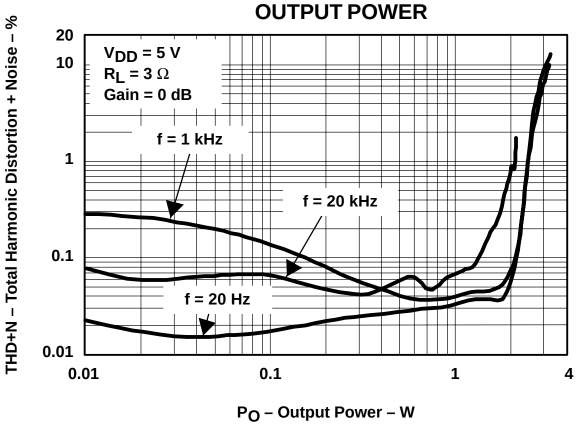
The improvements and functionality make this device ideal for LCD projectors, LCD monitors, powered speakers, and other applications that demand more battery life, reduced board space, and functionality that surpasses currently available class-D devices.

A chip-level shutdown control limits total supply current to 1 µA, making the device ideal for battery-powered applications. Protection circuitry increases device reliability: thermal and short circuit. Undervoltage shutdown saves battery power for more essential devices when battery voltage drops to low levels.

The TPA2008D2 is available in a 24-pin TSSOP PowerPAD™ package.



EFFICIENCY vs OUTPUT POWER



TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

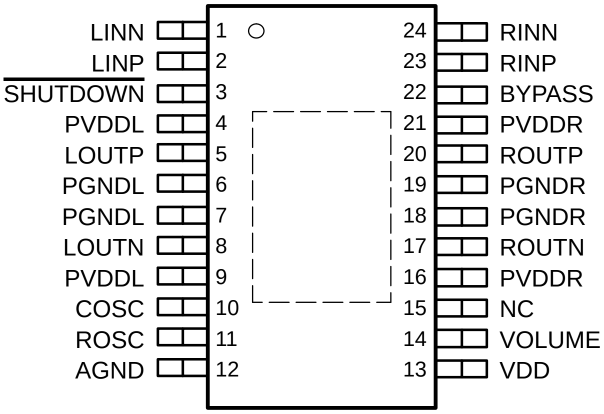
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

	TSSOP PowerPAD (PWP)†
Device	TPA2008D2PWP†
Package Designator	PWP†

† The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA2008D2PWPR).

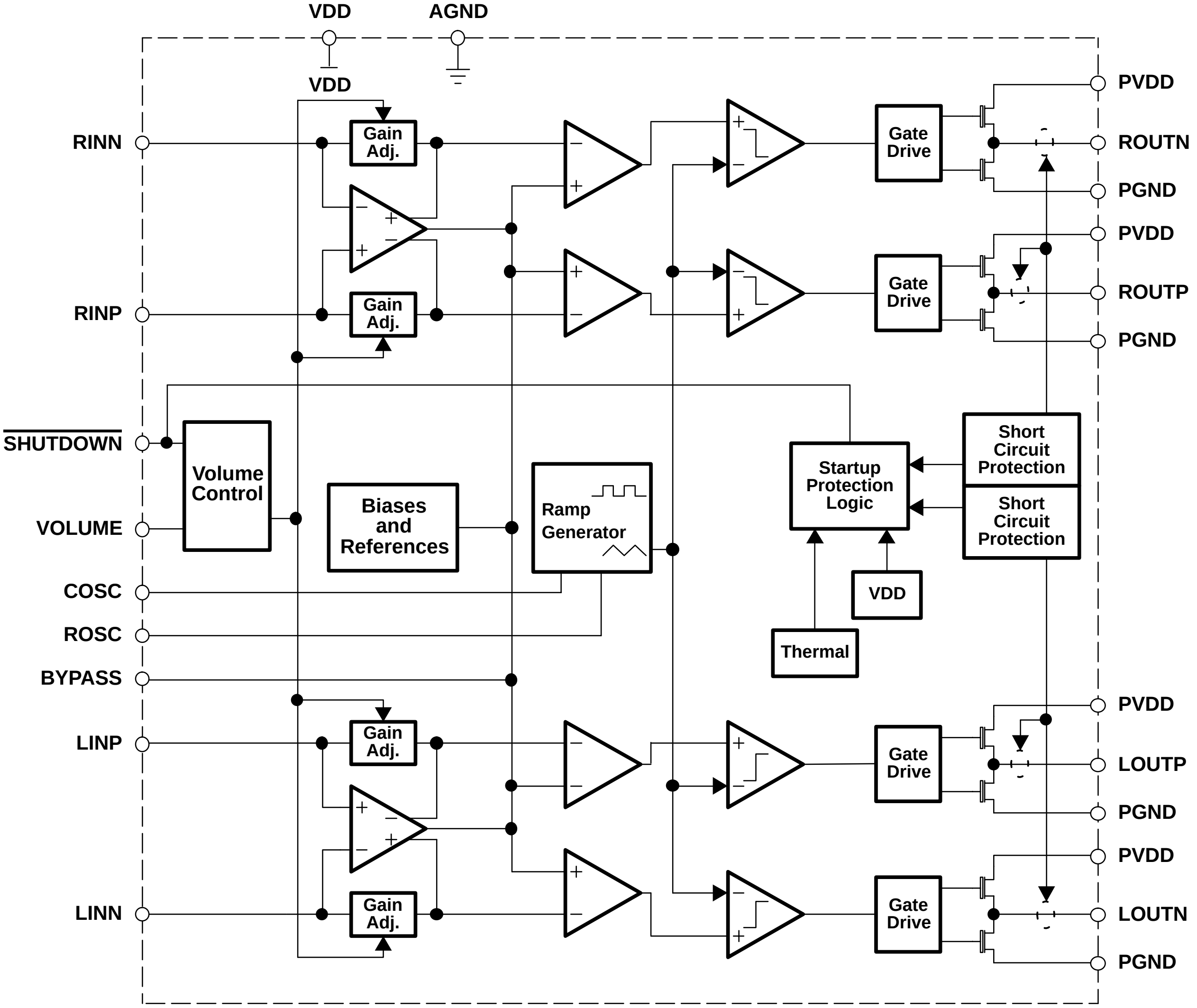
PWP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
AGND	12	–	Analog ground
BYPASS	22	I	Tap to voltage divider for internal mid-supply bias generator used for internal analog reference.
COSC	10	I	A capacitor connected to this terminal sets the oscillation frequency in conjunction with ROSC. For proper operation, connect a 220-pF capacitor from COSC to ground.
LINN	1	I	Negative differential audio input for left channel
LINP	2	I	Positive differential audio input for left channel
LOUTN	8	O	Negative audio output for left channel
LOUTP	5	O	Positive audio output for left channel
NC	15	I	No connection
PGNDL	6, 7	–	Power ground for left channel H-bridge
PGNDR	18, 19	–	Power ground for right channel H-bridge
PVDDL	4, 9	–	Power supply for left channel H-bridge
PVDDR	16, 21	–	Power supply for right channel H-bridge
RINN	24	I	Positive differential audio input for right channel
RINP	23	I	Negative differential audio input for right channel
ROSC	11	I	A resistor connected to the ROSC terminal sets the oscillation frequency in conjunction with COSC. For proper operation, connect a 120-kΩ resistor from ROSC to ground.
ROUTN	17	O	Negative output for right channel
ROUTP	20	O	Positive output for right channel
$\overline{\text{SHUTDOWN}}$	3	I	Places the amplifer in shutdown mode if a TTL logic low is placed on this terminal; normal operation if a TTL logic high is placed on this terminal.
VDD	13	–	Analog power supply
VOLUME	14	I	DC volume control for setting the gain on the internal amplifiers. The dc voltage range is 0 to VDD.
Thermal Pad	–	–	Connect to analog ground and the power grounds must be soldered down in all applications to properly secure device on the PCB.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	UNIT
Supply voltage range, V_{DD}, PV_{DD}	–0.3 V to 6 V
Input voltage range, V_I (RINN, RINP, LINN, LINP, VOLUME)	0 V to V_{DD}
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	–40°C to 85°C
Operating junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.18 W	21.8 mW/°C	1.2 W	872 mW

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
Volume terminal voltage		0	V_{DD}	V
High-level input voltage, V_{IH}	$\overline{\text{SHUTDOWN}}$	2		V
Low-level input voltage, V_{IL}	$\overline{\text{SHUTDOWN}}$		0.8	V
PWM frequency		200	300	kHz
Operating free-air temperature, T_A		–40	85	°C
Operating junction temperature, T_J			125	°C

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{DD} = PV_{DD} = 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Output offset voltage (measured differentially)	$V_I = 0$ V, $A_V = 20$ dB, $R_L = 8\ \Omega$			5	25	mV
PSRR	Power supply rejection ratio	$V_{DD} = PV_{DD} = 4.5$ V to 5.5 V			–70		dB
$\lvert I_{IH} \rvert$	High-level input current	$V_{DD} = PV_{DD} = 5.5$ V, VI = $V_{DD} = PV_{DD}$				1	µA
$\lvert I_{IL} \rvert$	Low-level input current	$V_{DD} = PV_{DD} = 5.5$ V, $V_I = 0$ V				1	µA
I_{DD}	Supply current	No filter (no load)			7	15	mA
$I_{DD(max)}$	RMS supply current at max power	$R_L = 3\ \Omega$, $P_O = 2.5$ W/channel (stereo)			1.8		A
$I_{DD(SD)}$	Supply current in shutdown mode	$\overline{\text{SHUTDOWN}} = 0$ V			50	1000	nA
$r_{ds(on)}$	Drain-source on-state resistance	$V_{DD} = 5$ V, $I_O = 500$ mA, $T_J = 25°C$	High side		450	600	mΩ
			Low side		450	600	

OPERATING CHARACTERISTICS

$T_A = 25°C$, $V_{DD} = PV_{DD} = 5$ V, $R_L = 3\ \Omega$, Gain = 0 dB (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
P_O	Output power	f = 1 kHz, $R_L = 3\ \Omega$, Stereo operation	THD+N = 1%		2.5		W
			THD+N = 10%		3		
THD+N	Total harmonic distortion plus noise	$P_O = 2.2$ W, f = 20 Hz to 20 kHz			<0.3%		
		$P_O = 1.5$ W, f = 1 kHz			0.045%		
BOM	Maximum output power bandwidth	THD = 5%			20		kHz
SNR	Signal-to-noise ratio	Maximum output at THD+N <0.5%			96		dB
	Thermal trip point				150		°C
	Thermal hysteresis				20		°C
V_n	Integrated noise floor	20 Hz to 20 kHz, inputs ac grounded	Volume = 0 dB		42		μV_{rms}
			Volume = 20 dB		85		

Table 1. DC Volume Control

Voltage on VOLUME Pin (V) (Increasing or Fixed Gain)	Voltage on VOLUME Pin (V) (Decreasing Gain)	GAIN OF AMPLIFIER (dB)
0–0.33	0.31–0	–38(1)
0.34–0.42	0.43–0.32	–37
0.43–0.52	0.54–0.44	–35
0.53–0.63	0.64–0.55	–33
0.64–0.75	0.75–0.65	–31
0.76–0.86	0.86–0.76	–29
0.87–0.97	0.97–0.87	–27
0.98–1.07	1.08–0.98	–25
1.08–1.18	1.19–1.09	–23
1.19–1.30	1.32–1.20	–21
1.31–1.41	1.42–1.33	–19
1.42–1.52	1.53–1.43	–17
1.53–1.63	1.63–1.54	–15
1.64–1.75	1.75–1.64	–13
1.76–1.85	1.84–1.76	–12
1.86–1.96	1.96–1.85	–10
1.97–2.07	2.09–1.97	–8
2.08–2.18	2.19–2.10	–6
2.19–2.30	2.33–2.20	–4
2.31–2.40	2.43–2.34	–2
2.41–2.52	2.49–2.44	0(1)
2.53–2.63	2.62–2.50	2
2.64–2.75	2.75–2.63	4
2.76–2.87	2.85–2.76	6
2.88–2.98	2.99–2.86	8
2.99–3.10	3.12–3.00	10
3.11–3.22	3.25–3.13	12
3.23–3.33	3.36–3.26	14
3.34–3.47	3.48–3.37	16
3.48–3.69	3.64–3.49	18
3.70–V_{DD}	V_{DD}–3.65	20(1)

(1) Tested in production . Remaining steps are specificed by design.

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
	Efficiency	vs Output power	1, 2
THD+N	Total harmonic distortion + noise	vs Frequency	3–5
		vs Output power	6–8
k_{SVR}	Supply ripple rejection ratio	vs Frequency	9
	Crosstalk	vs Frequency	10
CMRR	Common-mode rejection ratio	vs Frequency	11
R_i	Input resistance	vs Gain setting	12

TYPICAL CHARACTERISTICS

**EFFICIENCY
vs
OUTPUT POWER**

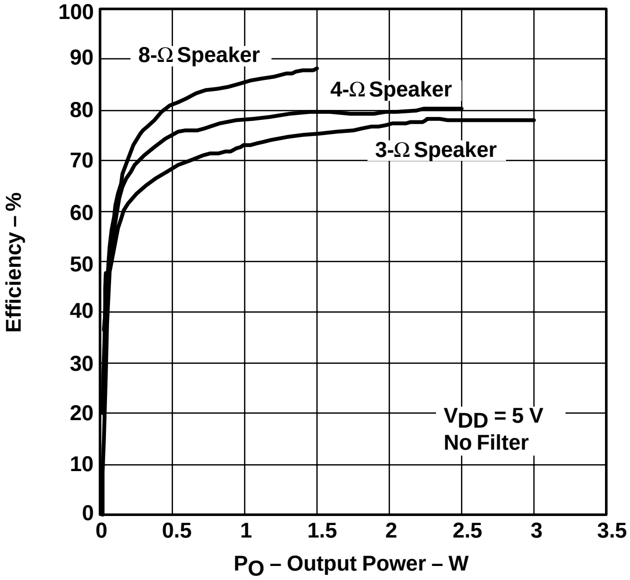


Figure 1

**EFFICIENCY
vs
OUTPUT POWER**

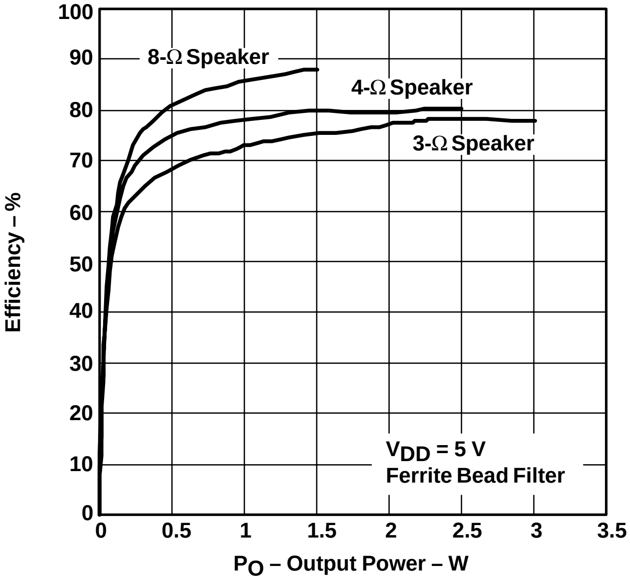


Figure 2

**TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY**

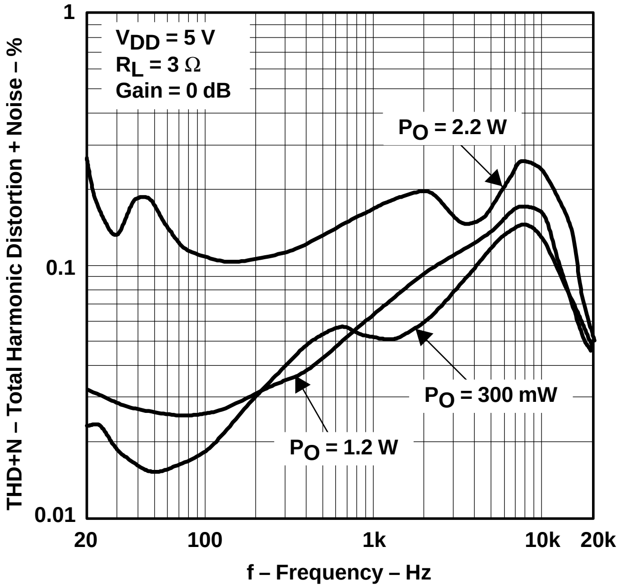


Figure 3

**TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY**

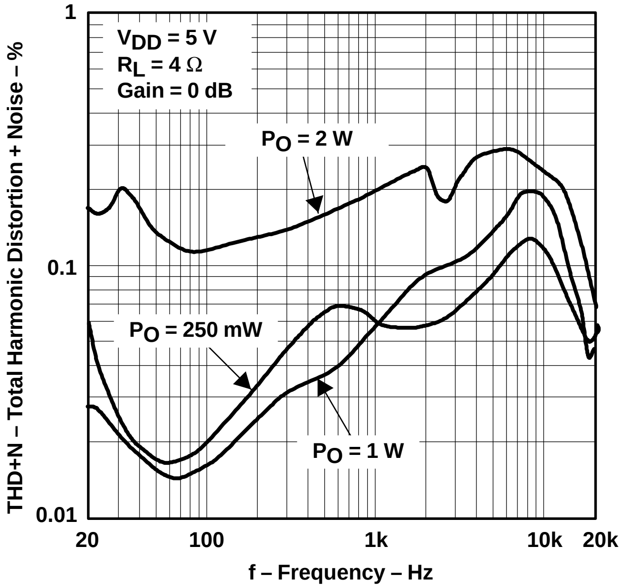


Figure 4

TYPICAL CHARACTERISTICS

**TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY**

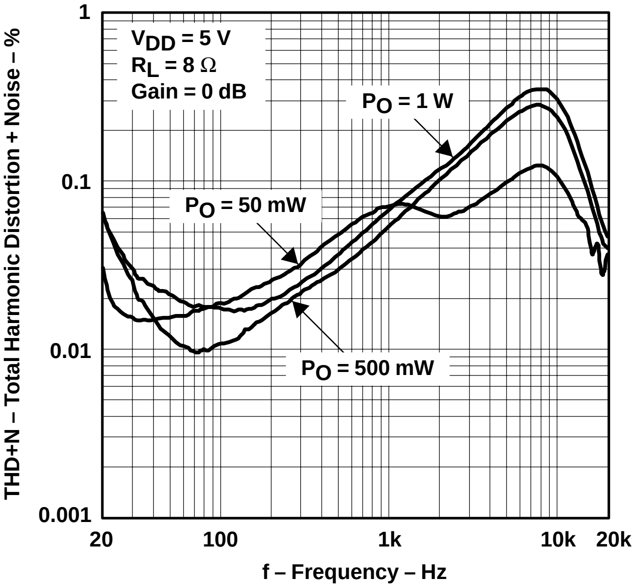


Figure 5

**TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER**

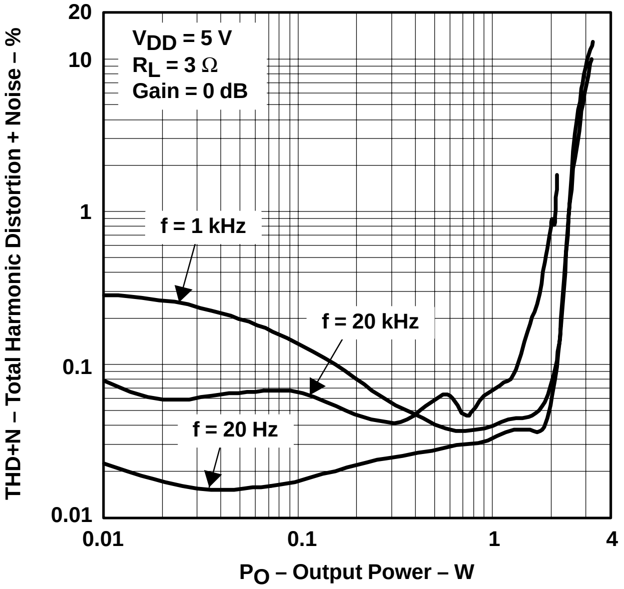


Figure 6

**TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER**

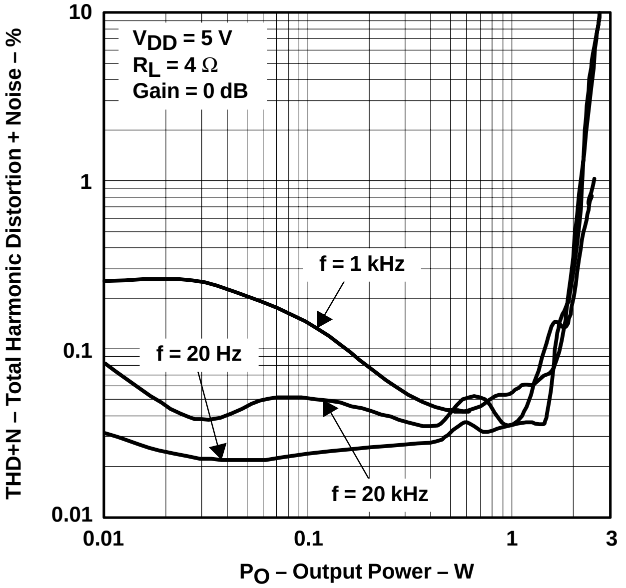


Figure 7

**TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER**

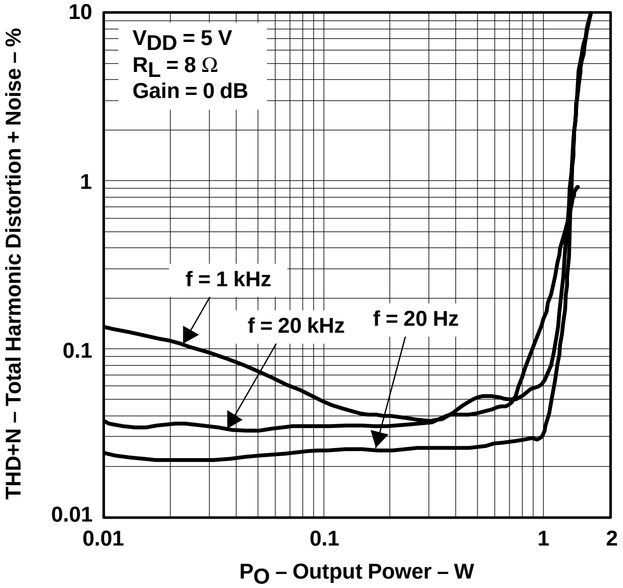


Figure 8

TYPICAL CHARACTERISTICS

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

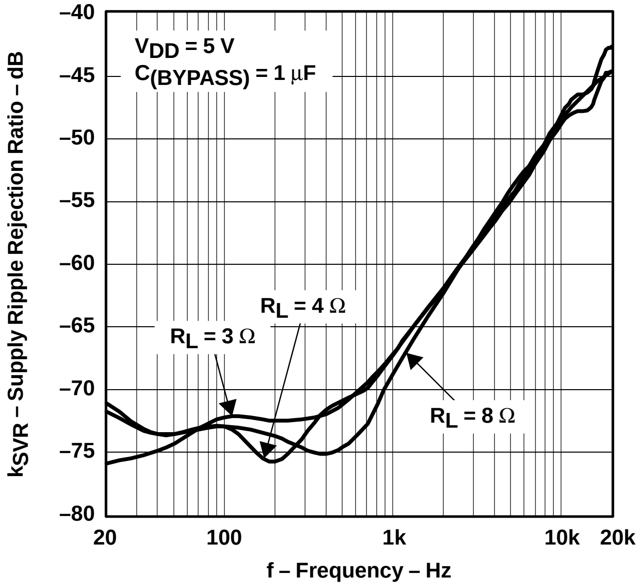


Figure 9

CROSSTALK
vs
FREQUENCY

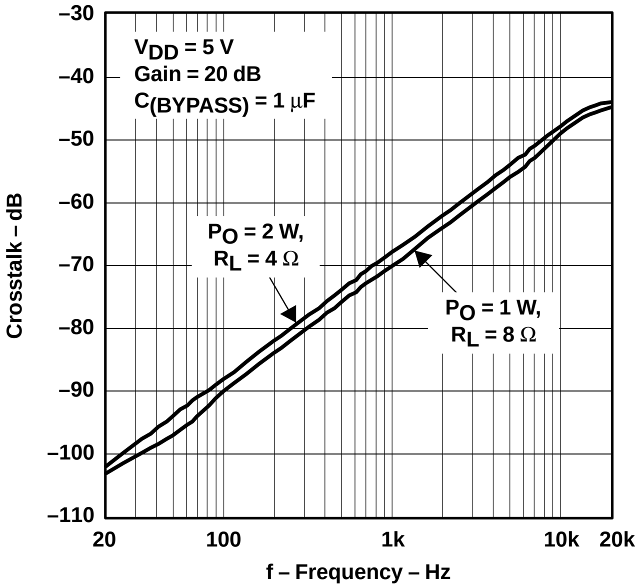


Figure 10

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

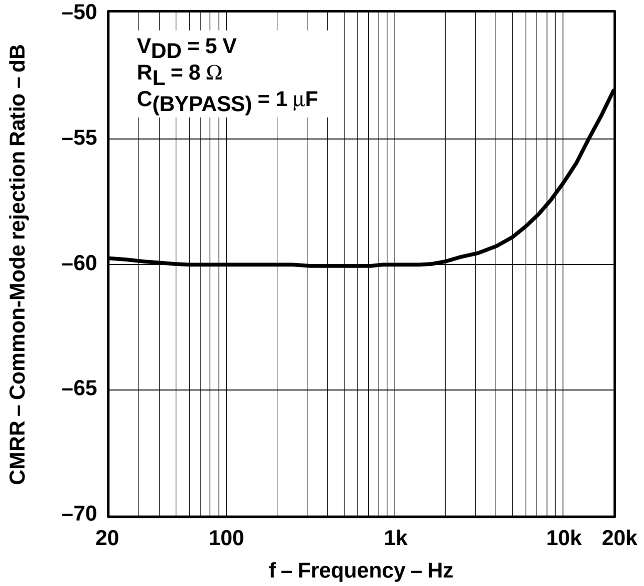


Figure 11

INPUT RESISTANCE
vs
GAIN SETTING

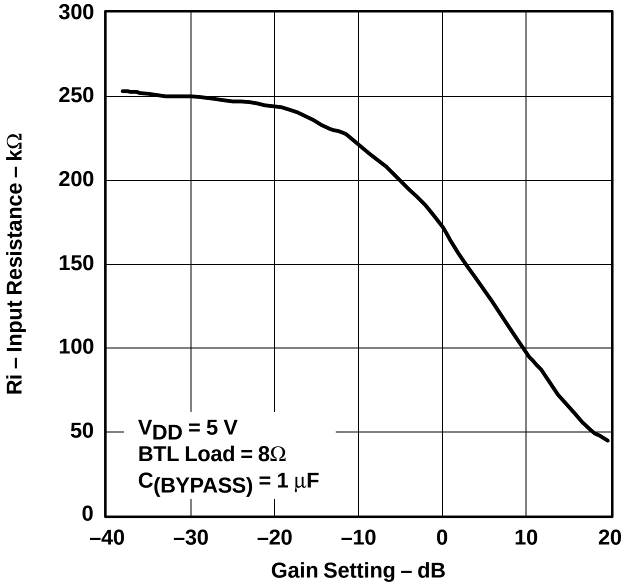


Figure 12

APPLICATION INFORMATION

APPLICATION CIRCUIT

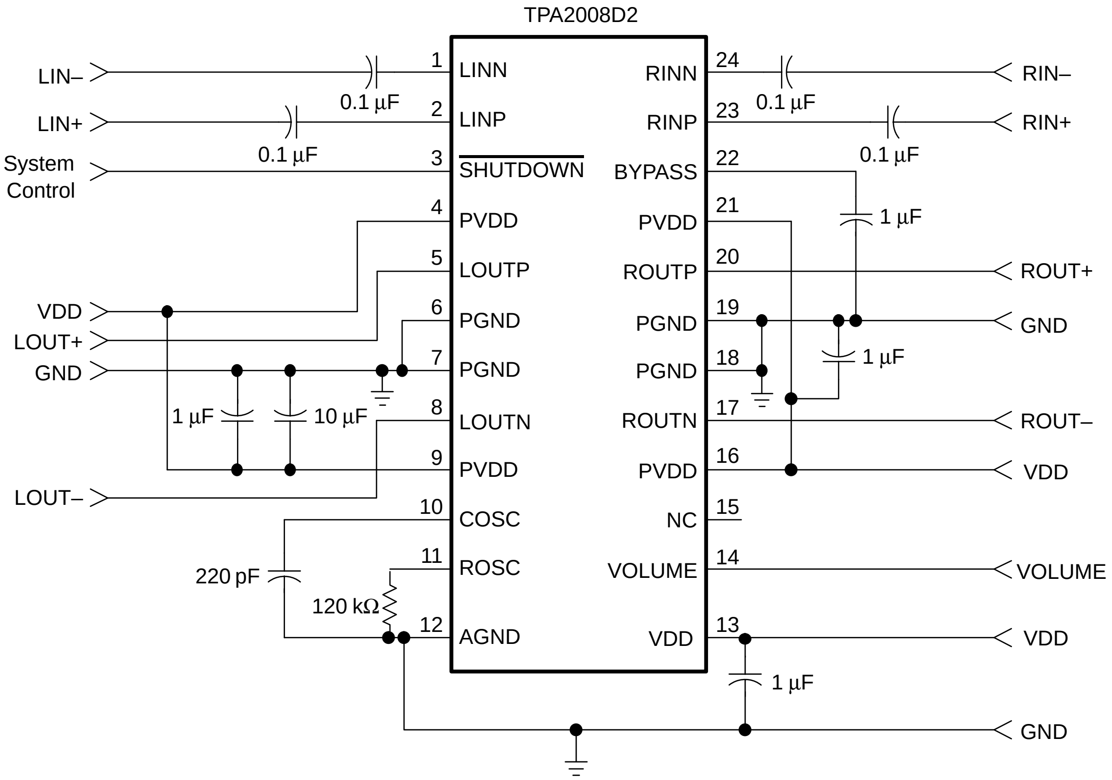


Figure 13. TPA2008D2 in a Stereo Configuration With Differential Inputs

APPLICATION INFORMATION

TRADITIONAL CLASS-D MODULATION SCHEME

The traditional class-D modulation scheme, which is used in the TPA032D0x family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage, V_{CC}. Therefore, the differential prefiltered output varies between positive and negative V_{CC}, where filtered 50% duty cycle yields 0 V across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 14. Note that even at an average of 0 V across the load (50% duty cycle), the current to the load is high, resulting in a high I^2R loss, thus causing a high supply current.

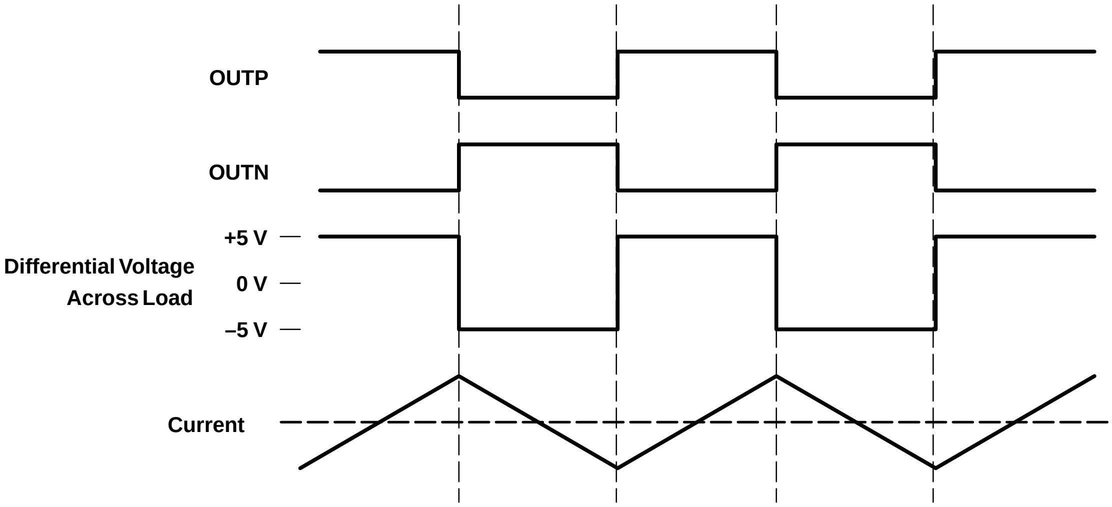


Figure 14. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms Into an Inductive Load With No Input

TPA2008D2 MODULATION SCHEME

The TPA2008D2 uses a modulation scheme that still has each output switching from 0 to the supply voltage. However, OUTP and OUTN are now in phase with each other with no input. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, greatly reducing the switching current, which reduces any I^2R losses in the load.

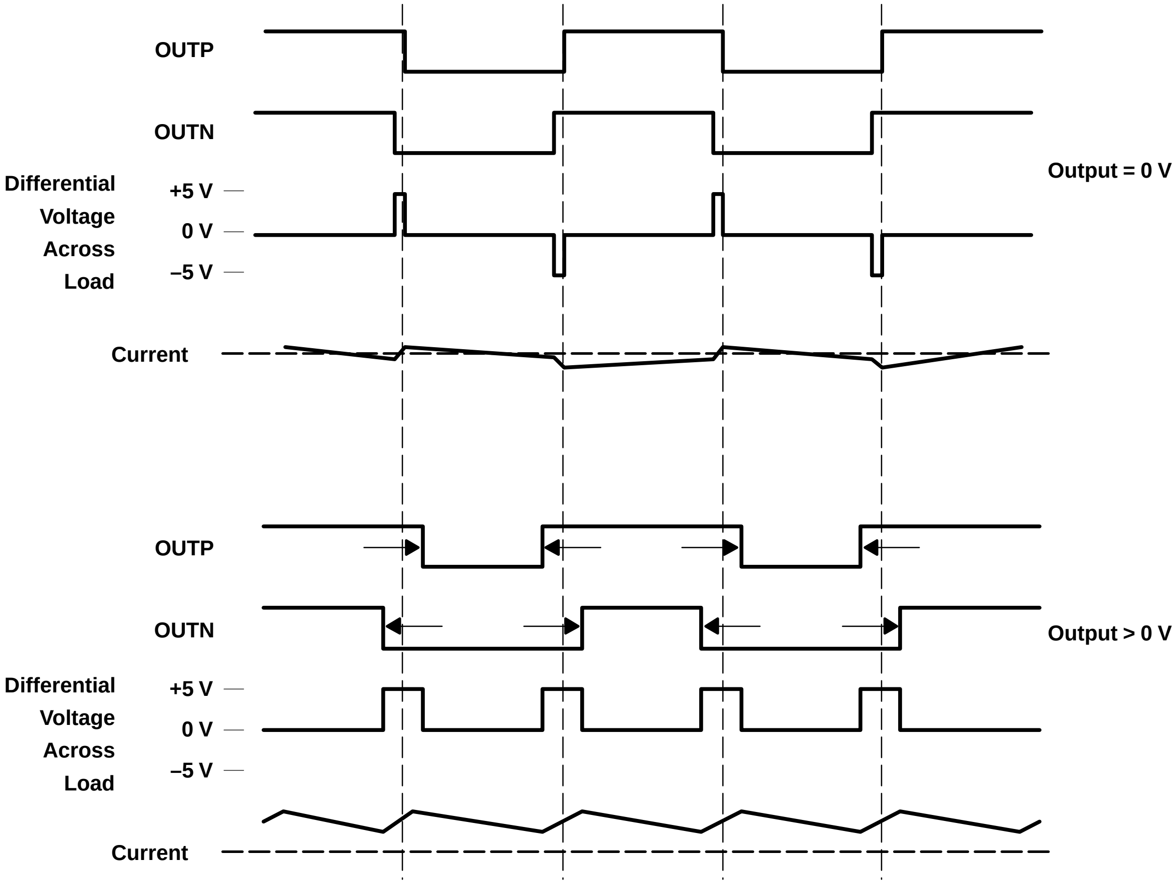


Figure 15. The TPA2008D2 Output Voltage and Current Waveforms Into an Inductive Load

EFFICIENCY: LC FILTER REQUIRED WITH THE TRADITIONAL CLASS-D MODULATION SCHEME

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{DD}$, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA2008D2 modulation scheme has very little loss in the load without a filter because the pulses are very short and the change in voltage is V_{DD} instead of $2 \times V_{DD}$. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance than the speaker, which results in less power dissipation, therefore increasing efficiency.

EFFECTS OF APPLYING A SQUARE WAVE INTO A SPEAKER

Audio specialists have advised for years not to apply a square wave to speakers. If the amplitude of the waveform is high enough and the frequency of the square wave is within the bandwidth of the speaker, the square wave could cause the voice coil to jump out of the air gap and/or scar the voice coil. A 250-kHz switching frequency, however, does not significantly move the voice coil, as the cone movement is proportional to $1/f^2$ for frequencies beyond the audio band.

Damage may occur if the voice coil cannot handle the additional heat generated from the high-frequency switching current. The amount of power dissipated in the speaker may be estimated by first considering the overall efficiency of the system. If the on-resistance ($r_{ds(on)}$) of the output transistors is considered to cause the dominant loss in the system, then the maximum theoretical efficiency for the TPA2008D2 with an 4-Ω load is as follows:

$$\text{Efficiency (theoretical, \%)} = R_L / \left(R_L + r_{ds(on)}\right) \times 100\% = 4/(4 + 0.45) \times 100\% = 89.9\% \tag{1}$$

The maximum measured output power is approximately 2.5 W with a 5-V power supply. The total theoretical power supplied ($P_{(total)}$) for this worst-case condition would therefore be as follows:

$$P_{(total)} = P_O/\text{Efficiency} = 2.5\text{ W} / 0.899 = 2.781\text{ W} \tag{2}$$

The efficiency measured in the lab using a 4-Ω speaker was 80%. The power not accounted for as dissipated across the $r_{ds(on)}$ may be calculated by simply subtracting the theoretical power from the measured power:

$$\text{Other losses} = P_{(total)}(\text{measured}) - P_{(total)}(\text{theoretical}) = 3.025 - 2.781 = 0.244\text{ W} \tag{3}$$

The quiescent supply current at 5 V is measured to be 7 mA. It can be assumed that the quiescent current encapsulates all remaining losses in the device, i.e., biasing and switching losses. It may be assumed that any remaining power is dissipated in the speaker and is calculated as follows:

$$P_{(dis)} = 0.244\text{ W} - (5\text{ V} \times 7\text{ mA}) = 0.209\text{ W} \tag{4}$$

Note that these calculations are for the worst-case condition of 2.5 W delivered to the speaker. Since the 0.209 W is only 7.4% of the power delivered to the speaker, it may be concluded that the amount of power actually dissipated in the speaker is relatively insignificant. Furthermore, this power dissipated is well within the specifications of most loudspeaker drivers in a system, as the power rating is typically selected to handle the power generated from a clipping waveform.

WHEN TO USE AN OUTPUT FILTER

Design the TPA2008D2 without the filter if the traces from amplifier to speaker are short (< 1 inch). Powered speakers, where the speaker is in the same enclosure as the amplifier, is a typical application for class-D without a filter.

Many applications require a ferrite bead filter. The ferrite filter reduces EMI around 1 MHz and higher (FCC and CE only test radiated emissions greater than 30 MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

Use an LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and/or there are long wires from the amplifier to the speaker.

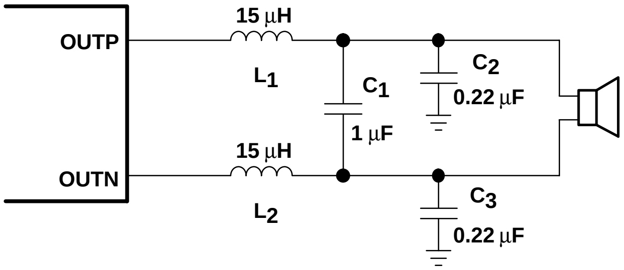


Figure 16. Typical LC Output Filter, Cutoff Frequency of 41 kHz, Speaker Impedance = 4 Ω

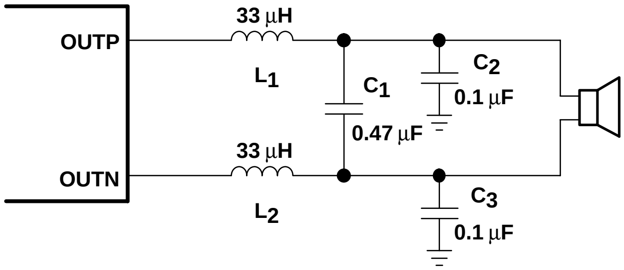


Figure 17. Typical LC Output Filter, Cutoff Frequency of 41 kHz, Speaker Impedance = 8 Ω

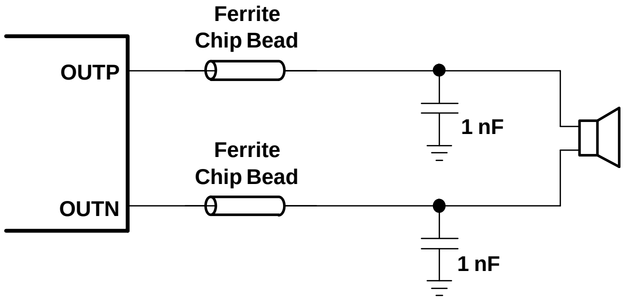


Figure 18. Typical Ferrite Chip Bead Filter (Chip bead example: Fair-Rite 2512067007Y3)

VOLUME CONTROL OPERATION

The VOLUME pin controls the volume of the TPA2008D2. It is controlled with a dc voltage, which should not exceed V_{DD}. Table 1 lists the gain voltage on the VOLUME pin.

The trip point, where the gain actually changes, is different depending on whether the voltage on the VOLUME terminal is increasing or decreasing as a result of hysteresis about each trip point. The hysteresis ensures that the gain control is monotonic and does not oscillate from one gain step to another. A pictorial representation of the volume control can be found in Figure 19. The graph focuses on three gain steps with the trip points defined in the first and second columns of Table 1. The dotted lines represent the hysteresis about each gain step.

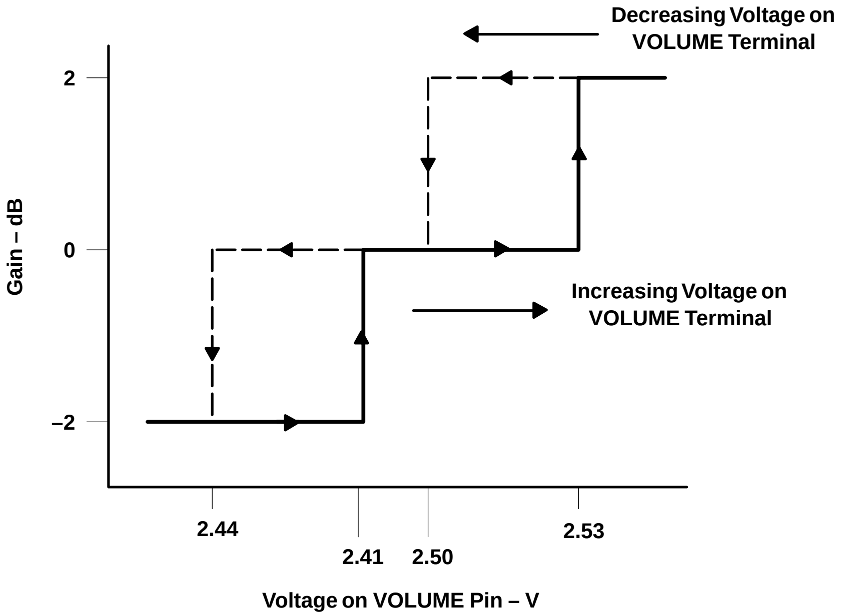


Figure 19. DC Volume Control Operation

SELECTION OF COSC AND ROSC

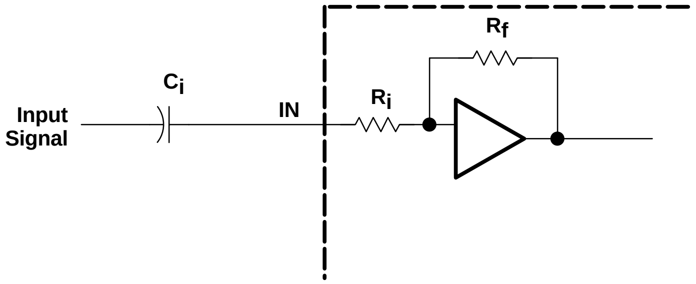
The switching frequency is determined using the values of the components connected to ROSC (pin 11) and COSC (pin 10) and may be calculated with the following equation:

$$f_{OSC} = 6.6 / (R_{OSC} \times C_{OSC}) \tag{5}$$

The frequency may be varied from 200 kHz to 300 kHz by adjusting the values chosen for R_{OSC} and C_{OSC}. The recommended values are C_{OSC} = 220 pF, R_{OSC} = 120 kΩ for a switching frequency of 250 kHz.

INPUT RESISTANCE

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over five times that value. As a result, if a single capacitor is used in the input high-pass filter, the –3 dB or cutoff frequency also changes by over five times.



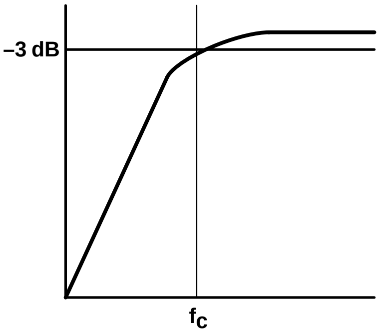
The –3-dB frequency can be calculated using equation 6. See Figure 12. Note that due to process variation, the input resistance, R_i, can change by up to 20%.

$$f_{-3\text{ dB}} = \frac{1}{2\pi C_i R_i} \tag{6}$$

INPUT CAPACITOR, C_I

In a typical application, an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input resistance of the amplifier (R_i) form a high-pass filter with the corner frequency determined in equation 7.

$$f_c = \frac{1}{2\pi R_i C_i} \tag{7}$$



The value of C_i is important, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_i is 50 kΩ and the specification calls for a flat bass response down to 30 Hz. Equation 5 is reconfigured as equation 8.

$$C_i = \frac{1}{2\pi R_i f_c} \tag{8}$$

In this example, C_i is 0.1 µF, so one would likely choose a value in the range of 0.1 µF to 1 µF. Figure 12 can be used to determine the input impedance for a given gain and can serve to aid in the calculation of C_i.

A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

C_i must be 10 times smaller than the bypass capacitor to reduce clicking and popping noise from power on/off and entering and leaving shutdown. After sizing C_i for a given cutoff frequency, size the bypass capacitor to 10 times that of the input capacitor.

$$C_i \le C_{BYP} / 10 \tag{9}$$

POWER SUPPLY DECOUPLING, C_S

The TPA2008D2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. Optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device V_{DD} terminal works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

MIDRAIL BYPASS CAPACITOR, C_{BYP}

The midrail bypass capacitor (C_{BYP}) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor (C_{BYP}) values of 0.47-µF to 1-µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

Increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering and leaving shutdown. To have minimal pop, C_{BYP} should be 10 times larger than C_i.

$$C_{BYP} \ge 10 \times C_i \tag{10}$$

DIFFERENTIAL INPUT

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA2008D2 EVM with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA2008D2 with a single-ended source, ac ground either input through a capacitor and apply the audio signal to the remaining input. In a single-ended input application, the unused input should be ac-grounded at the audio source instead of at the device input for best noise performance.

SHUTDOWN MODES

The TPA2008D2 employs a shutdown mode of operation designed to reduce supply current (I_{DD}) to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, $I_{DD(SD)} = 1$ µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because the amplifier state would be unpredictable.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

SHORT-CIRCUIT PROTECTION

The TPA2008D2 has short circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts, output-to-GND shorts, and output-to-V_{DD} shorts. When a short-circuit is detected on the outputs, the part immediately goes into shutdown. This is a latched fault and must be reset by cycling the voltage on the $\overline{\text{SHUTDOWN}}$ pin to a logic low and back to the logic high, or by cycling the power off and then back on. This clears the short-circuit flag and allows for normal operation if the short was removed. If the short was not removed, the protection circuitry activates again.

LOW-SUPPLY VOLTAGE DETECTION

The TPA2008D2 incorporates circuitry designed to detect when the supply voltage is low. When the supply voltage reaches 1.8 V or below, the TPA2008D2 goes into a state of shutdown. The current consumption drops from millamperes to microamperes, leaving the remaining battery power for more essential devices such as microprocessors. When the supply voltage level returns to normal, the device comes out of its shutdown state and starts to draw current again. Note that even though the device is drawing several milliamperes of current, it is not operationally functional until $V_{DD} \geq 4.5$ V.

THERMAL PROTECTION

Thermal protection on the TPA2008D2 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 20°C. The device begins normal operation at this point with no external system interaction.

THERMAL CONSIDERATIONS: OUTPUT POWER AND MAXIMUM AMBIENT TEMPERATURE

To calculate the maximum ambient temperature, the following equation may be used:

$$T_{Amax} = T_J - \Theta_{JA} P_{Dissipated} \tag{11}$$

where: $T_J = 125°C$

$\Theta_{JA} = 45.87°C/W$

(The derating factor for the 24-pin PWP package is given in the dissipation rating table.)

To estimate the power dissipation, the following equation may be used:

$$P_{Dissipated} = P_{O(average)} \times ((1 / \text{Efficiency}) - 1) \tag{12}$$

Efficiency = ~85% for an 8-Ω load

= ~80% for a 4-Ω load

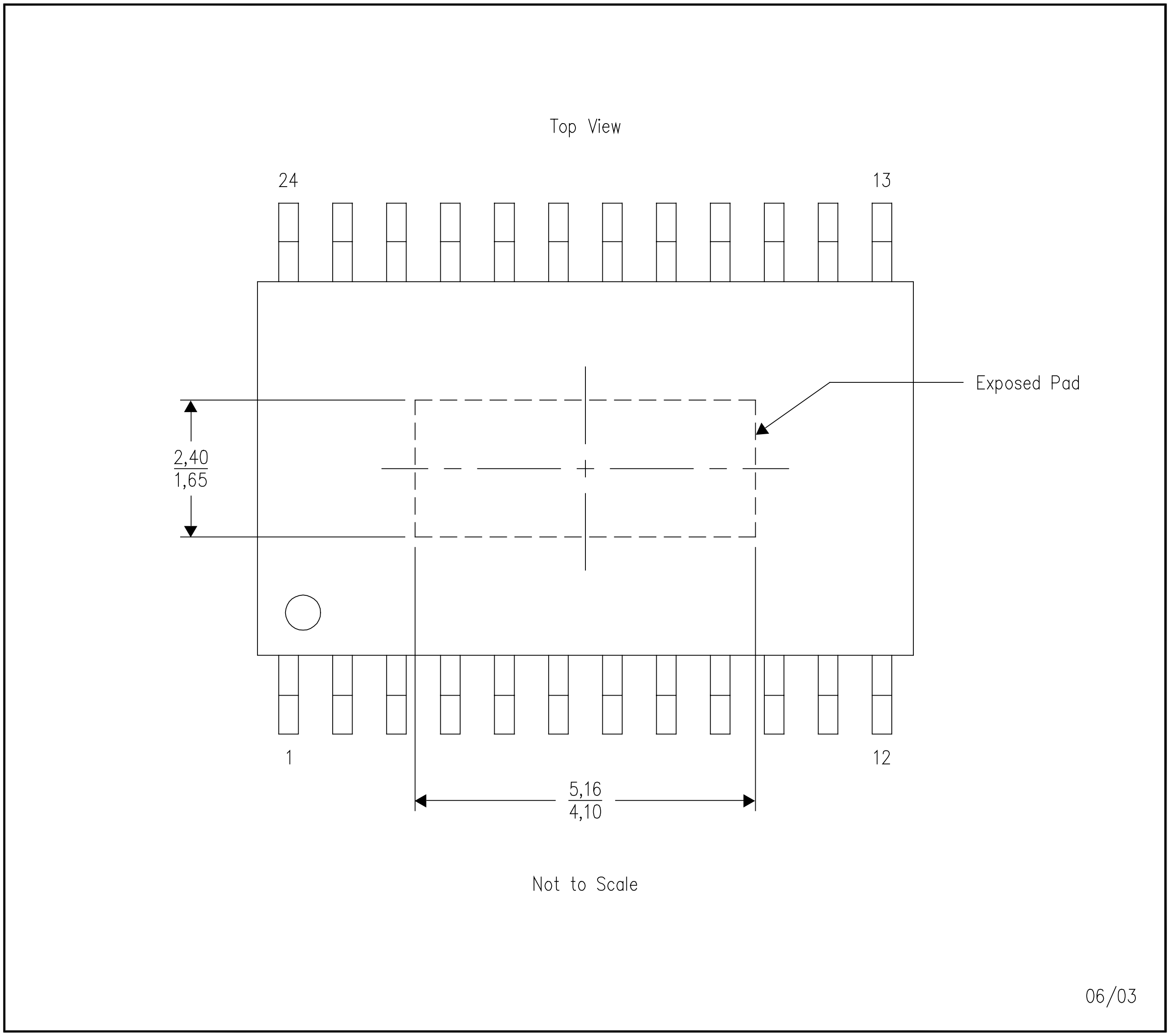
= ~75% for a 3-Ω load

Example. What is the maximum ambient temperature for an application that requires the TPA2008D2 to drive 2 W into a 4-Ω speaker (stereo)?

$P_{Dissipated} = 4\text{ W} \times ((1 / 0.8) - 1) = 1\text{ W}$ ($P_O = 2\text{ W} \times 2$)

$T_{Amax} = 125°C - (45.87°C/W \times 1\text{ W}) = 79.13°C$

PWP (R-PDSO-G24) **PowerPAD™ PLASTIC SMALL-OUTLINE**



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. For additional information on the PowerPAD™ package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, ***PowerPAD Thermally Enhanced Package***, Texas Instruments Literature No. SLMA002 and Application Brief, ***PowerPAD Made Easy***, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

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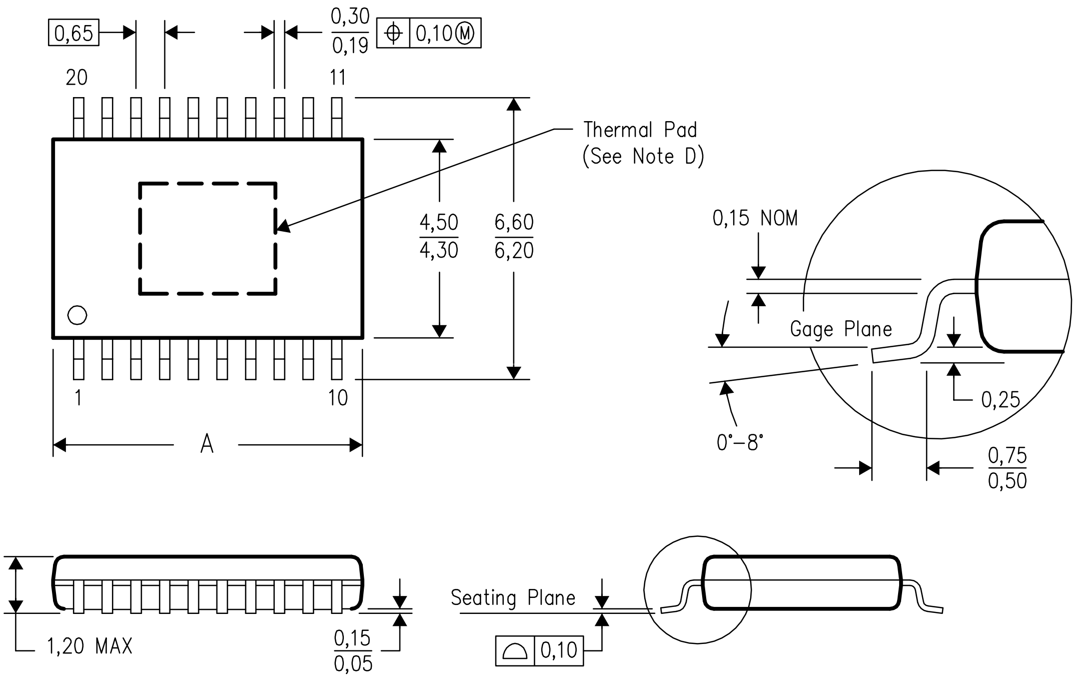
PWP (R-PDSO-G**) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

20 PIN SHOWN



PINS ** DIM	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/G 08/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. Falls within JEDEC MO–153

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