DATA SHEET

TJA1041
High speed CAN transceiver

Preliminary specification 2001 Dec 18

File under Integrated Circuits, IC18

Philips Semiconductors

FEATURES

Optimized for in-vehicle high speed communication

- Fully compatible with the ISO 11898 standard
- High speed (up to 1 Mbaud)
- Very low ElectroMagnetic Emission (EME)
- Differential receiver with high common-mode range for ElectroMagnetic Immunity (EMI)
- Passive behaviour in unpowered state
- Auto I/O-level adaptation to host controller supply voltage
- Voltage source for stabilizing the recessive bus level if split termination is used (further improvement of EME)
- Listen-only mode
- At least 110 nodes can be connected.

Low-power management

- Very low-current sleep and standby mode with local and remote wake-up
- Wake-up source recognition.

Diagnosis (detection and signalling)

- Short-circuits of the bus lines
- Over-temperature
- Transmit data (TXD) dominant time-out
- Receive data (RXD) recessive clamping
- RXD to TXD short-circuit
- Bus dominant time-out
- Cold start (first battery connection).

Protections

- TXD dominant time-out function
- RXD recessive clamping function
- TXD to RXD short-circuit handler
- Bus pins and pin V_{BAT} protected against transients in an automotive environment
- Bus pins and pin SPLIT short-circuit proof to battery and ground
- Thermally protected
- Undervoltage detection on pins V_{CC}, $V_{I/O}$ and V_{BAT}.

GENERAL DESCRIPTION

The TJA1041 is the interface between the protocol controller and the physical bus of a CAN network. It is primarily intended for high speed applications, up to 1 Mbaud, in passenger cars. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller and is fully compatible to the ISO 11898 standard. Besides an excellent EMC performance and passive behaviour in unpowered state, the TJA1041 provides furthermore:

- Low-power management, supporting local and remote wake-up with wake-up source recognition
- Several diagnosis functions including short-circuits of the bus lines and first battery connection
- Listen-only mode
- Auto adaptation of the I/O levels to the supply voltage of the microcontroller.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TJA1041T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{BAT}	supply voltage on pin V_{BAT}		5	27	V
V_{CC}	supply voltage on pin V_{CC}		4.75	5.25	V
$V_{I/O}$	supply voltage on pin $V_{I/O}$		2.8	5.25	V
I_{BAT}	supply current on pin V_{BAT}	V_{BAT} = 12 V	10	30	µA
V_{CANH}	DC voltage on pin CANH	0 < V_{CC} < 5.25 V; no time limit	–27	+40	V
V_{CANL}	DC voltage on pin CANL	0 < V_{CC} < 5.25 V; no time limit	–27	+40	V
V_{SPLIT}	DC voltage on pin SPLIT	0 < V_{CC} < 5.25 V; no time limit	–27	+40	V
T_{vj}	virtual junction temperature		–40	+150	°C
$V_{esd(HBM)}$	electrostatic discharge voltage on all pins	Human Body Model (HBM)	–4	+4	kV
$t_{PD(TXD-RXD)}$	propagation delay TXD to RXD	V_{STB} = 0 V	–	255	ns

BLOCK DIAGRAM

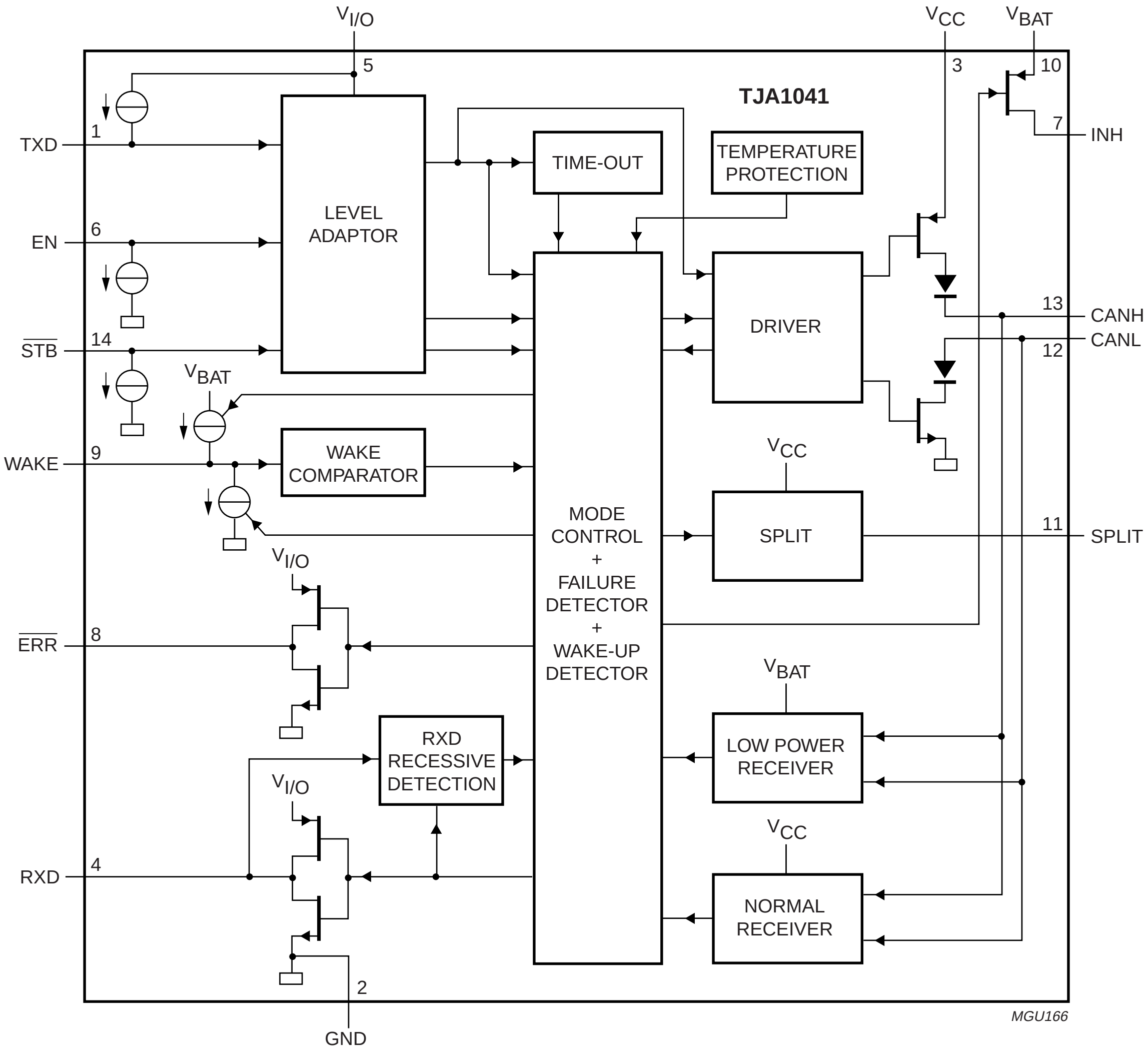


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TXD	1	transmit data input
GND	2	ground supply
V_{CC}	3	supply voltage
RXD	4	receive data output; reads out data from the bus lines
$V_{I/O}$	5	supply voltage for I/O-level adaptation
EN	6	enable control input
INH	7	inhibit output for switching external voltage regulator
$\overline{\text{ERR}}$	8	error and power-on indication output (active LOW)
WAKE	9	local wake-up input
V_{BAT}	10	battery supply voltage
SPLIT	11	common-mode stabilization output
CANL	12	LOW-level CAN bus line
CANH	13	HIGH-level CAN bus line
$\overline{\text{STB}}$	14	standby control input (active LOW)

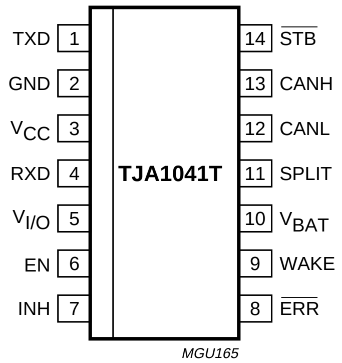


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

As well as dealing with the physical layer as described in the ISO 11898 standard, the TJA1041 controls the whole ECU power management and performs diagnoses of the system.

Operating modes

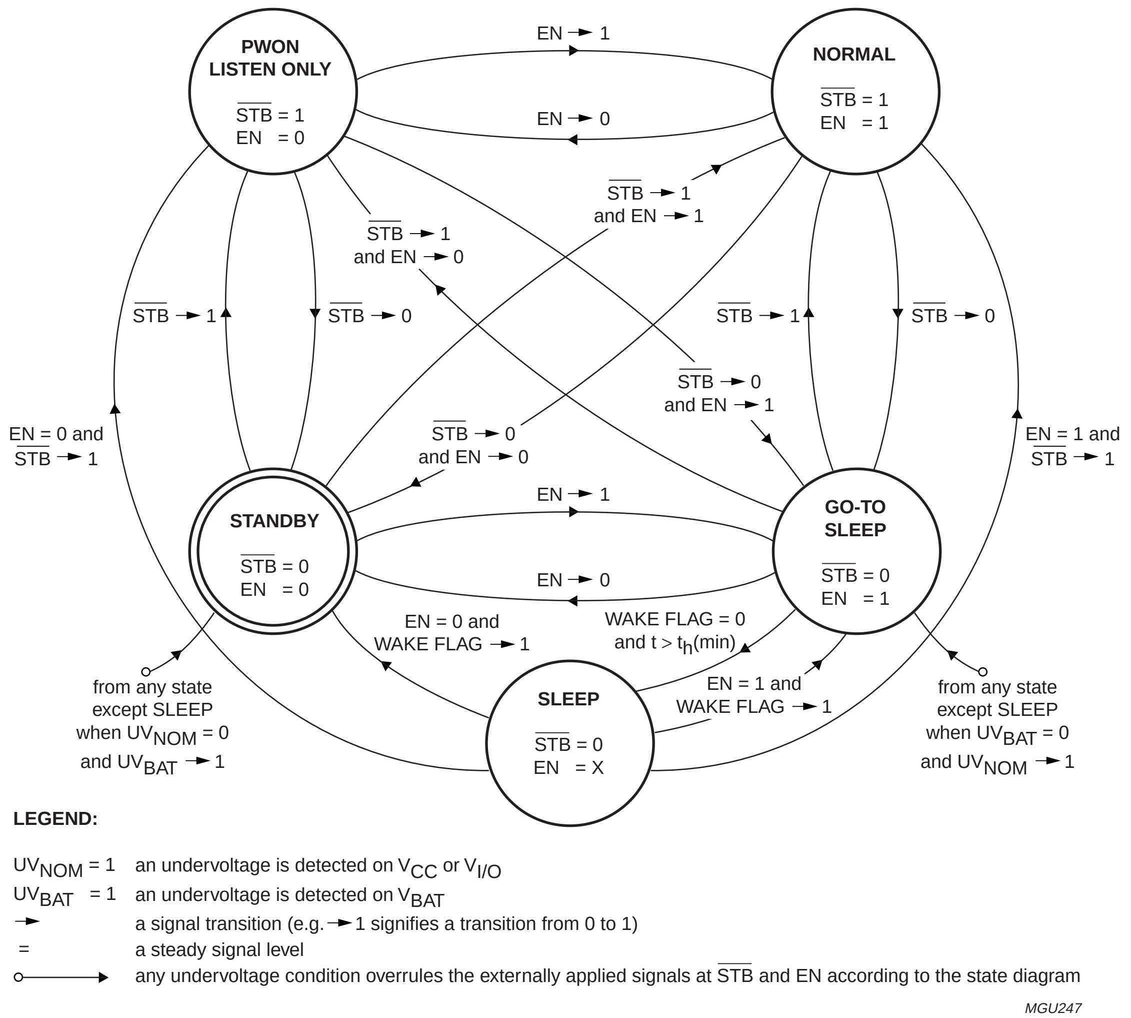
The TJA1041 can be operated in five modes, each with specific features. Two control pins ($\overline{\text{STB}}$ and EN) select the mode of operation, see Table 1 for a detailed description of the modes of operation, and Fig.3 for the state diagram.

Table 1 Operating modes

MODE	Pin $\overline{STB}$	Pin EN	Pin $\overline{ERR}$		Pin RXD		Pin INH
			LOW	HIGH	LOW	HIGH	
Normal	H	H	bus failure detected; note 1	no bus failure detected; note 1	bus dominant	bus recessive	H
			local wake-up request detected; note 2	remote wake-up request detected or no wake-up request detected	bus dominant	bus recessive	H
Pwon/ listen-only	H	L	V_{BAT} Pwon situation detected; note 3	no V_{BAT} Pwon situation detected; note 3	bus dominant	bus recessive	H
			TXD dominant time-out; over-temperature; RXD recessive clamping; TXD to RXD short or bus dominant time-out detected; note 4	no TXD dominant time-out; over-temperature; RXD recessive clamping; TXD to RXD short or bus dominant time-out detected; note 4	bus dominant	bus recessive	H
Go-to sleep command	L	H	wake-up request detected; note 5	no wake-up request detected; note 5	wake-up request detected; note 5	no wake-up request detected; note 5	note 6
Sleep; note 7	L	L					floating
Standby	L	L					H

Notes

1. Valid after the 4th dominant to recessive edge at pin TXD after entering the normal mode.
2. Valid before the 4th dominant to recessive edge at pin TXD after entering the normal mode.
3. Valid if V_{CC} and $V_{I/O}$ are present and coming from the sleep, standby or go-to sleep command mode.
4. Coming from normal mode.
5. Valid if V_{CC} and $V_{I/O}$ are present.
6. Will become floating if this mode is selected for a time longer than the hold time of go-to sleep command ($t_{h(min)}$) and the Pwon flag was previously cleared.
7. Transceiver will only enter the sleep mode if the go-to sleep command mode was selected longer than the hold time of go-to sleep command ($t_{h(min)}$) or by an undervoltage detection on V_{CC} or $V_{I/O}$ for $t > t_{UV(VCC)(VI/O)}$.



EN = 1 means a HIGH-level is present on pin EN.

Fig.3 State diagram operating modes.

NORMAL MODE

In this mode the transceiver is able to transmit and receive data via the bus lines CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD via the multiplexer (MUX) and the I/O-level adapter. After entering the normal mode, pin $\overline{ERR}$ will indicate the wake-up source before the 4th dominant to recessive edge on pin TXD. After the 4th dominant to recessive edge on pin TXD, pin $\overline{ERR}$ will become active (LOW) if a bus failure is present (see Table 1).

PWON/LISTEN-ONLY MODE

In Pwon/listen-only mode the CAN bus signal is reflected at pin RXD without activating the transmitter, thus providing a listen-only behaviour. Entering the Pwon/listen-only mode from the sleep, standby or go-to sleep command mode, pin $\overline{ERR}$ reflects the Pwon flag, indicating a previous loss of battery condition or a first battery connection. Entering the Pwon/listen-only mode from the normal mode, pin $\overline{ERR}$ reflects the local failures like TXD dominant time-out, over-temperature, RXD recessive clamping, bus dominant or TXD to RXD short-circuit situation. The bus is biased at half V_{CC}.

GO-TO SLEEP COMMAND MODE

In this mode a go-to sleep command is given to the transceiver. When this mode is selected for a time longer than the hold time of go-to sleep command and both the wake flag and the Pwon flag were previously cleared, the pull-up current at pin INH will be switched off. The transceiver is not able to transmit or receive data. Pins RXD and $\overline{ERR}$ will only reflect the internal wake-up flag if V_{CC} and $V_{I/O}$ are provided.

SLEEP MODE

The sleep mode is entered when the go-to sleep command mode is selected for longer than the hold time of the go-to sleep command ($t_{h(min)}$). In this mode pin INH is floating. The supply current on pin V_{BAT} is reduced to a minimum in a way that electromagnetic immunity is guaranteed and a wake-up event on the bus lines or on pin WAKE will be recognized. If a wake-up event is recognized, pin INH will be activated. Pin INH can be used to switch the voltage regulator which supplies V_{CC} and/or the supply voltage of the CAN controller and microcontroller ($V_{I/O}$). The bus is biased at ground level.

STANDBY MODE

By switching pins EN and $\overline{STB}$ directly to LOW, the standby mode is entered. The transceiver behaves in the same way as in the sleep mode with the exception that pin INH is HIGH.

Fail-safe fallback modes

The TJA1041 is provided with undervoltage detection circuits on V_{CC}, $V_{I/O}$ and V_{BAT}.

An undervoltage on V_{CC} and $V_{I/O}$ is detected when the voltage on these pins becomes lower than respectively $V_{CC(SLEEP)}$ and $V_{I/O(SLEEP)}$ for a time longer than $t_{UV(VCC)(VI/O)}$. If an undervoltage is detected on V_{CC} or $V_{I/O}$, the transceiver will enter the sleep mode. In this case the voltage regulators will be switched off via pin INH, which prevents extra current consumption in case of a short-circuit. Any wake-up event will switch on the voltage regulators via pin INH. If the short-circuit still exists, the voltage regulators will be switched off again via pin INH. If the short-circuit has disappeared, the transceiver will enter the mode determined by the signals on pins EN and $\overline{STB}$.

An undervoltage on V_{BAT} is detected when the voltage on this pin becomes lower than $V_{BAT(STANDBY)}$. If an undervoltage is detected on V_{BAT}, the TJA1041 will enter the sleep mode to guarantee that the transceiver will not disturb the bus and will ensure a low current consumption. Once the undervoltage is removed, the transceiver will return to the operating mode as determined by the logical state of pins EN and $\overline{STB}$.

Split circuit

The split circuit is a DC stabilized voltage source of $0.5V_{CC}$. It is turned on only in normal and Pwon/listen-only mode. In all other modes pin SPLIT is floating. The split circuit can be used to stabilize the recessive common-mode voltage in case of a split termination (see Fig.4). In case of a recessive bus voltage $<0.5V_{CC}$ due to the presence of an unsupplied transceiver in the network with a significant leakage current from the bus lines to ground, the split circuit will stabilize this recessive voltage to $0.5V_{CC}$. So a start of transmission does not cause a step in the common-mode signal which will lead to a poor ElectroMagnetic Emission (EME) behaviour.

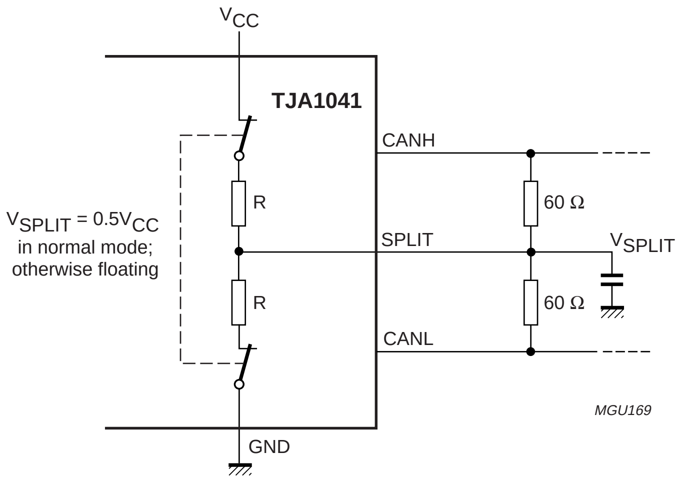


Fig.4 Stabilization circuitry example.

Pwon flag

The Pwon flag will be set in case of a power-on situation at V_{BAT}. It is redirected to pin $\overline{ERR}$ in the Pwon/listen-only mode coming from the sleep, standby or go-to sleep command mode. The Pwon flag will be reset if the transceiver enters the normal mode. In case of an active Pwon flag, the sleep mode cannot be entered. So in a V_{BAT} Pwon situation the sleep mode can only be entered once the normal mode of the transceiver has been selected.

Wake-up

Figure 5 shows the state diagram of wake-up. There are several ways to wake-up the TJA1041 which is in sleep or standby mode:

1. Wake-up via a dominant bus state
2. Local wake-up via an edge at pin WAKE
3. Mode change from sleep or standby mode to normal or Pwon/listen-only mode (wake-up flag will not be set).

The wake-up flag will be reset if the transceiver enters the normal mode.

WAKE-UP VIA A DOMINANT BUS STATE

The bus lines are monitored via a low-power differential comparator. Once the low-power differential comparator has detected a dominant bus level for more than t_{BUS}, the internal wake-up flag will be set.

See Table 1 for the effect this will have on pins $\overline{ERR}$, RXD and INH, depending on the actual mode of the transceiver.

LOCAL WAKE-UP VIA EDGE AT PIN WAKE

Any transition at pin WAKE results in a wake-up event. In order to suppress external noise a filter is integrated at pin WAKE. This means that the subsequent state on pin WAKE has to be valid for a certain time (t_{WAKE}). Pin WAKE provides an internal pull-up towards V_{BAT} if a HIGH level was present at pin WAKE for at least t_{WAKE} or an internal pull-down towards GND if a LOW level was present at pin WAKE for at least t_{WAKE}.

WAKE-UP VIA MODE TRANSITION

It is also possible to set pin INH to a HIGH level with a mode transition towards normal mode. This is useful for applications with a continuously powered microcontroller.

WAKE-UP SOURCE RECOGNITION

The TJA1041 can recognize if the wake-up source is a local wake-up event on pin WAKE or a wake-up via a dominant bus state. The wake-up source flag is set in case the wake-up source was an edge at pin WAKE. The wake-up source can be read on pin $\overline{ERR}$ if the normal mode is entered coming from any different mode (see Fig.5). This flag will be reset after four dominant to recessive edges on pin TXD in normal operating mode.

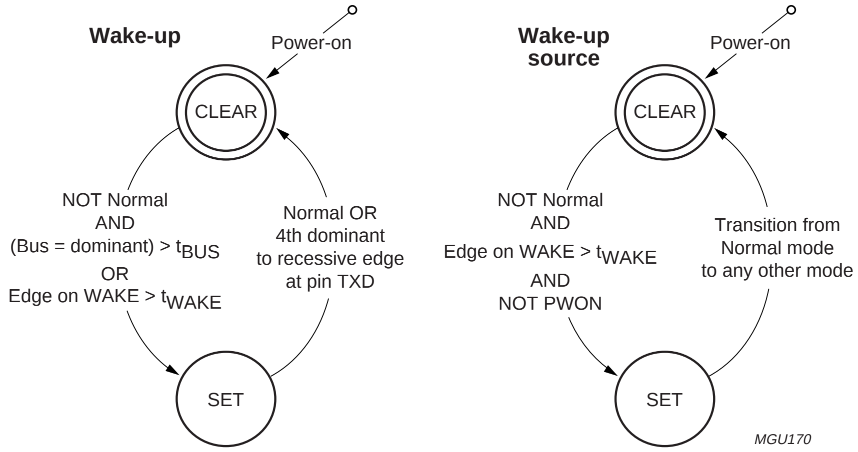


Fig.5 State diagrams of wake-up flag and wake-up source.

Error flags

There are two error flags which can be read at pin $\overline{ERR}$:

- An error flag indicating a bus failure in normal mode. This flag will be set after the 4th dominant to recessive edge at pin TXD if a bus failure was present
- An error flag indicating a TXD dominant time-out, over-temperature, RXD recessive clamping, bus dominant time-out or TXD to RXD short-circuit situation. This flag will be set in normal mode or Pwon/listen-only mode, but can be read only in the Pwon/listen-only mode.The flag will be reset if the transceiver enters the normal mode or if RXD is dominant while TXD is recessive.

BUS FAILURE DIAGNOSIS

During normal mode the TJA1041 provides an active LOW bus failure diagnosis output via pin $\overline{ERR}$ in case the transceiver drives the bus lines dominant. A detected bus failure can be read at pin $\overline{ERR}$ during normal mode.

TXD DOMINANT TIME-OUT FUNCTION

A ‘TXD dominant time-out’ timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure.

The timer is triggered by a negative edge on pin TXD. If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{DOM}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD. The transmitter stays disabled until RXD is dominant while TXD is recessive or a mode change towards normal mode.

The TXD dominant time-out time (t_{DOM}) defines the minimum possible bit rate of 40 kBaud. See Table 1 for the effect this will have on pin $\overline{ERR}$, depending on the actual mode of the transceiver.

OVER-TEMPERATURE DETECTION

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds 165 °C typical, the output drivers will be disabled until the virtual junction temperature becomes lower than 165 °C typical and TXD becomes recessive again. For this reason an output driver oscillation with temperature drifts is not possible.

RXD RECESSIVE CLAMPING

If a RXD recessive clamping situation is detected, the transmitter will be disabled to prevent a disturbance of the bus. If RXD is clamped to recessive the CAN controller can start a message anytime because it does not see a dominant state on the bus. This will disturb the messages on the bus. The transmitter stays disabled until RXD is dominant while TXD is recessive, or until a mode change towards normal mode occurs.

BUS DOMINANT TIME-OUT

If a RXD dominant time-out is detected, it can be read out in Pwon/listen-only mode at pin $\overline{ERR}$. If an application is using pin SPLIT and a short-circuit between V_{BAT} and pin CANH is present, the bus voltage could exceed 0.9 V which means that the transceiver will see a permanent dominant state on the bus and therefore RXD will become dominant (LOW). Because the normal bus failure detection circuit uses dominant to recessive edges at TXD, this bus failure will not be recognized because the CAN controller will not send a message if the bus is dominant.

TXD TO RXD SHORT-CIRCUIT

If pins RXD and TXD are short-circuited, the bus will become continuously dominant once the bus is driven dominant because the low-side driver of RXD is typically stronger than the high-side driver connected to TXD (CAN-controller). The TXD dominant time-out will disable the transmitter which results in a recessive state of the bus. The transmitter stays disabled until RXD is dominant while TXD is recessive, or until a mode-change towards normal mode occurs.

I/O-level adaptation

$V_{I/O}$ can be used to define the ratio-metric digital input threshold for pins TXD, EN and $\overline{STB}$ and the HIGH-level output voltage for pins RXD and $\overline{ERR}$. Due to this function the transceiver can be interfaced to any microcontroller with a power supply voltage between 2.8 and 5.25 V.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{BAT}	supply voltage on pin V_{BAT}		–0.3	+40	V
V_{CC}	supply voltage on pin V_{CC}		–0.3	+6	V
$V_{I/O}$	supply voltage on pin $V_{I/O}$		–0.3	V_{CC} + 0.3	V
V_n	DC voltage on pins $\overline{ERR}$, TXD, RXD, EN and $\overline{STB}$		–0.3	V_{CC} + 0.3	V
V_{CANH}	DC voltage on pin CANH	0 < V_{CC} < 5.25 V; no time limit	–27	+40	V
V_{CANL}	DC voltage on pin CANL	0 < V_{CC} < 5.25 V; no time limit	–27	+40	V
V_{SPLIT}	DC voltage on pin SPLIT	0 < V_{CC} < 5.25 V; no time limit	–27	+40	V
V_{trt}	transient voltages on pins CANH, CANL, SPLIT and V_{BAT}	according to ISO 7637; see Fig.7	–200	+200	V
$V_{i(WAKE)}$	DC input voltage on pin WAKE		–0.3	V_{BAT} + 0.3	V
$I_{i(WAKE)}$	DC input current on pin WAKE		–15	–	mA
$V_{O(INH)}$	DC output voltage on pin INH		–0.3	V_{BAT} + 0.3	V
T_{vj}	virtual junction temperature	note 1	–40	+150	°C
T_{stg}	storage temperature		–55	+150	°C
$V_{esd(HBM)}$	electrostatic discharge voltage on all pins	Human Body Model (HBM); note 2	–4	+4	kV
$V_{esd(MM)}$	electrostatic discharge voltage on all pins	Machine Model (MM); note 3	–200	+200	V

Notes

1. Junction temperature in accordance with IEC 60747-1. An alternative definition of T_{vj} is: $T_{vj} = T_{amb} + P \times R_{th(vj\text{-}amb)}$, where $R_{th(vj\text{-}amb)}$ is a fixed value to be used for the calculating of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor via a 0.75 µH series inductor and a 25 Ω series resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	tbf	K/W

CHARACTERISTICS

V_{CC} = 4.75 to 5.25 V; V_{BAT} = 5 to 27 V; T_{vj} = –40 to +150 °C; $V_{I/O}$ = 2.8 V to V_{CC}; R_L = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; unless otherwise specified; note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies (pins V_{BAT}, V_{CC} and $V_{I/O}$)						
$V_{BAT(stb)}$	V_{BAT} supply voltage for forced fail-safe fallback mode	V_{CC} = 5 V (fail-safe)	2.75	tbf	4.5	V
$V_{BAT(Pwon)}$	V_{BAT} supply voltage for setting Pwon flag		2.75	–	4.5	V
$V_{CC(sleep)}$	V_{CC} undervoltage detection for forced go-to sleep command mode	V_{BAT} = 12 V (fail-safe)	2.75	tbf	4.5	V
$V_{I/O(sleep)}$	$V_{I/O}$ undervoltage detection for forced go-to sleep command mode		0.5	1	2	V
I_{BAT}	supply current on pin BAT	sleep or standby mode; V_{INH} = V_{WAKE} = 12 V; V_{BAT} = 12 V	10	20	30	µA
		normal or Pwon/listen-only mode	10	20	30	µA
I_{CC}	supply current on pin V_{CC}	sleep or standby mode	–	1	10	µA
		normal or Pwon/listen-only mode; V_{TXD} = $V_{I/O}$ (recessive)	2	6	10	mA
		normal mode; V_{TXD} = 0 V (dominant); R_L = 60 Ω	25	55	80	mA
$I_{I/O}$	supply current on pin $V_{I/O}$	sleep or standby mode	–	0	–	µA
		normal or Pwon/listen-only mode	–	0.6	1	mA
Transmitter data input (pin TXD)						
V_{IH}	HIGH-level input voltage		$0.7V_{I/O}$	–	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	–	$0.3V_{I/O}$	V
I_{IH}	HIGH-level input current	normal mode; V_{TXD} = $V_{I/O}$	–5	0	+5	µA
I_{IL}	LOW-level input current	normal mode; V_{TXD} = $0.3V_{I/O}$	–75	–200	–750	µA
C_i	input capacitance	not tested	–	5	10	pF
Standby and enable control inputs (pins $\overline{STB}$ and EN)						
V_{IH}	HIGH-level input voltage		$0.7V_{I/O}$	–	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	–	$0.3V_{I/O}$	V
I_{IH}	HIGH-level input current	V_{STB} = V_{EN} = $0.7V_{I/O}$	1	4	10	µA
I_{IL}	LOW-level input current	V_{STB} = V_{EN} = 0 V	–	0	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiver data output (pin RXD)						
I_{OH}	HIGH-level output current	$V_{RXD} = V_{I/O} - 0.4$ V; $V_{I/O} = V_{CC}$	–1	–3	–6	mA
I_{OL}	LOW-level output current	$V_{RXD} = 0.4$ V	2	5	15	mA
Error and power-on indication output (pin $\overline{ERR}$)						
I_{OH}	HIGH-level output current	$V_{ERR} = V_{I/O} - 0.4$ V; $V_{I/O} = V_{CC}$	tbf	tbf	50	µA
I_{OL}	LOW-level output current	$V_{ERR} = 0.4$ V	0.1	0.35	0.75	mA
Local wake-up input (pin WAKE)						
I_{OL}	LOW-level input current	$V_{WAKE} = V_{BAT}$ - 3.1 V	1	4	10	µA
I_{OH}	HIGH-level input current	$V_{WAKE} = V_{BAT} - 1.9$ V	–1	–4	–10	µA
$V_{th(wake)}$	wake-up threshold voltage	$V_{STB} = 0$ V	$V_{BAT} - 3$	$V_{BAT} - 2.5$	$V_{BAT} - 2$	V
Bus lines (pins CANH and CANL)						
$V_{O(CANH)(reces)}$, $V_{O(CANL)(reces)}$	recessive output voltage on pins CANH and CANL	normal or Pwon/listen-only mode; $V_{TXD} = V_{I/O}$; no load	2	$0.5V_{CC}$	3	V
		sleep or standby mode; no load	–0.1	0	+0.1	V
$I_{O(CANH)(reces)}$, $I_{O(CANL)(reces)}$	recessive output current on pins CANH and CANL	$-27\ V < V_{CAN} < 32$ V	–2.5	–	+2.5	mA
$V_{O(CANH)(dom)}$	dominant output voltage on pin CANH	$V_{TXD} = 0$ V	3	3.6	4.25	V
$V_{O(CANL)(dom)}$	dominant output voltage on pin CANL	$V_{TXD} = 0$ V	0.5	1.4	1.75	V
$V_{O(dom)(m)}$	matching of dominant output voltage between pins CANH and CANL		–	–	tbf	V
$V_{i(dif)(bus)}$	differential input voltage ($V_{CANH} - V_{CANL}$)	$V_{TXD} = 0$ V; $45\ \Omega < R_L < 65\ \Omega$; dominant	1.5	–	3.0	V
		$V_{TXD} = V_{I/O}$; no load; recessive	–50	–	+50	mV
$I_{O(CANH)(sc)}$	short-circuit output current on pin CANH	$V_{CANH} = 0$ V; $V_{TXD} = 0$ V	–45	–70	–95	mA
$I_{O(CANL)(sc)}$	short-circuit output current on pin CANL	$V_{CANL} = 40$ V; $V_{TXD} = 0$ V	45	70	100	mA
$R_{sc(CANH,CANL)}$	detectable short-circuit resistance between bus lines and V_{BAT}, V_{CC} and GND	normal mode	0	–	50	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{dif(th)}$	differential receiver threshold voltage	V_{CANH} > –12 V; V_{CANL} < 12 V				
		normal mode (see Fig.8)	0.5	0.7	0.9	V
		standby mode	0.5	0.7	1	V
$V_{dif(hys)}$	differential receiver hysteresis	normal mode; V_{CANH} > –12 V; V_{CANL} < 12 V	50	70	100	mV
$R_{i(cm)}$	common-mode input resistance	normal mode	15	25	35	kΩ
$R_{i(cm)(m)}$	matching between pin CANH and pin CANL common-mode input resistance	$V_{CANH} = V_{CANL}$	–3	0	+3	%
$R_{i(dif)}$	differential input resistance		25	50	75	kΩ
$C_{i(cm)}$	common-mode input capacitance	$V_{TXD} = V_{CC}$; not tested	–	–	20	pF
$C_{i(dif)}$	differential input capacitance	$V_{TXD} = V_{CC}$; not tested	–	–	10	pF
I_{LI}	input leakage current	V_{CC} = 0 V; $V_{CANH} = V_{CANL}$ = 5 V	100	170	250	μA
Common-mode stabilization output (pin SPLIT)						
V_o	output voltage	normal mode; –500 μA < I_{SPLIT} < 500 μA	$0.3V_{CC}$	$0.5V_{CC}$	$0.7V_{CC}$	V
$\lvert I_L \rvert$	leakage current	sleep or standby mode	–	0	5	μA
Inhibit output (pin INH)						
ΔV_H	HIGH-level voltage drop	I_{INH} = –0.18 mA	–	–	0.8	V
$\lvert I_L \rvert$	leakage current	sleep or standby mode	–	0	5	μA
Thermal shutdown						
$T_{j(sd)}$	shutdown junction temperature		155	165	180	°C
Timing characteristics; see Fig.10						
$t_{d(TXD-BUSon)}$	delay TXD to bus active	normal mode	tbf	tbf	110	ns
$t_{d(TXD-BUSoff)}$	delay TXD to bus inactive		tbf	tbf	95	ns
$t_{d(BUSon-RXD)}$	delay bus active to RXD		tbf	tbf	115	ns
$t_{d(BUSoff-RXD)}$	delay bus inactive to RXD		tbf	tbf	160	ns
$t_{UV(VCC)}$, $t_{UV(VI/O)}$	undervoltage detection time on V_{CC} and $V_{I/O}$		5	10	15	ms
$t_{dom(TXD)}$	TXD dominant time-out	V_{TXD} = 0 V	300	600	1000	μs
$t_{dom(bus)}$	bus dominant time-out	V_{dif} > 0.9 V	300	600	1000	μs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{h(min)}$	minimum hold time of go-to sleep command		5	25	50	µs
t_{BUS}	dominant time for wake-up via bus	sleep or standby mode; V_{BAT} = 12 V	1	2	3.5	µs
t_{wake}	minimum wake-up time after receiving a falling or rising edge	sleep or standby mode; V_{BAT} = 12 V	5	25	50	µs

Note

1. All parameters are guaranteed over the virtual junction temperature range by design, but only 100% tested at 125 °C ambient temperature for dies on wafer level and in addition to this 100% tested at 25 °C ambient temperature for cased products.

TEST AND APPLICATION INFORMATION

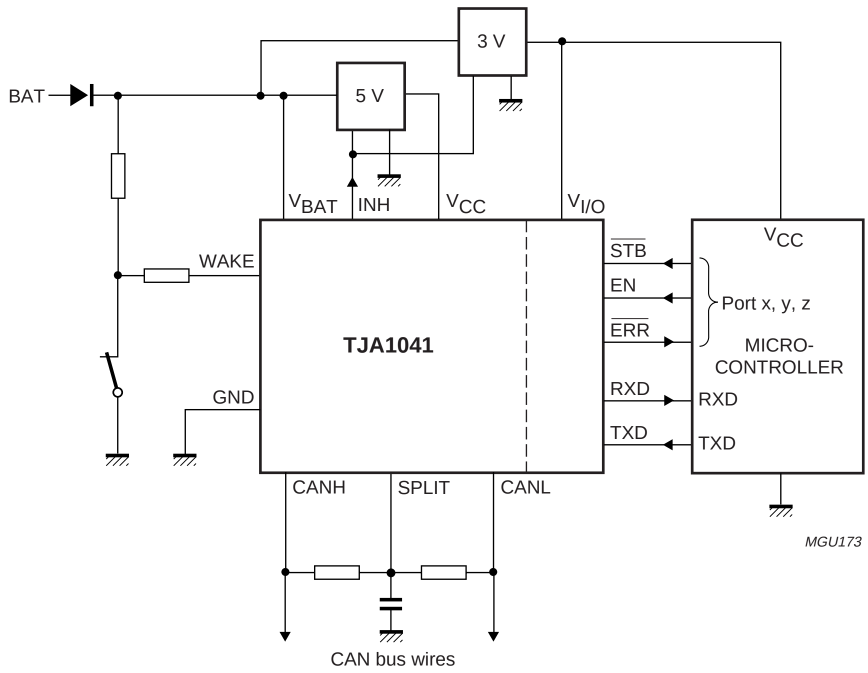
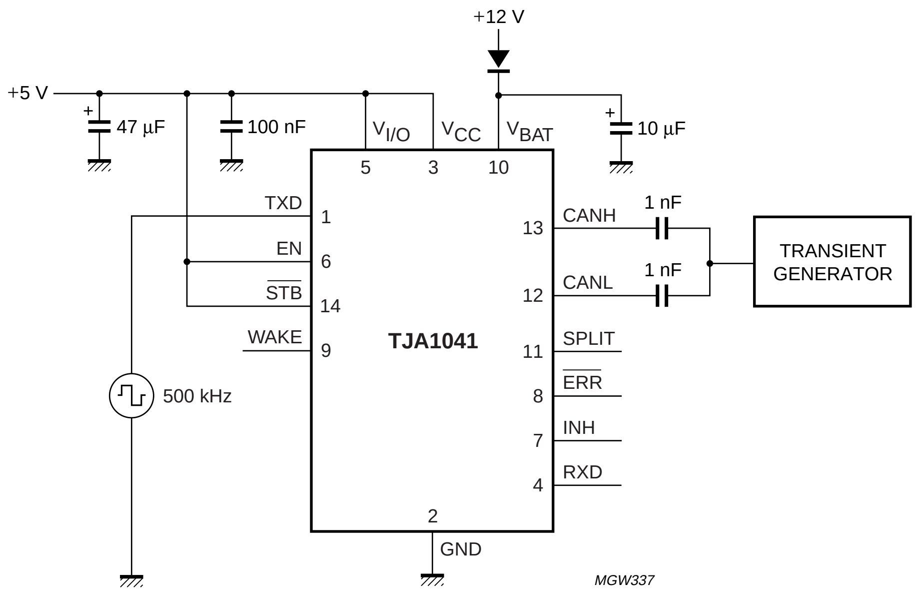


Fig.6 Typical application for 3 V microcontroller.



The waveforms of the applied transients will be in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, 3b, 5, 6 and 7.

Fig.7 Test circuit for automotive transients.

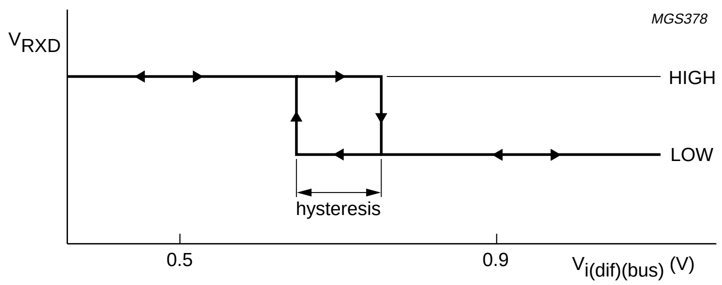


Fig.8 Hysteresis of the receiver.

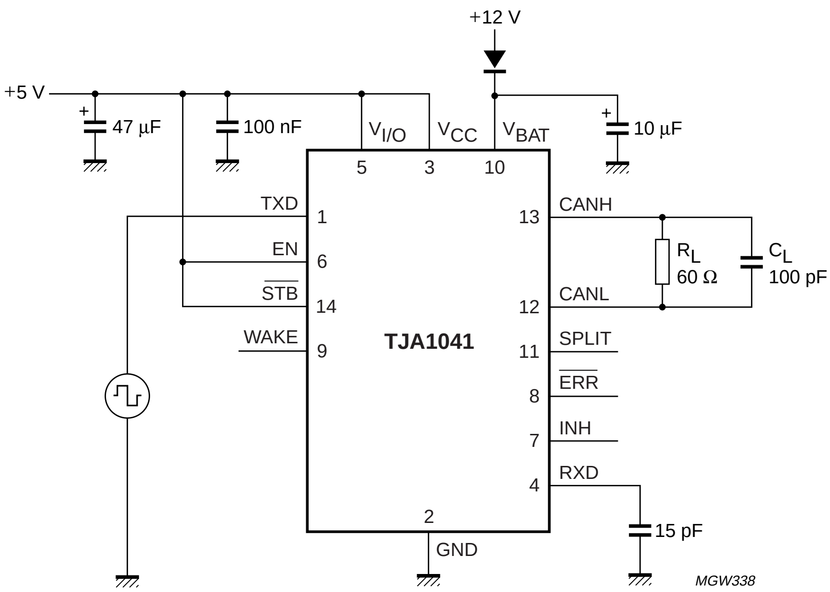
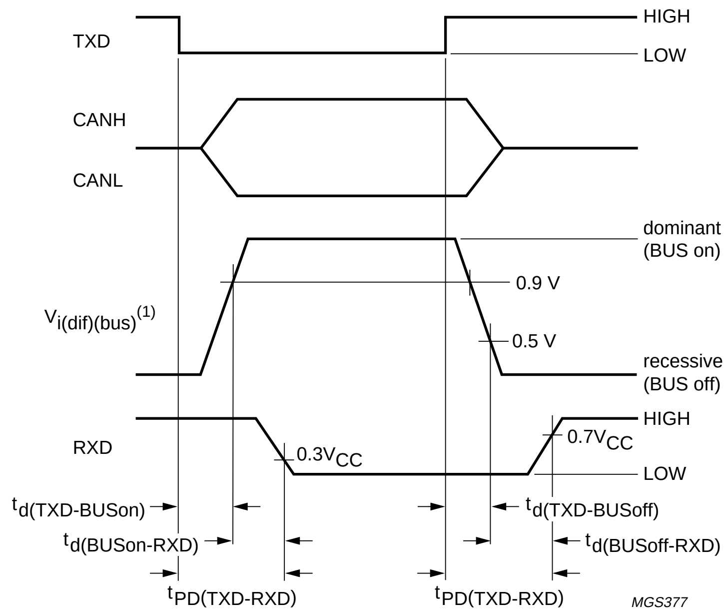


Fig.9 Test circuit for timing characteristics.

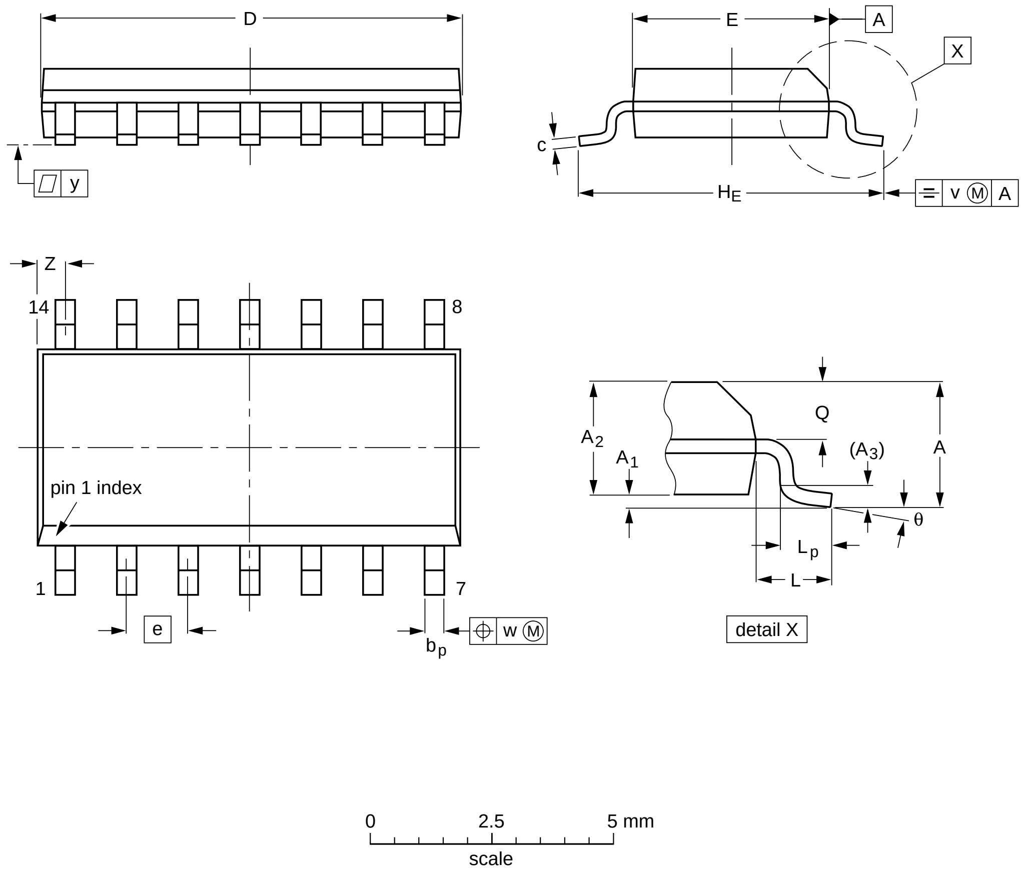


(1) $V_{i(dif)(bus)} = V_{CANH} - V_{CANL}$.

Fig.10 Timing diagram.

PACKAGE OUTLINE

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				~~97-05-22~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a LOW voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
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