INTEGRATED CIRCUITS

DATA SHEET

TJA1040
High speed CAN transceiver

Preliminary specification 2001 Dec 18

File under Integrated Circuits, IC18

Philips Semiconductors

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FEATURES

- Fully compatible with the ISO 11898 standard
- High speed (up to 1 Mbaud)
- Very low ElectroMagnetic Emission (EME)
- Differential receiver with high common-mode range for ElectroMagnetic Immunity (EMI)
- Transceiver in unpowered state disengages from the bus (zero load)
- Input levels compatible with 3.3 and 5 V devices
- Voltage source for stabilizing the recessive bus level if split termination is used (further improvement of EME)
- At least 110 nodes can be connected
- Very low-current standby mode with wake-up via the bus (remote)
- Transmit Data (TXD) dominant time-out function
- Bus pins protected against transients in an automotive environment
- Bus pins and pin SPLIT short-circuit proof to battery and ground
- Thermally protected.

GENERAL DESCRIPTION

The TJA1040 is the interface between the Controller Area Network (CAN) protocol controller and the physical bus. It is primarily intended for high speed applications, up to 1 Mbaud, in passenger cars. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The TJA1040 is the pin and functionality successor of the PCA82C250/251 high speed CAN transceiver. Moreover, it is pin compatible with the TJA1050. Together with an excellent EMC performance and ideal passive behaviour in unpowered state, the TJA1040 also provides a low-power management, supporting remote wake-up.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		4.75	5.25	V
I_{CC}	supply current	standby mode	5	15	µA
V_{CANH}	DC voltage on pin CANH	$0 < V_{CC} < 5.25$ V; no time limit	–27	+40	V
V_{CANL}	DC voltage on pin CANL	$0 < V_{CC} < 5.25$ V; no time limit	–27	+40	V
V_{SPLIT}	DC voltage on pin SPLIT	$0 < V_{CC} < 5.25$ V; no time limit	–27	+40	V
T_{vj}	virtual junction temperature		–40	+150	°C
$V_{esd(HBM)}$	electrostatic discharge voltage on all pins	Human Body Model (HBM)	–4	+4	kV
$t_{PD(TXD-RXD)}$	propagation delay TXD to RXD	$V_{STB} = 0$ V	–	255	ns

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TJA1040T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

BLOCK DIAGRAM

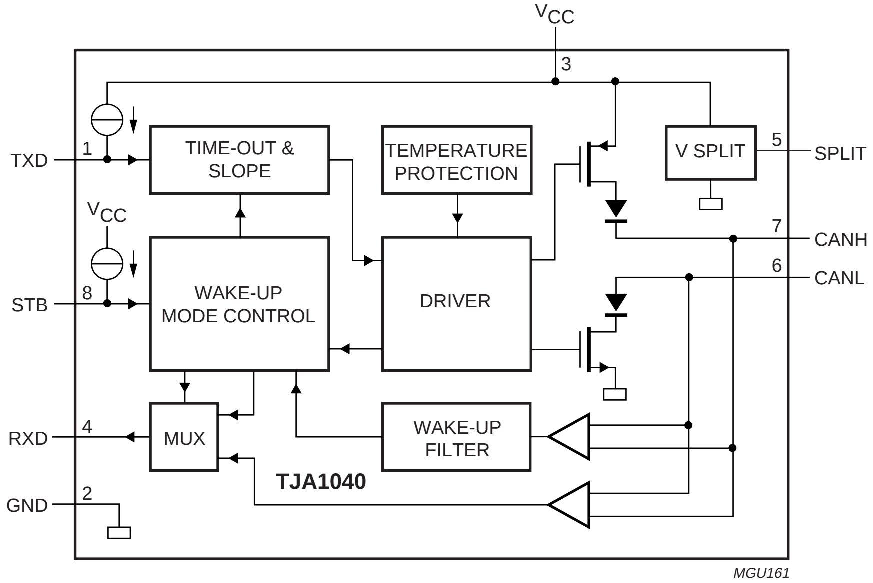


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
TXD	1	transmit data input
GND	2	ground supply
V_{CC}	3	supply voltage
RXD	4	receive data output; reads out data from the bus lines
SPLIT	5	common-mode stabilization output
CANL	6	LOW-level CAN bus line
CANH	7	HIGH-level CAN bus line
STB	8	standby mode control input

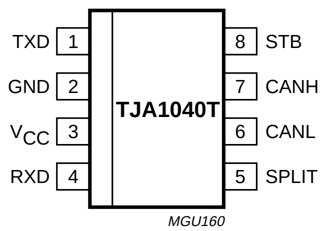


Fig.2 Pinning diagram.

FUNCTIONAL DESCRIPTION

Operating modes

The TJA1040 provides two modes of operation which are selectable via pin STB. See Table 1 for a detailed description of the modes of operation.

Table 1 Operating modes

MODE	Pin STB	Pin RXD	
		LOW	HIGH
normal	L	bus dominant	bus recessive
standby	H	wake-up request detected	no wake-up request detected

NORMAL MODE

In this mode the transceiver is able to transmit and receive data via the bus lines CANH and CANL. See Fig.1 for the block diagram. The differential receiver converts the analog data on the bus lines into digital data which is output to RXD via the multiplexer (MUX). The slope of the output signals on the bus lines is fixed and optimized in a way that lowest ElectroMagnetic Emission (EME) is guaranteed.

STANDBY MODE

In this mode the transmitter and receiver are switched off, and the low-power differential receiver monitors the bus lines.

The supply current on V_{CC} is reduced to a minimum in such a way that ElectroMagnetic Immunity (EMI) is guaranteed and a wake-up event on the bus lines will be recognized.

In this mode the bus lines are terminated to ground to reduce the supply current (I_{CC}) to a minimum. A diode is added in series with the high-side driver of RXD to prevent a reverse current from RXD to V_{CC} in the unpowered state. In normal mode this diode is bypassed. This diode is not bypassed in standby mode to reduce current consumption.

Split circuit

The split circuit is a DC stabilized voltage source of $0.5V_{CC}$. It is turned on only in normal mode. In standby mode pin SPLIT is floating. The split circuit can be used to stabilize the recessive common-mode voltage by connecting pin SPLIT to the centre tap of the split termination (see Fig.3). In case of a recessive bus voltage $<0.5V_{CC}$ due to the presence of an unsupplied transceiver in the network with a significant leakage current from the bus lines to ground, the split circuit will stabilize this recessive voltage to $0.5V_{CC}$. So a start of transmission does not cause a step in the common-mode signal which will lead to a poor ElectroMagnetic Emission (EME) behaviour.

Wake-up

In the standby mode the bus lines are monitored via a low-power differential comparator. Once the low-power differential comparator has detected a dominant bus level for more than t_{BUS}, pin RXD will become LOW.

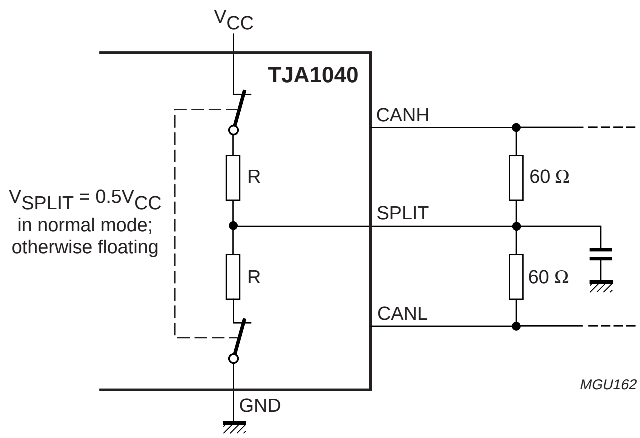


Fig.3 Stabilization circuitry example.

Over-temperature detection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds 165 °C the output drivers will be disabled until the virtual junction temperature becomes lower than the typical 165 °C and TXD becomes recessive again. For this reason an output driver oscillation with temperature drifts is not possible.

TXD dominant time-out function

A ‘TXD dominant time-out’ timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{dom}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD. The TXD dominant time-out time (t_{dom}) defines the minimum possible bit rate of 40 kBaud.

Fail-safe features

Pin TXD provides a pull-up towards V_{CC} in order to force a recessive level in case pin TXD is unsupplied.

Pin STB provides a pull-up towards V_{CC} in order to force the transceiver into standby mode in case pin STB is unsupplied.

In the event that the V_{CC} is lost, pins TXD, STB and RXD will become floating to prevent reverse supplying conditions via these pins.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.3	+6	V
V_n	DC voltage on pins TXD, RXD and STB		–0.3	V_{CC} + 0.3	V
V_{CANH}	DC voltage on pin CANH	0 < V_{CC} < 5.25 V; no time limit	–27	+40	V
V_{CANL}	DC voltage on pin CANL	0 < V_{CC} < 5.25 V; no time limit	–27	+40	V
V_{SPLIT}	DC voltage on pin SPLIT	0 < V_{CC} < 5.25 V; no time limit	–27	+40	V
V_{trt}	transient voltages on pins CANH, CANL and SPLIT	according to ISO 7637; see Fig.5	–200	+200	V
T_{vj}	virtual junction temperature	note 1	–40	+150	°C
T_{stg}	storage temperature		–55	+150	°C
$V_{esd(HBM)}$	electrostatic discharge voltage on all pins	Human Body Model (HBM); note 2	–4	+4	kV
$V_{esd(MM)}$	electrostatic discharge voltage on all pins	Machine Model (MM); note 3	–200	+200	V

Notes

1. Junction temperature in accordance with IEC 60747-1. An alternative definition of T_{vj} is: $T_{vj} = T_{amb} + P \times R_{th(vj-amb)}$, where $R_{th(vj-amb)}$ is a fixed value to be used for the calculating of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor via a 0.75 µH series inductor and a 25 Ω series resistor.

CHARACTERISTICS

V_{CC} = 4.75 to 5.25 V; T_{vj} = –40 to +150 °C; R_L = 60 Ω; all voltages are defined with respect to ground; positive currents flow into the IC; unless otherwise specified; note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin V_{CC})						
I_{CC}	supply current	standby mode	5	10	15	μA
		normal mode				
		recessive; $V_{TXD} = V_{CC}$	2.5	5	10	mA
		dominant; V_{TXD} = 0 V	30	50	70	mA
Transmitter data input (pin TXD)						
V_{IH}	HIGH-level input voltage		2	–	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	–	+0.8	V
I_{IH}	HIGH-level input current	$V_{TXD} = V_{CC}$	–5	0	+5	μA
I_{IL}	LOW-level input current	normal mode; V_{TXD} = 0 V	–100	–200	–300	μA
C_i	input capacitance	not tested	–	5	10	pF
Standby input (pin STB)						
V_{IH}	HIGH-level input voltage		2	–	V_{CC} + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	–	+0.8	V
I_{IH}	HIGH-level input current	$V_{STB} = V_{CC}$	–	0	–	μA
I_{IL}	LOW-level input current	V_{STB} = 0 V	–1	–4	–10	μA
Receiver data output (pin RXD)						
V_{OH}	HIGH-level output voltage	standby mode; I_{RXD} = –100 μA	V_{CC} – 1.1	V_{CC} – 0.7	V_{CC} – 0.4	V
I_{OH}	HIGH-level output current	normal mode; $V_{RXD} = V_{CC}$ – 0.4 V	–0.1	–0.4	–1	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V	2	8.5	20	mA
Common-mode stabilization output (pin SPLIT)						
V_o	output voltage	normal mode; –500 μA < I_o < +500 μA	$0.3V_{CC}$	$0.5V_{CC}$	$0.7V_{CC}$	V
$\lvert I_L \rvert$	leakage current	standby mode	–	0	5	μA
Bus lines (pins CANH and CANL)						
$V_{O(CANH)(reces)}$	recessive output voltage on pin CANH	normal mode; $V_{TXD} = V_{CC}$; no load	2	$0.5V_{CC}$	3	V
		standby mode; no load	–0.1	0	0.1	V
$I_{O(CANH)(reces)}$	recessive output current on pin CANH	–27 V < V_{CANH} < +32 V	–2.5	–	+2.5	mA
$V_{O(CANL)(reces)}$	recessive output voltage on pin CANL	normal mode; $V_{TXD} = V_{CC}$; no load	2	$0.5V_{CC}$	3	V
		standby mode; no load	–0.1	0	0.1	V
$I_{O(CANL)(reces)}$	recessive output current on pin CANL	–27 V < V_{CANH} < +32 V	–2.5	–	+2.5	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{O(CANH)(dom)}$	dominant output voltage on pin CANH	V_{TXD} = 0 V	3	3.6	4.25	V
$V_{O(CANL)(dom)}$	dominant output voltage on pin CANL	V_{TXD} = 0 V	0.5	1.4	1.75	V
$V_{O(dom)(m)}$	matching between CANH and CANL dominant output voltage		–	–	tbf	V
$V_{O(dif)(bus)}$	differential bus output voltage ($V_{CANH} – V_{CANL}$)	V_{TXD} = 0 V; dominant; 45 Ω < R_L < 65 Ω	1.5	–	3.0	V
		V_{TXD} = V_{CC}; recessive; no load	–50	–	+50	mV
$I_{O(CANH)(sc)}$	short-circuit output current on pin CANH	V_{CANH} = 0 V; V_{TXD} = 0 V	–45	–70	–95	mA
$I_{O(CANL)(sc)}$	short-circuit output current on pin CANL	V_{CANL} = 40 V; V_{TXD} = 0 V	45	70	100	mA
$V_{dif(th)}$	differential receiver threshold voltage	V_{CANH} > –12 V; V_{CANL} < 12 V				
		normal mode (see Fig.6)	0.5	0.7	0.9	V
		standby mode	0.5	0.7	1	V
$V_{dif(hys)}$	differential receiver hysteresis voltage	normal mode; V_{CANH} > –12 V; V_{CANL} < 12 V	50	70	100	mV
$R_{i(cm)}$	common-mode input resistance	normal mode	15	25	35	kΩ
$R_{i(cm)(m)}$	matching between pin CANH and pin CANL common-mode input resistance	V_{CANH} = V_{CANL}	–3	0	+3	%
$R_{i(dif)}$	differential input resistance		25	50	75	kΩ
$C_{i(cm)}$	common-mode input capacitance	V_{TXD} = V_{CC}; not tested	–	–	20	pF
$C_{i(dif)}$	differential input capacitance	V_{TXD} = V_{CC}; not tested	–	–	10	pF
I_{LI}	input leakage current	V_{CC} = 0 V; V_{CANH} = V_{CANL} = 5 V	–5	0	+5	µA
Thermal shutdown						
$T_{j(sd)}$	shutdown junction temperature		155	165	180	°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing characteristics; see Fig.8						
$t_{d(TXD-BUSon)}$	delay TXD to bus active	normal mode	tbf	tbf	110	ns
$t_{d(TXD-BUSoff)}$	delay TXD to bus inactive		tbf	tbf	95	ns
$t_{d(BUSon-RXD)}$	delay bus active to RXD		tbf	tbf	115	ns
$t_{d(BUSoff-RXD)}$	delay bus inactive to RXD		tbf	tbf	160	ns
$t_{dom(TXD)}$	TXD dominant time-out	V_{TXD} = 0 V	300	600	1000	µs
t_{BUS}	dominant time for wake-up via bus	standby mode	tbf	2	tbf	µs
$t_{d(stb-norm)}$	delay standby mode to normal mode		tbf	20	tbf	µs
$t_{PD(TXD-RXD)}$	propagation delay TXD to RXD	V_{STB} = 0 V	–	–	255	ns

Note

1. All parameters are guaranteed over the virtual junction temperature range by design, but only 100% tested at 125 °C ambient temperature for dies on wafer level and in addition to this 100% tested at 25 °C ambient temperature for cased products.

TEST AND APPLICATION INFORMATION

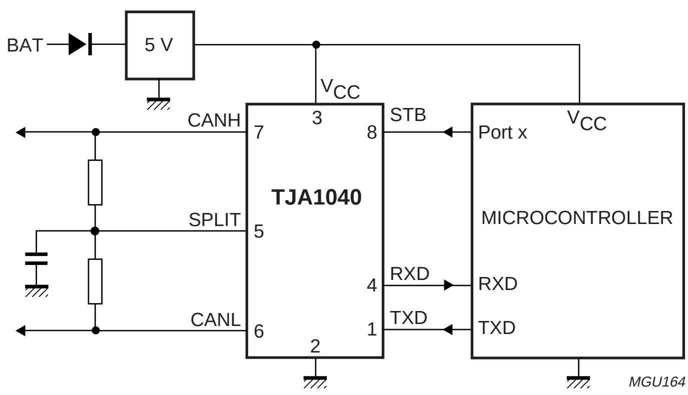
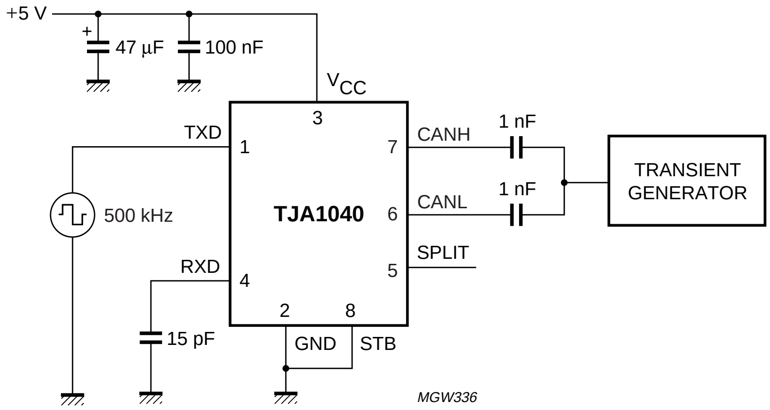


Fig.4 Typical application for 5 V microcontroller.



The waveforms of the applied transients will be in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, 3b, 5, 6 and 7.

Fig.5 Test circuit for automotive transients.

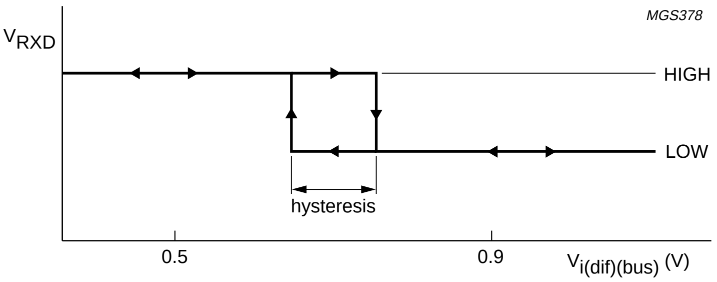


Fig.6 Hysteresis of the receiver.

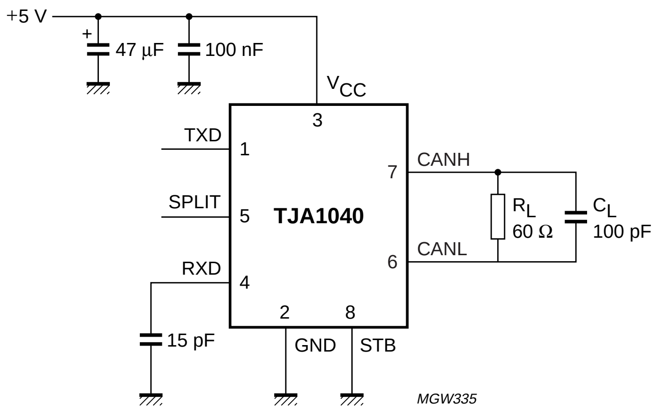
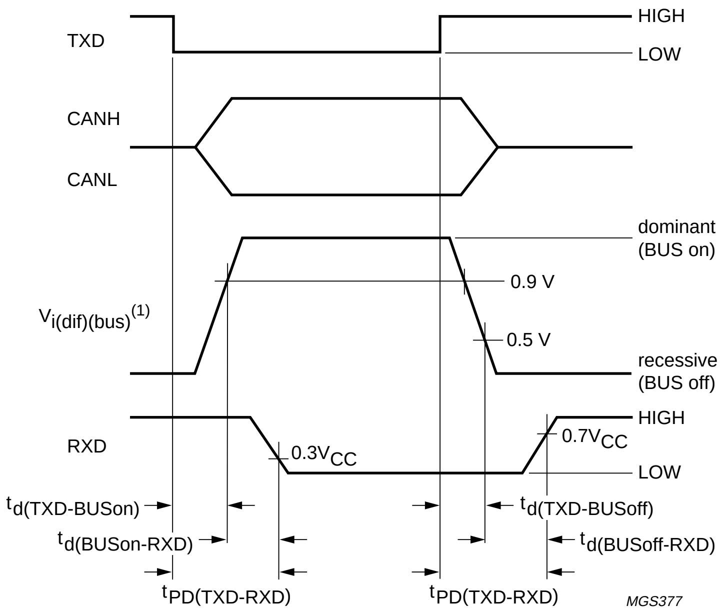


Fig.7 Test circuit for timing characteristics.

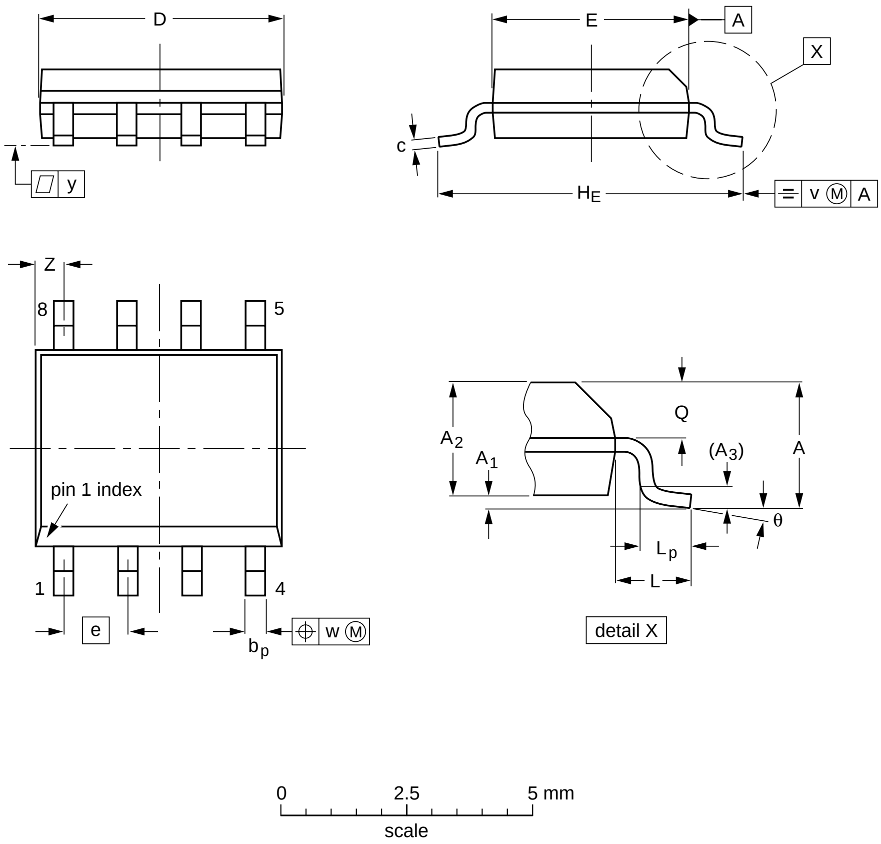


(1) $V_{i(dif)(bus)} = V_{CANH} - V_{CANL}$.

Fig.8 Timing diagram.

PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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