

DATA SHEET

TDA8566Q

**2 × 40 W/2 Ω stereo BTL car radio
power amplifier with differential
inputs and diagnostic outputs**

Product specification
Supersedes data of 1998 Sep 23
File under Integrated Circuits, IC01

2000 Jan 28

2 × 40 W/2 Ω stereo BTL car radio power amplifier with differential inputs and diagnostic outputs

TDA8566Q

FEATURES

- Differential inputs
- Very high Common Mode Rejection Ratio (CMRR)
- High common mode input signal handling
- Requires very few external components
- High output power
- 4 and 2 Ω load driving capability
- Low offset voltage at output
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature pre-warning)
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- Load dump protection
- Short-circuit proof to ground, to V_P and across the load

- Low power dissipation in any short-circuit condition
- Thermally protected
- Reverse polarity safe
- Protected against electrostatic discharge
- No switch-on/switch-off plop
- Flexible leads
- Low thermal resistance.

GENERAL DESCRIPTION

The TDA8566Q is an integrated class-B output amplifier contained in a 17-lead single-in-line (SIL; bent to DIL) plastic power package. The device contains 2 amplifiers in a Bridge-Tied Load configuration (BTL). The output power is 2 × 25 W in a 4 Ω load or 2 × 40 W in a 2 Ω load. It has a differential input stage and 2 diagnostic outputs. The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	operating supply voltage		6	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	7.5	A
$I_{q(tot)}$	total quiescent current		–	115	–	mA
I_{stb}	standby current		–	0.1	100	μA
I_{sw}	switch-on current		–	–	40	μA
Z_i	input impedance		100	120	–	kΩ
P_{out}	output power	$R_L = 4 \Omega$; THD = 10%	–	25	–	W
		$R_L = 2 \Omega$; THD = 10%	–	40	–	W
SVRR	supply voltage ripple rejection	$R_s = 0 \Omega$	–	60	–	dB
α_{cs}	channel separation	$R_s = 10 \text{ k}\Omega$	–	50	–	dB
CMRR	common mode rejection ratio		–	75	–	dB
G_v	closed loop voltage gain		25	26	27	dB
V_{no}	noise output voltage	$R_s = 0 \Omega$	–	–	120	μV
V_{os}	DC output offset voltage		–	–	100	mV

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8566Q	DBS17P	plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

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BLOCK DIAGRAM

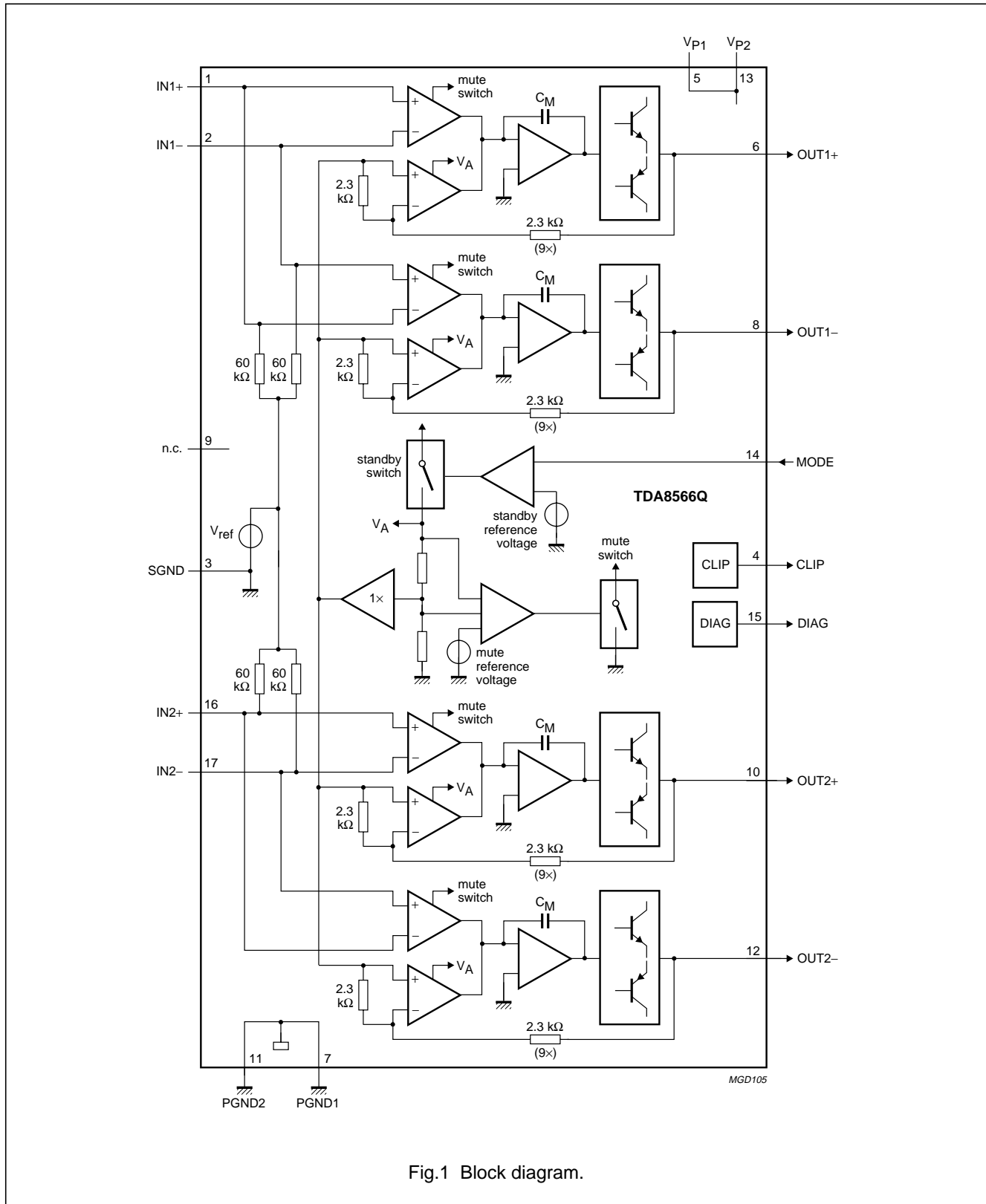


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
IN1+	1	channel 1 input positive
IN1-	2	channel 1 input negative
SGND	3	small signal ground
CLIP	4	clip detection
V _{P1}	5	supply voltage 1
OUT1+	6	channel 1 speaker output positive
PGND1	7	channel 1 negative power supply (ground)
OUT1-	8	channel 1 speaker output negative
n.c.	9	not connected
OUT2+	10	channel 2 speaker output positive
PGND2	11	channel 2 negative power supply (ground)
OUT2-	12	channel 2 speaker output negative
V _{P2}	13	supply voltage 2
MODE	14	mode select switch (standby/mute/operating)
DIAG	15	short-circuit and temperature pre-warning diagnostic
IN2+	16	channel 2 input positive
IN2-	17	channel 2 input negative

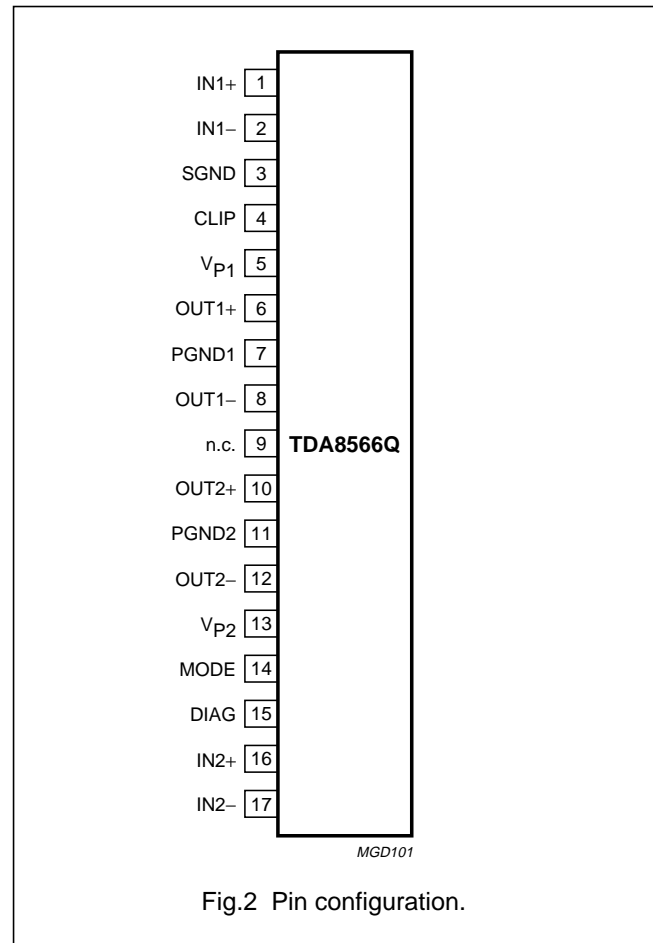


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8566Q contains 2 identical amplifiers and can be used for BTL applications. The gain of each amplifier is fixed at 26 dB. Special features of this device are:

1. Mode select switch
2. Clip detection
3. Short-circuit diagnostic
4. Temperature pre-warning
5. Open-collector outputs
6. Differential inputs.

Mode select switch (pin 14)

- Standby: low supply current (<100 μA)
- Mute: input signal suppressed
- Operating: normal on condition.

Since this pin has a very low input current (<40 μA), a low cost supply switch can be applied. To avoid switch-on plops, it is advisable to keep the amplifier in the mute mode for a period of ≥150 ms (charging the input capacitors at pins 1, 2, 16 and 17). This can be realized by microcontroller control or by an external timing circuit (see Fig.7).

Clip detection (pin 4)

When clipping occurs at one or more output stages, the dynamic distortion detector becomes active and pin 4 goes LOW. This information can be used to drive a sound processor or a DC volume control to attenuate the input signal and so limit the level of distortion. The output level of pin 4 is independent of the number of channels that are being clipped. The clip detection circuit is disabled in a short-circuit condition, so if a fault condition occurs at the outputs, pin 4 will remain at a HIGH level. The clip detection waveforms are illustrated in Fig.3.

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Short-circuit diagnostic (pin 15)

When a short-circuit occurs at one or more outputs to ground or to the supply voltage, the output stages are switched off until the short-circuit is removed and the device is switched on again (with a delay of approximately 20 ms after the removal of the short-circuit). During this short-circuit condition, pin 15 is continuously LOW.

When a short-circuit occurs across the load of one or both channels, the output stages are switched off for approximately 20 ms. After approximately 50 μs the load condition is again checked to see if the short-circuit is still present. Due to this duty cycle of 50 μs/20 ms the average current consumption during this short-circuit condition is very low (approximately 40 mA). During this short-circuit condition, pin 15 is LOW for 20 ms and HIGH for 50 μs (see Fig.4). The power dissipation in any short-circuit condition is very low.

Temperature pre-warning (pin 15)

When the junction temperature (T_{vj}) reaches 145 °C, pin 15 will become continuously LOW.

Open-collector outputs

Pins 4 and 15 are open-collector outputs, therefore more devices can be tied together. Pins 4 and 15 can also be tied together. An external pull-up resistor is required.

Differential inputs

The input stage is a high-impedance fully differential balanced input stage that is also capable of operating in a single-ended mode with one of the inputs capacitively coupled to an audio ground. It should be noted that if a source resistance is added (input voltage dividers) the CMRR degrades to lower values.

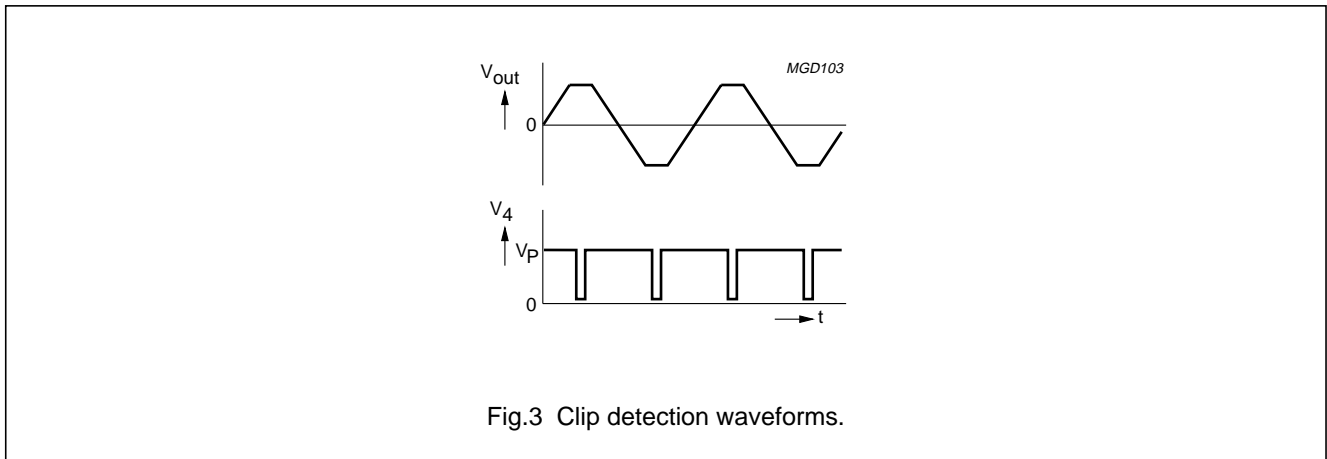


Fig.3 Clip detection waveforms.

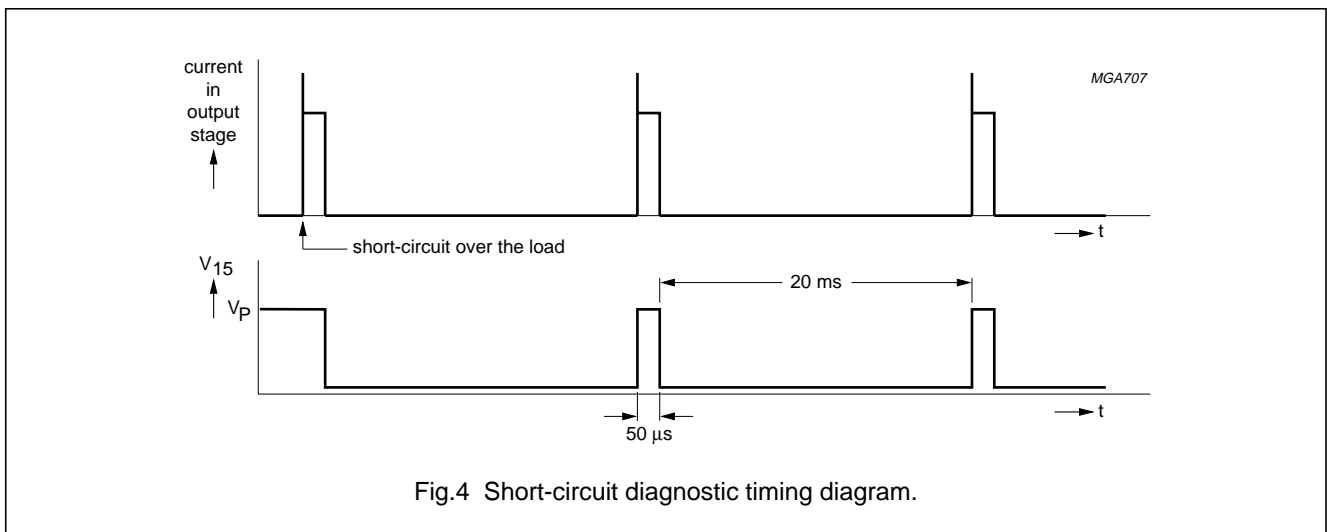


Fig.4 Short-circuit diagnostic timing diagram.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _P	supply voltage	operating	–	18	V
		non-operating	–	30	V
		during 50 ms; load dump protection t _{rise} ≥ 2.5 ms	–	45	V
I _{OSM}	non-repetitive peak output current		–	10	A
I _{ORM}	repetitive peak output current		–	7.5	A
T _{stg}	storage temperature		–55	+150	°C
T _{vj}	virtual junction temperature		–	150	°C
T _{amb}	ambient temperature		–40	+85	°C
V _{psc}	short-circuit safe voltage		–	18	V
V _{pr}	reverse polarity		–	6.0	V
P _{tot}	total power dissipation		–	60	W

QUALITY SPECIFICATION

Quality specification in accordance with “UZW-FQ-611-E”, if this type is used as an audio amplifier. The number of the quality specification can be found in the “Quality Reference Handbook”. The handbook can be ordered using the code 9397 750 00192.

THERMAL CHARACTERISTICS

Thermal characteristics in accordance with (IEC 747-1).

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-c)}	thermal resistance from junction to case		1.3	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	40	K/W

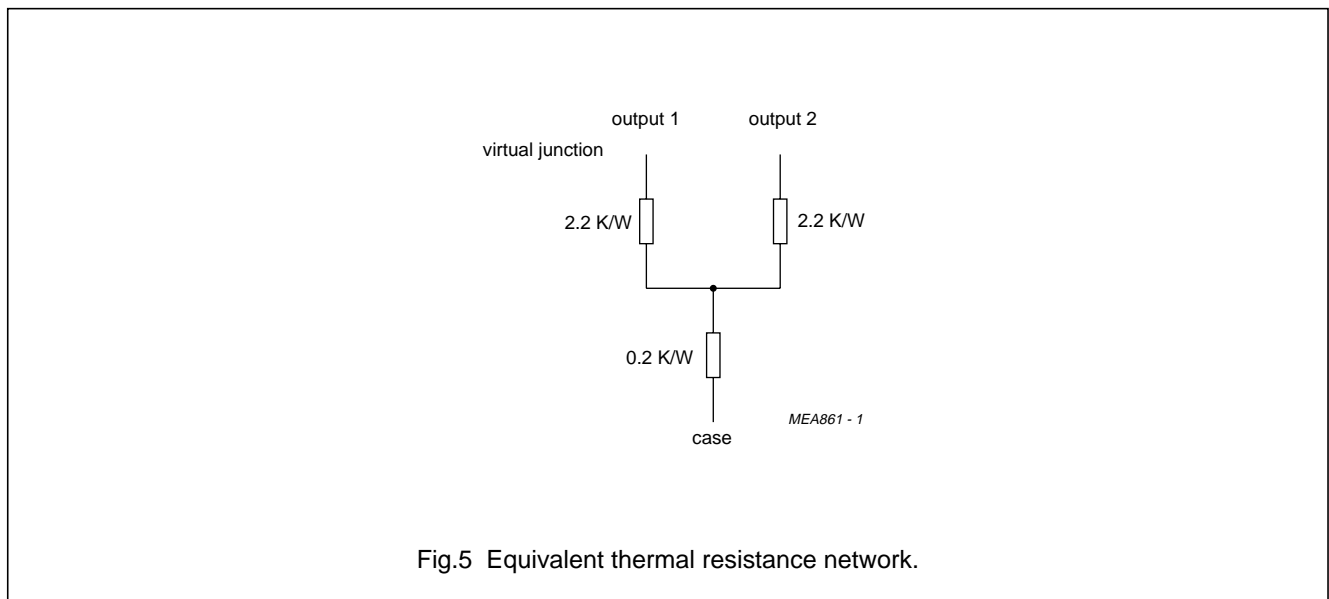


Fig.5 Equivalent thermal resistance network.

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DC CHARACTERISTICS

$V_P = 14.4$ V; $T_{amb} = 25$ °C; measured in test circuit of Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage						
V_P	supply voltage	note 1	6	14.4	18	V
I_q	quiescent current	$R_L = \infty$	–	115	180	mA
Operating condition						
$V_{ms(op)}$	mode select switch level		8.5	–	V_P	V
I_{14}	mode select switch current	$V_{14} = 14.4$ V	–	15	40	μA
V_o	output voltage	note 2	–	7.0	–	V
V_{os}	output offset voltage		–	–	100	mV
Mute condition						
$V_{ms(mute)}$	mode select switch level		3.3	–	6.4	V
V_o	output voltage	note 2	–	7.0	–	V
V_{os}	output offset voltage		–	–	100	mV
Standby condition						
$V_{ms(stb)}$	mode select switch level		0	–	2	V
I_{stb}	standby current		–	0.1	100	μA
Diagnostic						
V_{15}	diagnostic output voltage	during any fault condition	–	–	0.6	V
T_{vj}	temperature pre-warning	$V_{15} = 0.6$ V	–	145	–	°C

Notes

1. The circuit is DC adjusted at $V_P = 6$ to 18 V and AC operating at $V_P = 8.5$ to 18 V.
2. At $V_P = 18$ to 30 V the DC output voltage $\leq 0.5 V_P$.

AC CHARACTERISTICS

$V_P = 14.4$ V; $T_{amb} = 25$ °C; $R_L = 2$ Ω; $f_i = 1$ kHz; measured in test circuit of Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_{out}	output power	THD = 0.5%	25	30	–	W
		THD = 10%	33	40	–	W
		THD = 30%	45	55	–	W
		$V_P = 13.5$ V; THD = 0.5%	–	25	–	W
		$V_P = 13.5$ V; THD = 10%	–	35	–	W
		THD = 0.5%; $R_L = 4$ Ω	16	19	–	W
		THD = 10%; $R_L = 4$ Ω	21	25	–	W
		THD = 30%; $R_L = 4$ Ω	28	35	–	W
		$V_P = 13.5$ V; THD = 0.5%; $R_L = 4$ Ω	–	14	–	W
		$V_P = 13.5$ V; THD = 10%; $R_L = 4$ Ω	–	22	–	W

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion	$P_{out} = 1\text{ W}$	–	0.1	–	%
		note 3; $V_4 = 0.6\text{ V}$	–	8	–	%
		$P_{out} = 1\text{ W}; R_L = 4\ \Omega$	–	0.05	–	%
B	power bandwidth	THD = 0.5%; $P_{out} = -1\text{ dB}$ with respect to 25 W	–	20 to 20000	–	Hz
f_l	low frequency roll off	-1 dB; note 1	–	25	–	Hz
f_h	high frequency roll off	-1 dB	20	–	–	kHz
G_v	closed loop voltage gain		25	26	27	dB
SVRR	supply voltage ripple rejection	on; note 2	50	–	–	dB
		mute; note 2	50	–	–	dB
		standby; note 2	80	–	–	dB
Z_i	input impedance	differential	100	120	150	kΩ
		single-ended	50	60	75	kΩ
$ \Delta Z_i $	input impedance mismatch		–	2	–	%
V_{no}	noise output voltage	on; B = 20 Hz to 20 kHz; $R_s = 0\ \Omega$	–	85	120	μV
		on; B = 20 Hz to 20 kHz; $R_s = 10\text{ k}\Omega$	–	100	–	μV
		mute; B = 20 Hz to 20 kHz; independent of R_s	–	60	–	μV
α_{cs}	channel separation	$P_{out} = 25\text{ W}; R_s = 10\text{ k}\Omega$	45	–	–	dB
$ \Delta G_v $	channel unbalance		–	–	1	dB
V_o	output signal voltage in mute	$V_i = V_{i(max)} = 1\text{ V (RMS)}$	–	–	2	mV
CMRR	common mode rejection ratio	$R_s = 0\ \Omega$; note 4	60	75	–	dB
		$R_s = 45\text{ k}\Omega$; note 5	40	–	–	dB

Notes

1. Frequency response externally fixed.
2. $V_{ripple} = V_{ripple(max)} = 2\text{ V (p-p)}$; $R_s = 0\ \Omega$.
3. Dynamic Distortion Detector (DDD) active; pin 4 is LOW.
4. Common mode rejection ratio measured at the output (over R_L) with both inputs tied together;
 $V_{common} \leq 3.5\text{ V (RMS)}$; $f = 100\text{ Hz to }10\text{ kHz}$; $R_s = 0\ \Omega$.
5. Common mode rejection ratio measured at the output (over R_L) with both inputs tied together;
 $V_{common} \leq 3.5\text{ V (RMS)}$; $f = 1\text{ kHz}$; $R_s = 45\text{ k}\Omega$. The mismatch of the input coupling capacitors is excluded.

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TEST AND APPLICATION INFORMATION

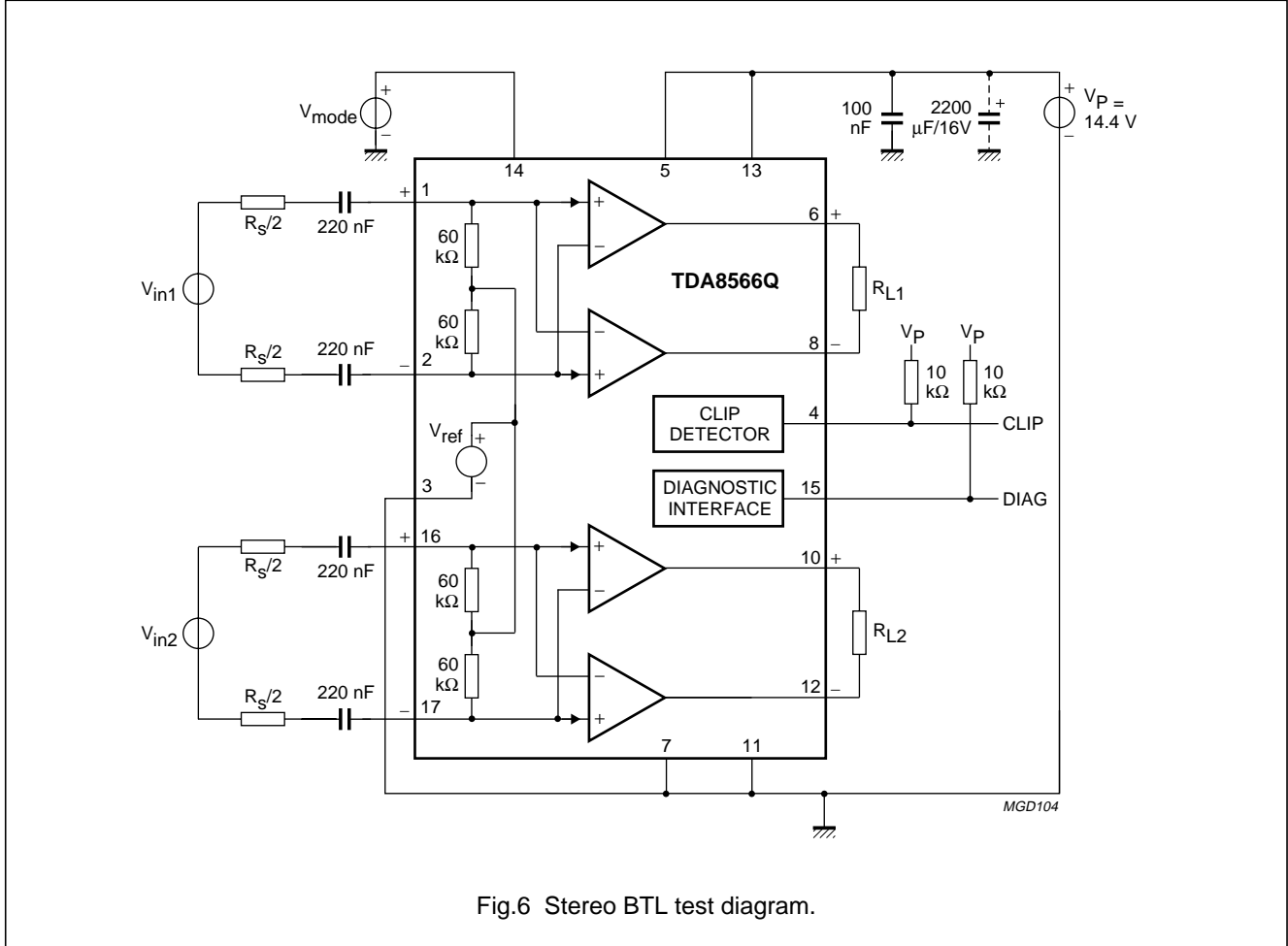


Fig.6 Stereo BTL test diagram.

Application notes

DIAGNOSTIC OUTPUT

Special care must be taken in the PCB layout to separate pin 4 from pins 1, 2, 16 and 17 to minimize the crosstalk between the CLIP output and the inputs.

MODE SELECT SWITCH

To avoid switch-on plops, it is advisable to keep the amplifier in the mute mode during ≥ 150 ms (charging of the input capacitors at pins 1, 2, 16 and 17). The circuit in Fig.7 slowly ramps-up the voltage at the mode select switch pin when switching on and results in fast muting when switching off.

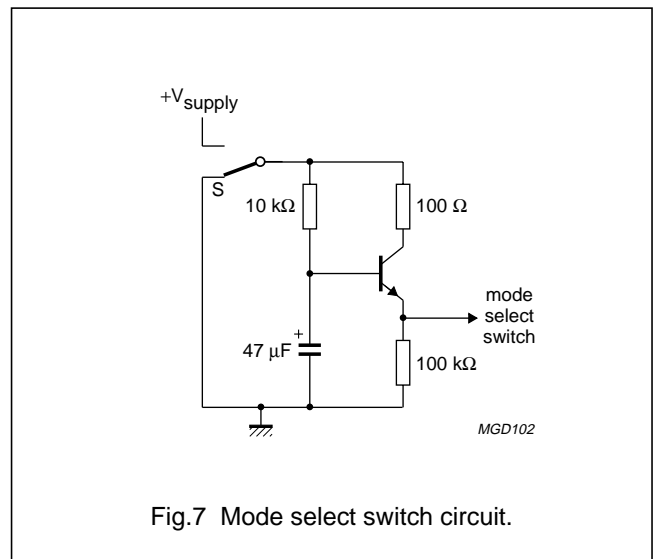


Fig.7 Mode select switch circuit.

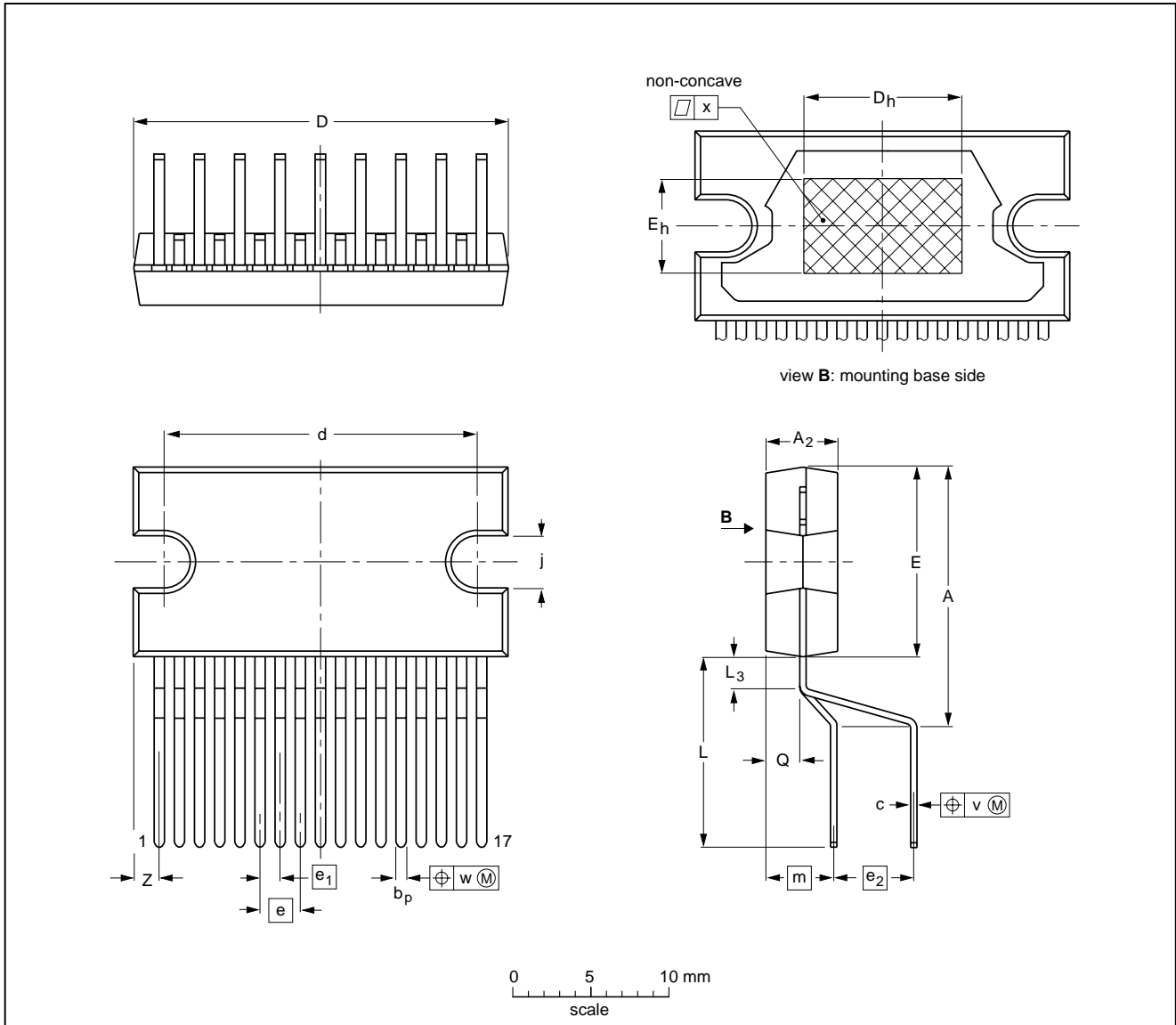
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PACKAGE OUTLINE

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)

SOT243-1



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₂	b _p	c	D ⁽¹⁾	d	D _h	E ⁽¹⁾	e	e ₁	e ₂	E _h	j	L	L ₃	m	Q	v	w	x	Z ⁽¹⁾
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT243-1						97-12-16 99-12-17

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SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable ⁽¹⁾

Note

- For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

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Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

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Tel. +381 11 3341 299, Fax.+381 11 3342 553

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Printed in The Netherlands

753503/25/04/pp12

Date of release: 2000 Jan 28

Document order number: 9397 750 06608

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