



TDA7565

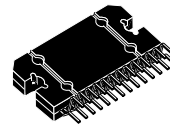
QUAD POWER AMPLIFIER WITH BUILT-IN VOLTAGE CONVERTER

PRODUCT PREVIEW

- DMOS POWER OUTPUT
- NON-SWITCHING HI-EFFICIENCY AMPLIFIER
- SWITCHING HIGH EFFICIENCY VOLTAGE CONVERTER
- HIGH OUTPUT POWER CAPABILITY 4x60W EIAJ/4Ω
- FULL I²C BUS DRIVING:
 - ST-BY
 - INDEPENDENT FRONT/REAR SOFT PLAY/MUTE
 - SELECTABLE GAIN 26dB - 12dB (FOR LOW NOISE LINE OUTPUT FUNCTION)
 - HIGH EFFICIENCY ENABLE/DISABLE
 - VOLTAGE CONVERTER ENABLE/DISABLE
 - REGULATED VOLTAGE SELECTION
 - SWITCHING FREQUENCY SELECTION
- HARDWARE MUTE FUNCTION
- FULL FAULT PROTECTION
- DC OFFSET DETECTION
- FOUR INDEPENDENT SHORT CIRCUIT PROTECTION
- CLIPPING DETECTOR WITH SELECTABLE THRESHOLD (1%/10%) VIA I²C BUS

MULTIPOWER BCD TECHNOLOGY

MOSFET OUTPUT POWER STAGE



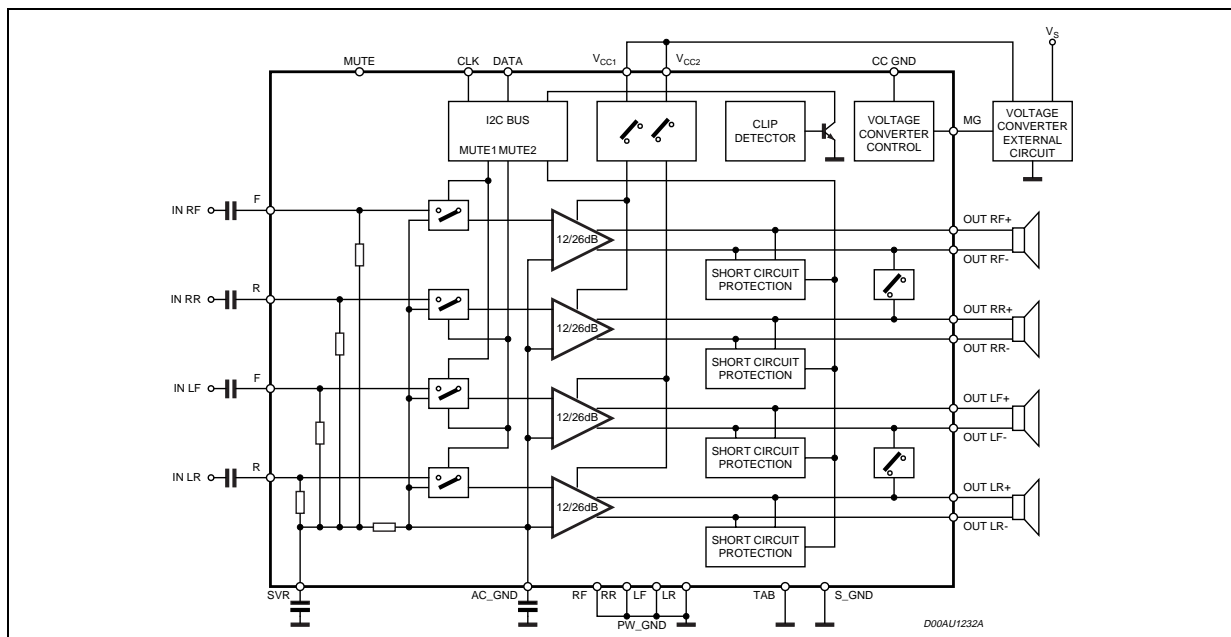
FLEXIWATT27

ORDERING NUMBER: TDA7565

DESCRIPTION

The TDA7565 is a new BCD technology QUAD BRIDGE type of car radio amplifier in Flexiwatt27 package specially intended for car radio applications. Thanks to the DMOS output stage the TDA7565 has a very low distortion allowing a clear powerful sound. The built-in voltage converter control block assures a very high output power with an extremely low number of added components. The dissipated power under average listening condition is aligned to the conventional solutions (4x40W).

BLOCK DIAGRAM



TDA7565

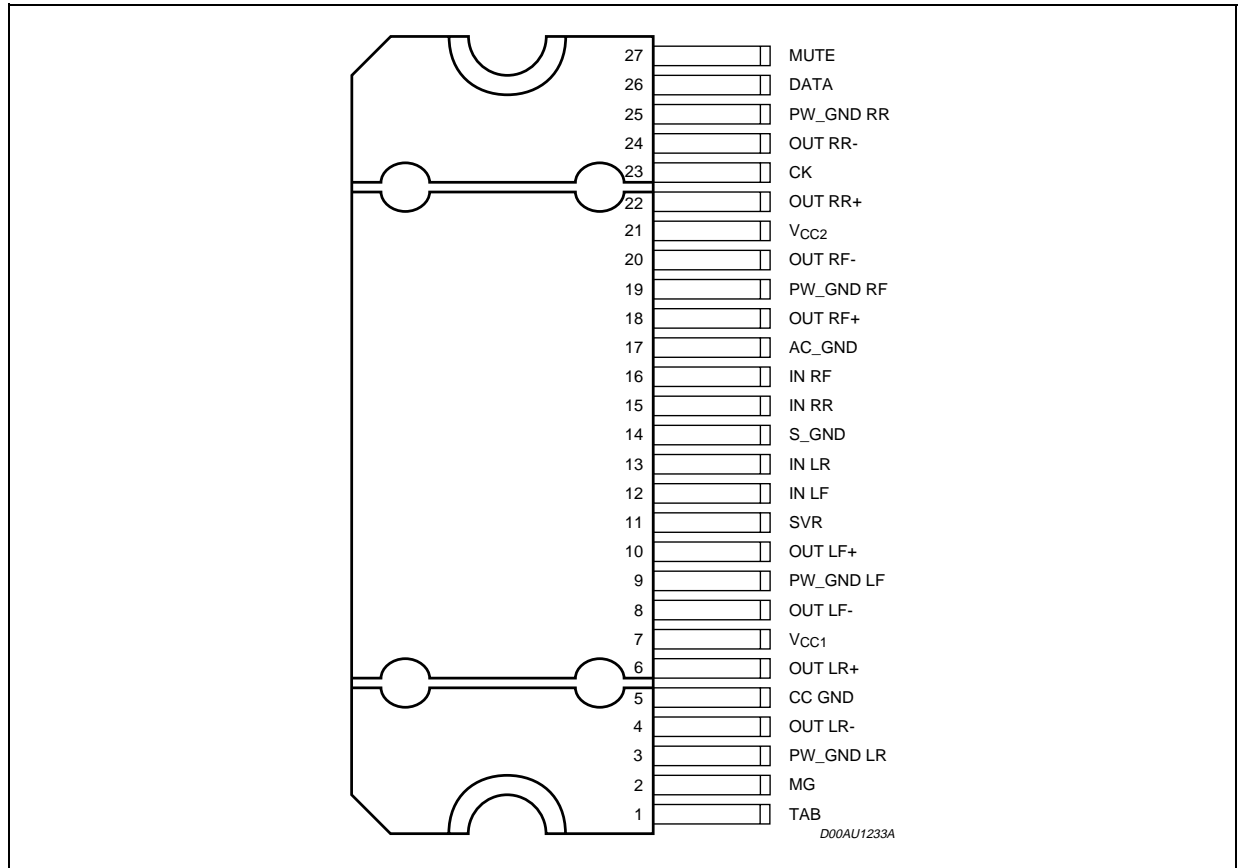
ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------------------------------|--|------------|------|
| V _{opc OFF} | Operating Supply Voltage , converter OFF | 18 | V |
| V _{opc ON} | Operating Supply Voltage , converter ON | 25 | V |
| V _S | DC Supply Voltage | 28 | V |
| V _{peak} | Peak Supply Voltage (for t = 50ms) | 50 | V |
| V _{CK} | CK pin Voltage | 6 | V |
| V _{DATA} | Data Pin Voltage | 6 | V |
| I _O | Output Peak Current (not repetitive t = 100μs) | 8 | A |
| I _O | Output Peak Current (repetitive f > 10Hz) | 6 | A |
| P _{tot} | Power Dissipation T _{case} = 70°C | 80 | W |
| T _{stg} , T _j | Storage and Junction Temperature | -55 to 150 | °C |

THERMAL DATA

| Symbol | Description | Value | Unit |
|------------------------|----------------------------------|--------|------|
| R _{th j-case} | Thermal Resistance Junction-case | Max. 1 | °C/W |

PIN CONNECTION



ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, $V_S = 13.5V$; $R_L = 4\Omega$; $f = 1KHz$; Voltage converter Disabled (V_{COff}); $T_{amb} = 25^\circ C$; unless otherwise specified.)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|-------------------------------------|---|--|-----------|---------------------|-----------|-------------|
| POWER AMPLIFIER | | | | | | |
| V_S | Supply Voltage Range | | 8 | | 18 | V |
| I_d | Total Quiescent Drain Current | | | 180 | 300 | mA |
| I_d | Total Quiescent Drain Current (V_{COn}) | | | TBD | | mA |
| P_O | Output Power (V_{COff}) $V = 14.4V$ | EIAJ ($V_S = 13.7V$) | | 35 | | W |
| | | THD = 10% | | 25 | | W |
| | | THD = 1% | | 20 | | W |
| P_O | Output Power (V_{COn}) $V = 14.4V$ | EIAJ ($V_S = 13.7V$) | | 60 | | W |
| | | THD = 10% | | 40 | | W |
| | | THD = 1% | | 31 | | W |
| THD | Total Harmonic Distortion | $P_O = 1W$ to $12W$; STDMODE HE MODE; $P_O = 1-2W$ HE MODE; $P_O = 4-12W$ | | 0.03 0.03 0.1 | 0.1 | % % % |
| | | $P_O = 1-12W$, $f = 10kHz$ | | 0.15 | 0.5 | % |
| | | | | | | |
| C_T | Cross Talk | $f = 1KHz$ to $10KHz$, $R_G = 600\Omega$ | 50 | 55 | | dB |
| R_{IN} | Input Impedance | | 60 | 100 | 130 | K Ω |
| G_{V1} | Voltage Gain 1 | | 25.5 | 26 | 26.5 | dB |
| ΔG_{V1} | Voltage Gain Match 1 | | -1 | | 1 | dB |
| G_{V2} | Voltage Gain 2 | | 11.5 | 12 | 12.5 | dB |
| ΔG_{V2} | Voltage Gain Match 2 | | -1 | | 1 | dB |
| E_{IN1} | Output Noise Voltage 1 | $R_g = 600\Omega$; $G_V = 26dB$ filter 20Hz to 22kHz | | 60 | 100 | μV |
| E_{IN2} | Output Noise Voltage 2 | $R_g = 600\Omega$; $G_V = 26dB$ filter 20Hz to 12kHz | | 15 | 20 | μV |
| SVR | Supply Voltage Rejection | $f = 100Hz$ to $10kHz$; $V_r = 1Vpk$; $R_g = 600\Omega$ | 50 | 60 | | dB |
| BW | Power Bandwidth | (-3dB) | 75 | | | KHz |
| A_{SB} | Stand-by Attenuation | | 70 | 100 | | dB |
| I_{SB} | Stand-by Current | | | | 100 | μA |
| A_M | Mute Attenuation | | 70 | 90 | | dB |
| V_{OS} | Offset Voltage | Mute & Play | -100 | | 100 | mV |
| V_{AM} | Min. Supply Voltage Threshold | | 6.5 | 7 | 7.5 | V |
| | Slew Rate | | 1.5 | | | V/ μs |
| T_{ON} | Turn on Delay | D2/D1 (IB1) 0 to 1 | | 10 | 20 | ms |
| T_{OFF} | Turn off Delay | D2/D1 (IB1) 1 to 0 | | 10 | 20 | ms |
| | Thermal Foldback Junction Temperature | | 155 | 170 | 185 | $^\circ C$ |
| CD _{THD} | Clip Det THD level | D0 (IB1) = 0 | 0 | 1 | 2 | % |
| | | D0 (IB1) = 1 | 5 | 10 | 15 | % |
| V_O | Offset Detection | Power Amplifier = play AC Input = 0 | ± 1.5 | ± 2 | ± 2.5 | V |
| T_{hw} | Thermal Warning | | | 165 | | $^\circ C$ |
| I²C BUS INTERFACE | | | | | | |
| f_{SCL} | Clock Frequency | | | | 400 | KHz |
| V_{IL} | Input Low Voltage | | | | 1.5 | V |
| V_{IH} | Input High Voltage | | 2.3 | | | V |

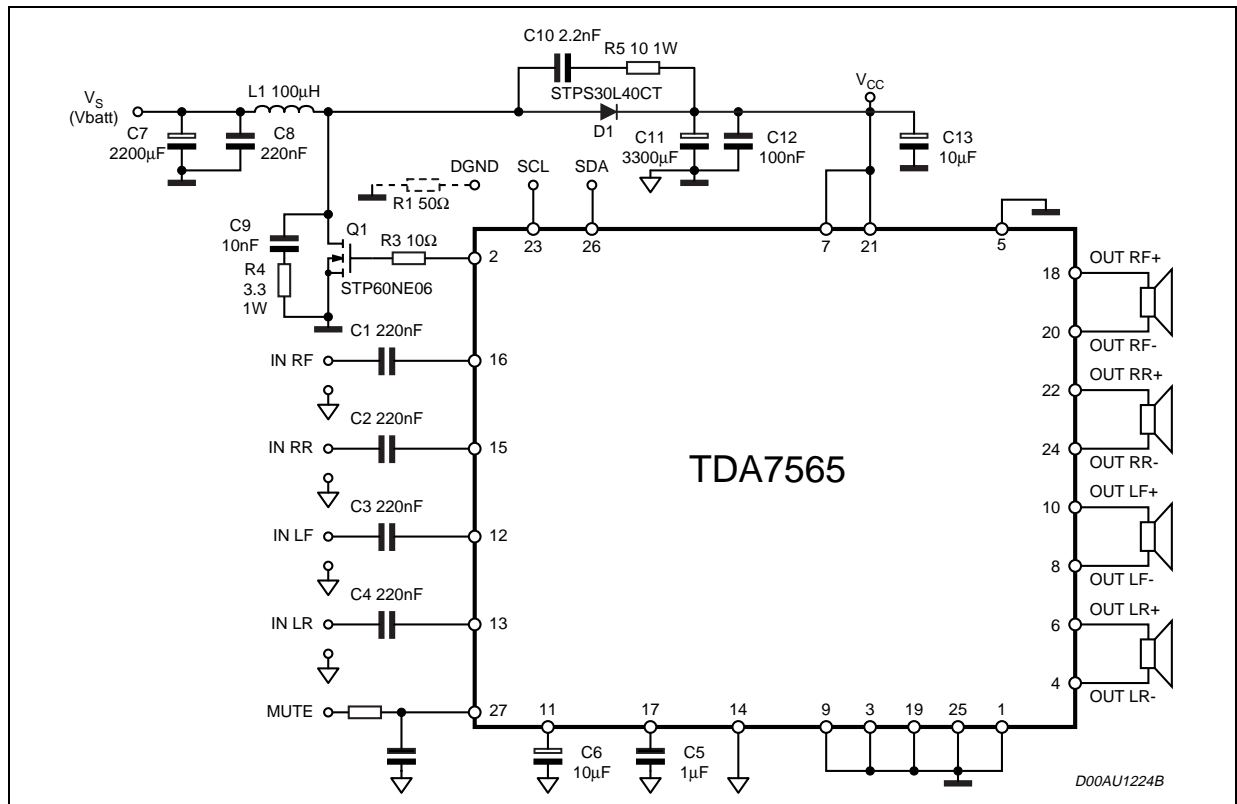
TDA7565

ELECTRICAL CHARACTERISTICS (continua)

(Refer to the test circuit, $V_S = 13.5V$; $R_L = 4\Omega$; $f = 1KHz$; Voltage converter Disabled (V_{Coff}); $T_{amb} = 25^\circ C$; unless otherwise specified.)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|----------------------|---|---|------|----------------------------|------|--------------------------|
| $V_{Min}(pin27)$ | Mute in Threshold Voltage | Amp. Mute | | | 1.5 | V |
| $V_{Mout}(pin27)$ | Mute out Threshold Voltage | | 3.5 | | | V |
| $AM(pin 27)$ | Mute Attenuation | | 80 | 90 | | |
| VOLTAGE CONVERTER | | | | | | |
| V_{cc1}, V_{cc2} | Converter Output Voltage (VC = ON) | $V_S = 14V$ D3 (IB2) = 0; D6 (IB2) = 0 D3 (IB2) = 1; D6 (IB2) = 0 D3 (IB2) = 0; D6 (IB2) = 1 D3 (IB2) = 1; D6 (IB2) = 1 | | 15 16.5 17.5 18.5 | | V V V V |
| F_s | Voltage Converter Switching Frequency | D6 (IB1) = 0; D7 (IB1) = 0 D6 (IB1) = 1; D7 (IB1) = 0 D6 (IB1) = 0; D7 (IB1) = 1 D6 (IB1) = 1; D7 (IB1) = 1 | | 100 150 260 400 | | kHz kHz kHz kHz |
| V_{mgl} | Mos Gate Output Low Voltage | $I_o = 250mA$ | | | 1 | V |
| V_{mgh} | Mos Gate Output High Voltage | $I_o = 20mA$ | | 10.5 | | V |
| | | $I_o = 200mA$ | | 10 | | V |
| $V_{mgclamp}$ | Mos Gate Output Clamp Voltage | $I_o = 5mA$ | | TBD | | V |
| t_f | Fall Time | $C_o = 1nF$ | | 20 | | ns |
| t_r | Rise Time | $C_o = 1nF$ | | 50 | | ns |
| $V_{mgl} (V_{Coff})$ | Mos Gate Output Voltage with Voltage Converter Disabled | $I_o = 5mA$ | | | 0.5 | V |

Figure 1. Demoboard Schematic



I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7565 and viceversa takes place through the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

Data Validity

As shown by fig. 2, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

As shown by fig. 3 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

Byte Format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

The transmitter* puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 22). The receiver** the acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

* Transmitter

- master (μ P) when it writes an address to the TDA7565
- slave (TDA7565) when the μ P reads a data byte from TDA7565

** Receiver

- slave (TDA7565) when the μ P writes an address to the TDA7565
- master (μ P) when it reads a data byte from TDA7565

Figure 2. Data Validity on the I²C BUS

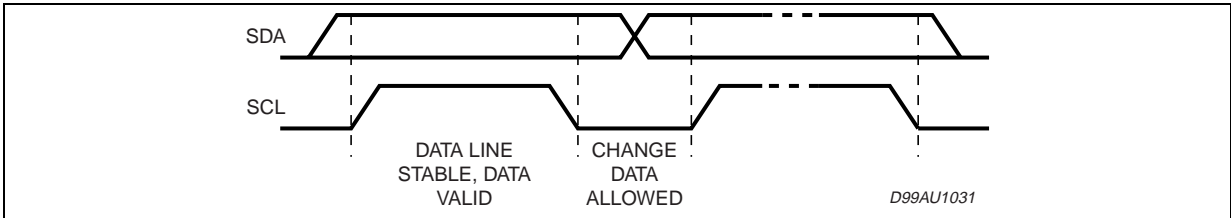


Figure 3.

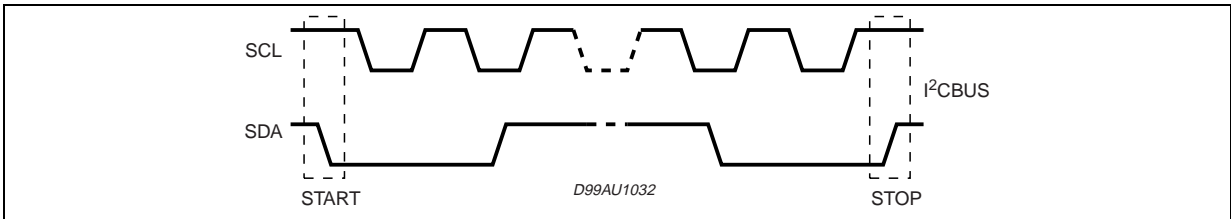
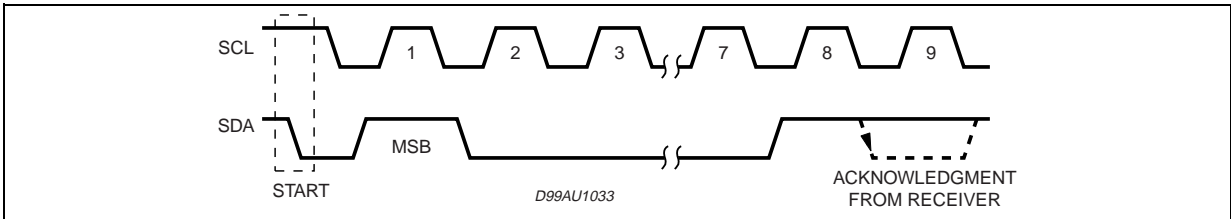


Figure 4.



SOFTWARE SPECIFICATIONS

All the functions of the TDA7565 are activated by I²C interface.

The bit 0 of the "ADDRESS BYTE" defines if the next bytes are write instruction (from μ P to TDA7565) or read instruction (from TDA7565 to μ P).

| | |
|----------------|---|
| D7 | Address bit |
| D6 | Address bit |
| D5 | Address bit |
| D4 | Address bit |
| D3 | Address bit |
| D2 | Address bit |
| D1 | Address bit |
| D0(R/W) | Read/Write bit 0 = Write instruction 1 = read instruction |

If R/W = 0, the μ P sends 2 "Instruction Bytes": IB1 and IB2.

IB1

| | |
|-----------|---|
| D7 | Sel Freq Switch 1 |
| D6 | Sel Freq Switch 2 |
| D5 | Offset Detection start (D5 = 1) Offset Detection stop (D5 = 0) (off) |
| D4 | Front Channel Gain = 26dB (D4 = 0) Gain = 12dB (D4 = 1) |
| D3 | Rear Channel Gain = 26dB (D3 = 0) Gain = 12dB (D3 = 1) |
| D2 | Mute front channels (D2 = 0) Unmute front channels (D2 = 1) |
| D1 | Mute rear channels (D1 = 0) Unmute rear channels (D1 = 1) |
| D0 | CD 1% (D0 = 0) CD 10% (D0 = 1) |

IB2

| | |
|-----------|---|
| D7 | Voltage Converter Enabled (D7 = 1) Voltage Converter Disabled (D7 = 0) |
| D6 | Regulated voltage selection 1 |
| D5 | Test Speed |
| D4 | Stand-by on - Amplifier not working - (D4 = 0) Stand-by off - Amplifier working - (D4 = 1) |
| D3 | Regulated voltage selection 0) |
| D2 | To be forced to "Level 1" |
| D1 | Right Channel Power amplifier working in standard mode (D1 = 0) Power amplifier working in HiEff mode(D1 = 1) |
| D0 | Left Channel Power amplifier working in standard mode (D0 = 0) Power amplifier working in HiEff mode(D0 = 1) |

DB1

| | |
|-----------|--------------------------------|
| D7 | Thermal Warning |
| D6 | X |
| D5 | X |
| D4 | X |
| D3 | X |
| D2 | Offset (LF) |
| D1 | Short Circuit Protection (CH1) |
| D0 | X |

DB2

| | |
|-----------|--------------------------------|
| D7 | Off Status |
| D6 | X |
| D5 | Clip Detector Output |
| D4 | X |
| D3 | X |
| D2 | Offset (LR) |
| D1 | Short Circuit Protection (CH2) |
| D0 | X |

DB3

| | |
|-----------|--------------------------------|
| D7 | St-By Status |
| D6 | X |
| D5 | X |
| D4 | X |
| D3 | X |
| D2 | Offset (RF) |
| D1 | Short Circuit Protection (CH3) |
| D0 | X |

DB4

| | |
|-----------|--------------------------------|
| D7 | X |
| D6 | X |
| D5 | X |
| D4 | X |
| D3 | X |
| D2 | Offset (RR) |
| D1 | Short Circuit Protection (CH4) |
| D0 | X |

Examples of bytes sequence

1 - Turn-On of the power amplifier with 26dB gain, mute on, diagnostic defeat, HighEff mode, voltage converter disabled.

| | | | | | | | |
|-------|--------------------------|-----|----------|-----|----------|-----|------|
| Start | Address byte with D0 = 0 | ACK | IB1 | ACK | IB2 | ACK | STOP |
| | | | XX00X000 | | 0XX1XX10 | | |

2 - Turn-Off of the power amplifier

| | | | | | | | |
|-------|--------------------------|-----|----------|-----|----------|-----|------|
| Start | Address byte with D0 = 0 | ACK | IB1 | ACK | IB2 | ACK | STOP |
| | | | XXXXXXXX | | XXX0XXX0 | | |

4 - Offset detection procedure start

| | | | | | | | |
|-------|--------------------------|-----|----------|-----|----------|-----|------|
| Start | Address byte with D0 = 0 | ACK | IB1 | ACK | IB2 | ACK | STOP |
| | | | XX1XX11X | | XXX1XXX0 | | |

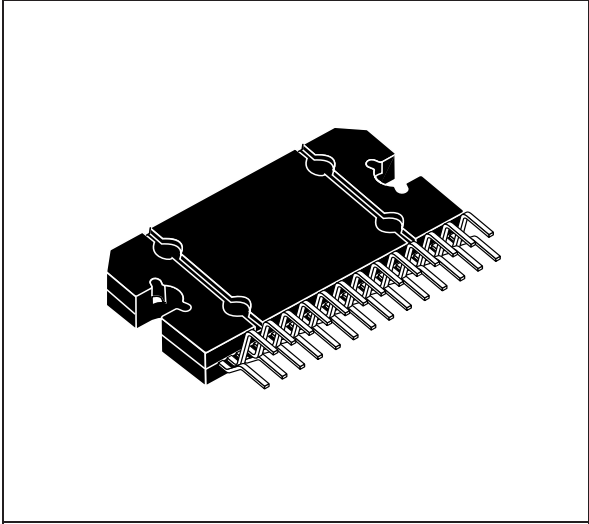
4 - Offset detection procedure stop and reading operation.

| | | | | |
|-------|--------------------------|-----|-----|------|
| Start | Address byte with D0 = 1 | ACK | DB1 | STOP |
|-------|--------------------------|-----|-----|------|

- The purpose of this test is to check if a D.C. offset (2V typ.) is present on the outputs, produced by input capacitor with anomalous leakage current or humidity between pins.
- The delay from 3 to 4 can be selected by software, starting from T.B.D. ms

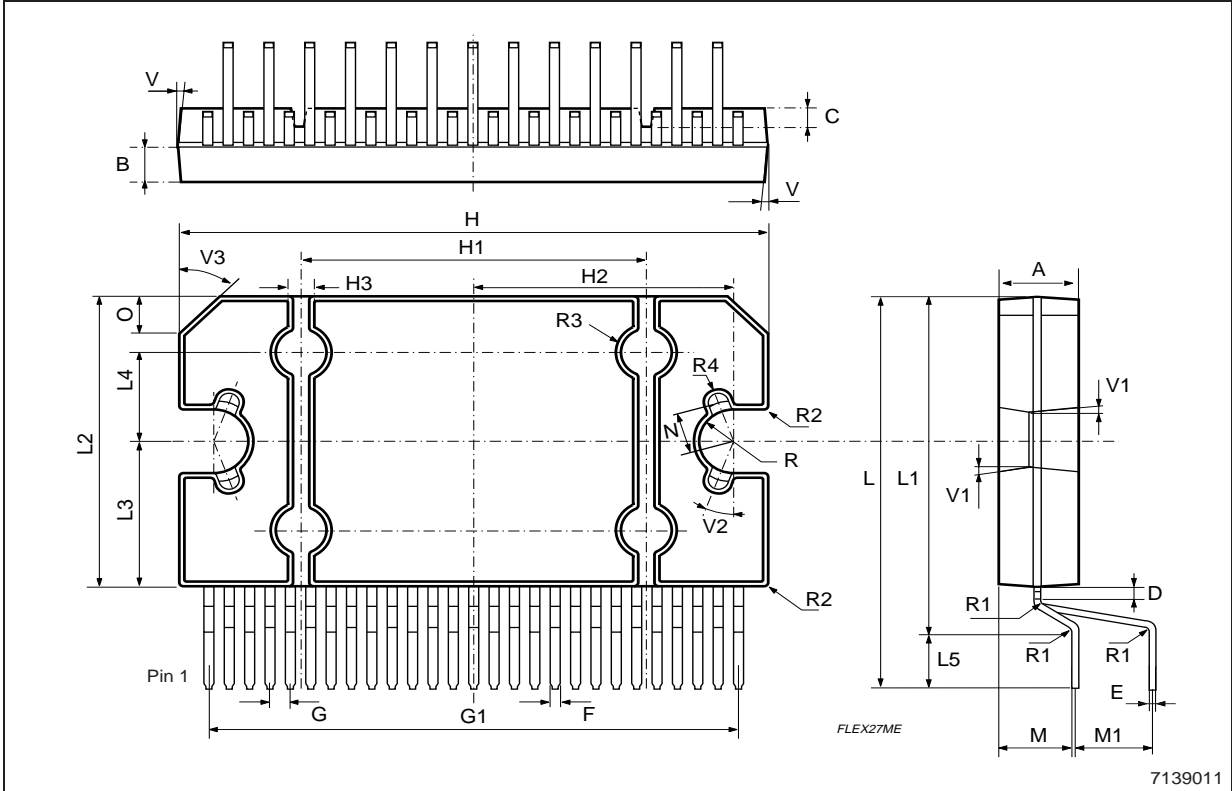
| DIM. | mm | | | inch | | |
|--------|-------|-------|------------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | 4.45 | 4.50 | 4.65 | 0.175 | 0.177 | 0.183 |
| B | 1.80 | 1.90 | 2.00 | 0.070 | 0.074 | 0.079 |
| C | | 1.40 | | | 0.055 | |
| D | 0.75 | 0.90 | 1.05 | 0.029 | 0.035 | 0.041 |
| E | 0.37 | 0.39 | 0.42 | 0.014 | 0.015 | 0.016 |
| F (1) | | | 0.57 | | | 0.022 |
| G | 0.80 | 1.00 | 1.20 | 0.031 | 0.040 | 0.047 |
| G1 | 25.75 | 26.00 | 26.25 | 1.014 | 1.023 | 1.033 |
| H (2) | 28.90 | 29.23 | 29.30 | 1.139 | 1.150 | 1.153 |
| H1 | | 17.00 | | | 0.669 | |
| H2 | | 12.80 | | | 0.503 | |
| H3 | | 0.80 | | | 0.031 | |
| L (2) | 22.07 | 22.47 | 22.87 | 0.869 | 0.884 | 0.904 |
| L1 | 18.57 | 18.97 | 19.37 | 0.731 | 0.747 | 0.762 |
| L2 (2) | 15.50 | 15.70 | 15.90 | 0.610 | 0.618 | 0.626 |
| L3 | 7.70 | 7.85 | 7.95 | 0.303 | 0.309 | 0.313 |
| L4 | | 5 | | | 0.197 | |
| L5 | | 3.5 | | | 0.138 | |
| M | 3.70 | 4.00 | 4.30 | 0.145 | 0.157 | 0.169 |
| M1 | 3.60 | 4.00 | 4.40 | 0.142 | 0.157 | 0.173 |
| N | | 2.20 | | | 0.086 | |
| O | | 2 | | | 0.079 | |
| R | | 1.70 | | | 0.067 | |
| R1 | | 0.5 | | | 0.02 | |
| R2 | | 0.3 | | | 0.12 | |
| R3 | | 1.25 | | | 0.049 | |
| R4 | | 0.50 | | | 0.019 | |
| V | | | 5° (Typ.) | | | |
| V1 | | | 3° (Typ.) | | | |
| V2 | | | 20° (Typ.) | | | |
| V3 | | | 45° (Typ.) | | | |

OUTLINE AND MECHANICAL DATA



Flexiwatt27 (vertical)

(1): dam-bar protusion not included
 (2): molding protusion included



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