STW77N65M5

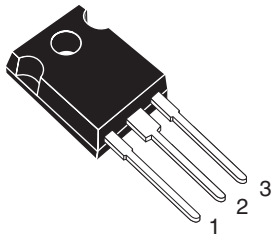
N-channel 650 V, 0.033 Ω, 66 A, MDmesh™ V Power MOSFET TO-247

Preliminary Data

Features

Type	V_{DSS} @T_{jMAX}	$R_{DS(on)}$ max	I_D
STW77N65M5	710 V	< 0.038 Ω	66 A

- TO-247 worldwide best $R_{DS(on)}$
- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested



TO-247

Application

- Switching applications

Description

MDmesh V is a revolutionary Power MOSFET technology, which combines an innovative proprietary vertical process with the well known company`s PowerMESH™ horizontal layout. The resulting product has an extremely low on-resistance, unmatched among silicon-based Power MOSFETs, making it especially suited for applications which require superior power density and outstanding efficiencies.

Figure 1. Internal schematic diagram

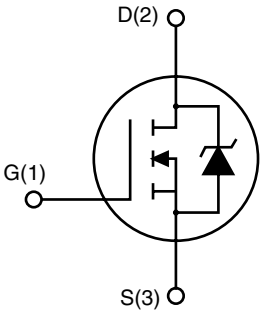


Table 1. Device summary

Order codes	Marking	Package	Packaging
STW77N65M5	77N65M5	TO-247	Tube

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	25	V
I_D	Drain current (continuous) at T_C = 25 °C	66	A
I_D	Drain current (continuous) at T_C = 100 °C	41.5	A
I_{DM} (1)	Drain current (pulsed)	264	A
P_{TOT}	Total dissipation at T_C = 25 °C	400	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	TBD	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, I_D = I_{AR}, V_{DD} = 50V)	TBD	mJ
dv/dt (2)	Peak diode recovery voltage slope	TBD	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq$ 66 A, di/dt = 400 A/µs, peak $V_{DS} < V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.31	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	50	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	650			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0) V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C				1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 33 A		0.033	0.038	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	I_D = 33 A, V_{DS} = 15 V		TBD		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0		TBD TBD TBD		pF pF pF
$C_{o(tr)}$ (2)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 520 V		TBD		pF
$C_{o(er)}$ (3)	Equivalent capacitance energy related	V_{GS} = 0, V_{DS} = 0 to 520 V		TBD		pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain		TBD		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 520 V, I_D = 66 A, V_{GS} = 10 V (see *Figure 3*)		190 TBD TBD		nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
3. $C_{oss\ eq.}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 400 V, I_D = 40 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 4*)		TBD TBD TBD TBD		ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				66 264	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 33 A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 33 A, di/dt = 100 A/µs V_{DD} = 100 V (see *Figure 7*)		TBD TBD TBD		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 33 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C (see *Figure 7*)		TBD TBD TBD		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

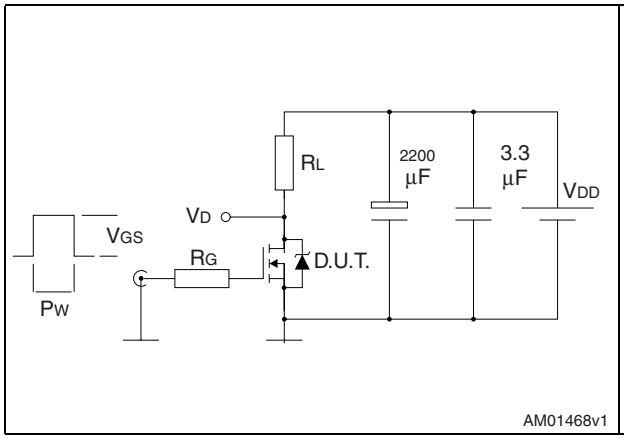


Figure 3. Gate charge test circuit

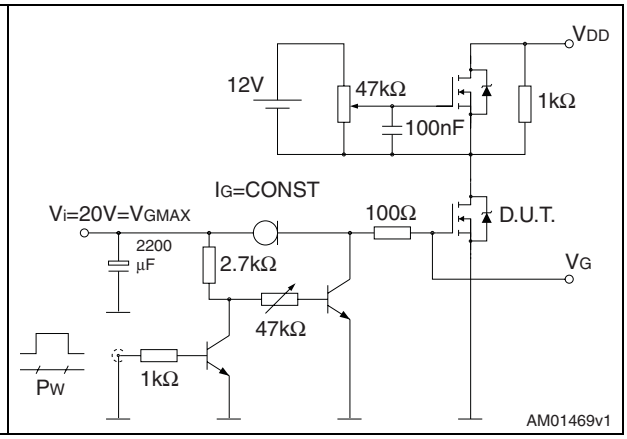


Figure 4. Test circuit for inductive load switching and diode recovery times

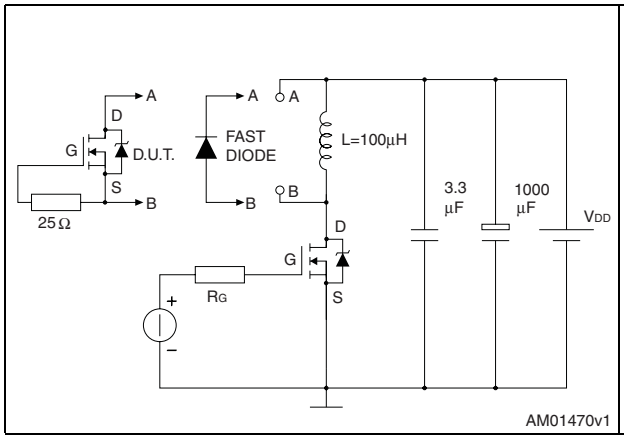


Figure 5. Unclamped inductive load test circuit

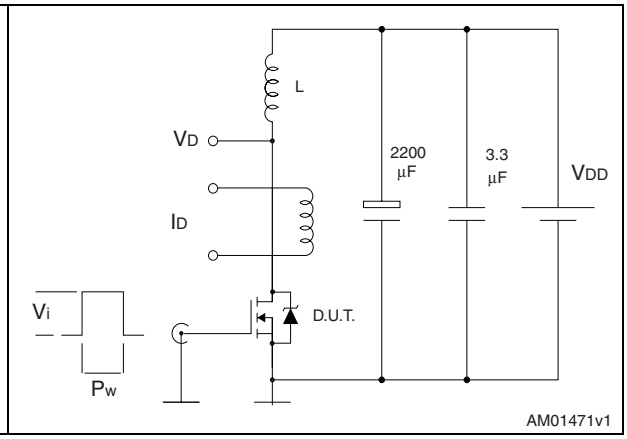


Figure 6. Unclamped inductive waveform

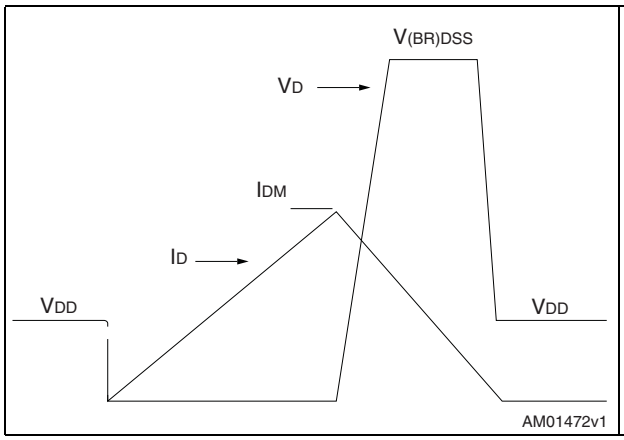
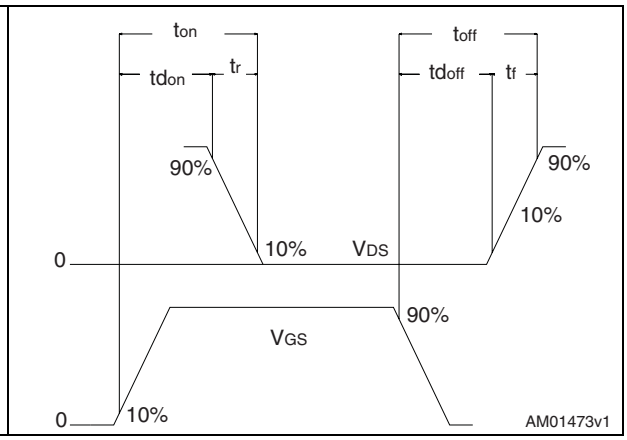


Figure 7. Switching time waveform

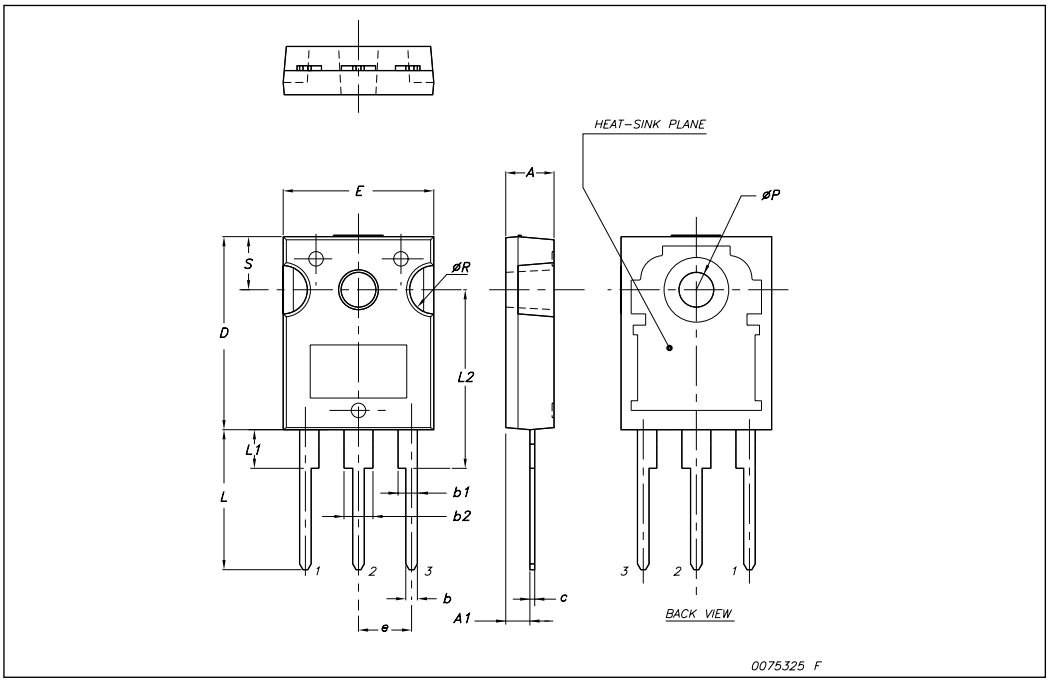


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

TO-247 Mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



5 Revision history

Table 8. Document revision history

Date	Revision	Changes
20-Jan-2009	1	First release

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