



# STD6N62K3 - STF6N62K3 STP6N62K3 - STU6N62K3

N-channel 620 V, 1.1  $\Omega$ , 5.5 A, IPAK, DPAK, TO-220, TO-220FP  
SuperMESH3™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>	P <sub>w</sub>
STD6N62K3	620 V	< 1.28 $\Omega$	5.5 A	90 W
STF6N62K3	620 V	< 1.28 $\Omega$	5.5 A <sup>(1)</sup>	25 W
STP6N62K3	620 V	< 1.28 $\Omega$	5.5 A	90 W
STU6N62K3	620 V	< 1.28 $\Omega$	5.5 A	90 W

1. Limited by package

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Improved diode reverse recovery characteristics
- Zener-protected

## Application

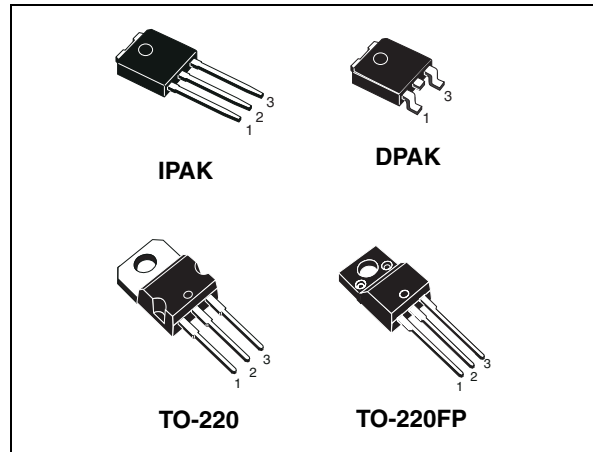
- Switching applications

## Description

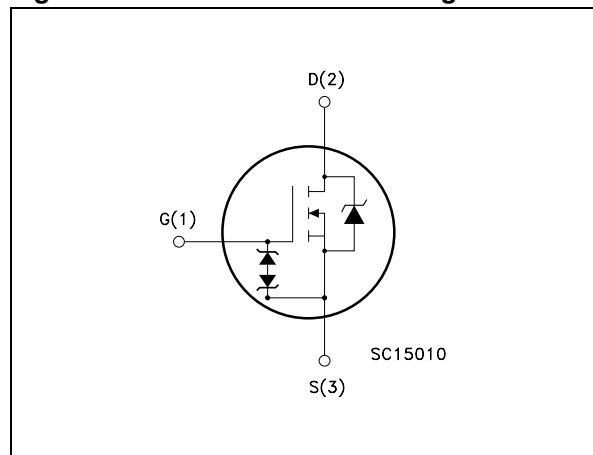
The new SuperMESH3™ series is obtained through the combination of a further fine tuning of ST's well established strip-based PowerMESH™ layout with a new optimization of the vertical structure. In addition to reducing on-resistance significantly versus previous generation, special attention has been taken to ensure a very good dv/dt capability and higher margin in breakdown voltage for the most demanding application.

**Table 1. Device summary**

Order codes	Marking	Package	Packaging
STD6N62K3	6N62K3	DPAK	Tape and reel
STF6N62K3	6N62K3	TO-220FP	Tube
STP6N62K3	6N62K3	TO-220	Tube
STU6N62K3	6N62K3	IPAK	Tube



**Figure 1. Internal schematic diagram**



# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value				Unit
		TO-220	DPAK	IPAK	TO-220FP	
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	620				V
$V_{GS}$	Gate- source voltage	$\pm 30$				V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	5.5		5.5 <sup>(1)</sup>		A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3.465		3.465 <sup>(1)</sup>		A
$I_{DM}$ <sup>(2)</sup>	Drain current (pulsed)	22		22 <sup>(1)</sup>		A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	90		25		W
	Derating factor	0.72		0.2		W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD(HBM-C = 100 pF, R = 1.5 k $\Omega$ )	2500				V
$dv/dt$ <sup>(3)</sup>	Peak diode recovery voltage slope	9				V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; $T_C = 25\text{ }^\circ\text{C}$ )	--		2500		V
$T_{stg}$	Storage temperature	-55 to 150				$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150				$^\circ\text{C}$

1. Limited by package
2. Pulse width limited by safe operating area
3.  $I_{SD} \leq 5.5\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	TO-220	DPAK	IPAK	TO-220FP	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.39			5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max	--	50	--	--	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	100		62.5	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	300				$^\circ\text{C}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Max value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	5.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{V}$ )	140	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	620			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$ , $T_C = 125\text{ °C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 2.8\text{ A}$		1.1	1.28	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}$ , $I_D = 2.8\text{ A}$		4.1		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$		706 66 8.4		pF pF pF
$C_{OSS\ eq(1)}$	Equivalent output capacitance	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }496\text{ V}$		60		pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain		7		$\Omega$
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 496\text{ V}$ , $I_D = 5.5\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 17</a> )		25.7 4.6 14.4		nC nC nC

1.  $C_{OSS\ eq}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on delay time Rise time Turn-off-delay time Fall time	$V_{DD} = 310\text{ V}$ , $I_D = 2.75\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16</a> )		13 12.5 27 19		ns ns ns ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				5.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				22	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5.5 \text{ A}, V_{GS} = 0$			1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 5.5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 30 \text{ V}$ (see <a href="#">Figure 21</a> )		190		ns
$Q_{rr}$	Reverse recovery charge			970		nC
$I_{RRM}$	Reverse recovery current			10.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 5.5 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 30 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 21</a> )		255		ns
$Q_{rr}$	Reverse recovery charge			1520		nC
$I_{RRM}$	Reverse recovery current			12		A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 9. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$ (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, IPAK, DPAK

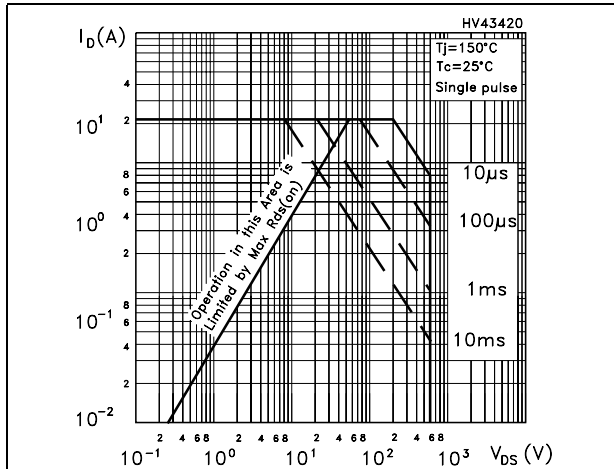


Figure 3. Thermal impedance for TO-220, IPAK, DPAK

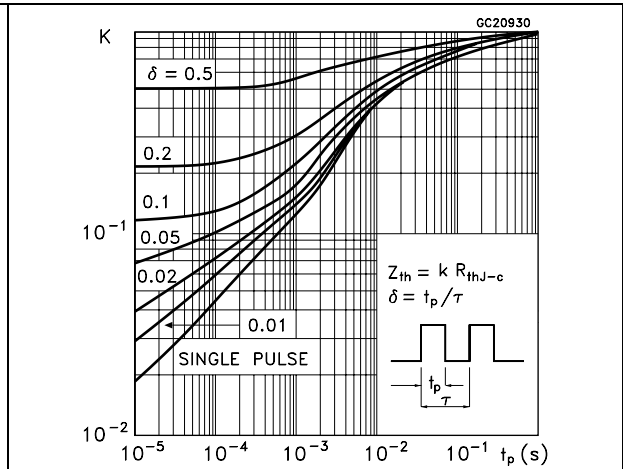


Figure 4. Safe operating area for TO-220FP

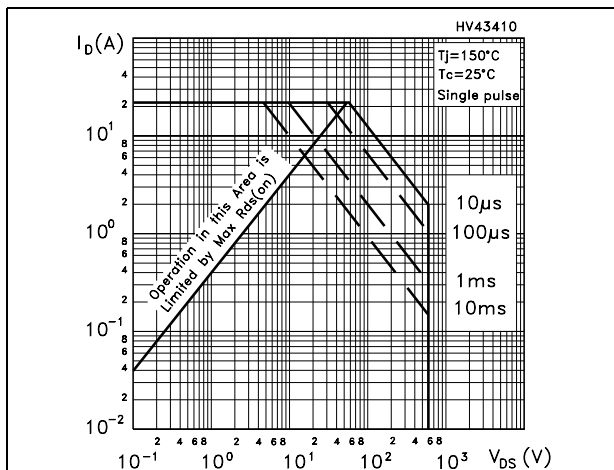


Figure 5. Thermal impedance for TO-220FP

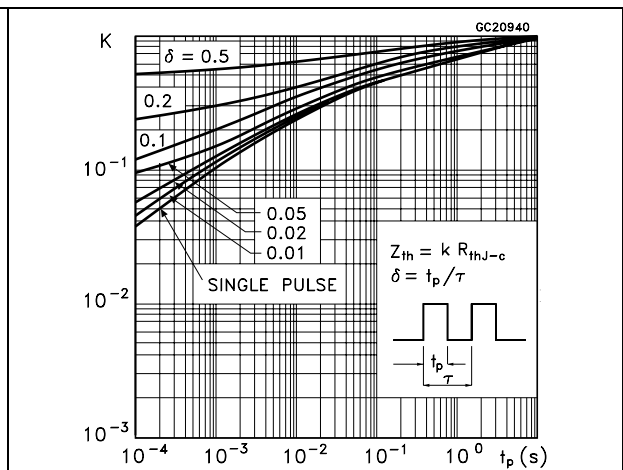


Figure 6. Output characteristics

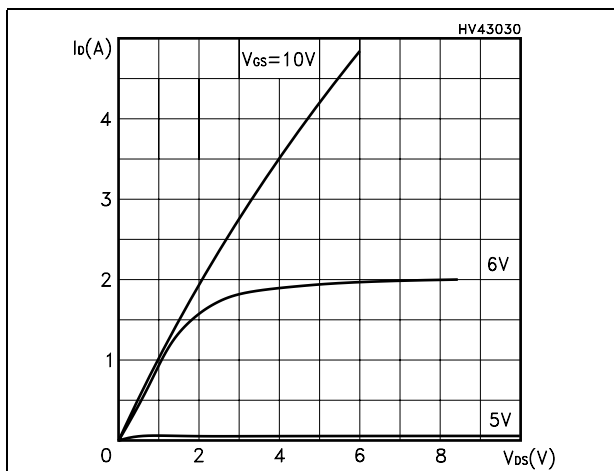


Figure 7. Transfer characteristics

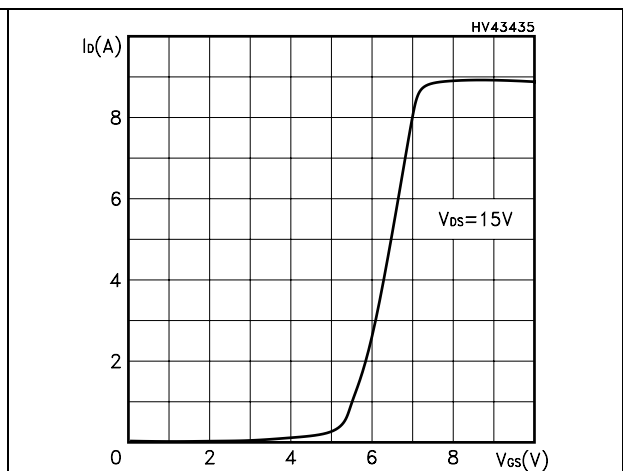


Figure 8. Normalized  $BV_{DSS}$  vs temperature      Figure 9. Static drain-source on resistance

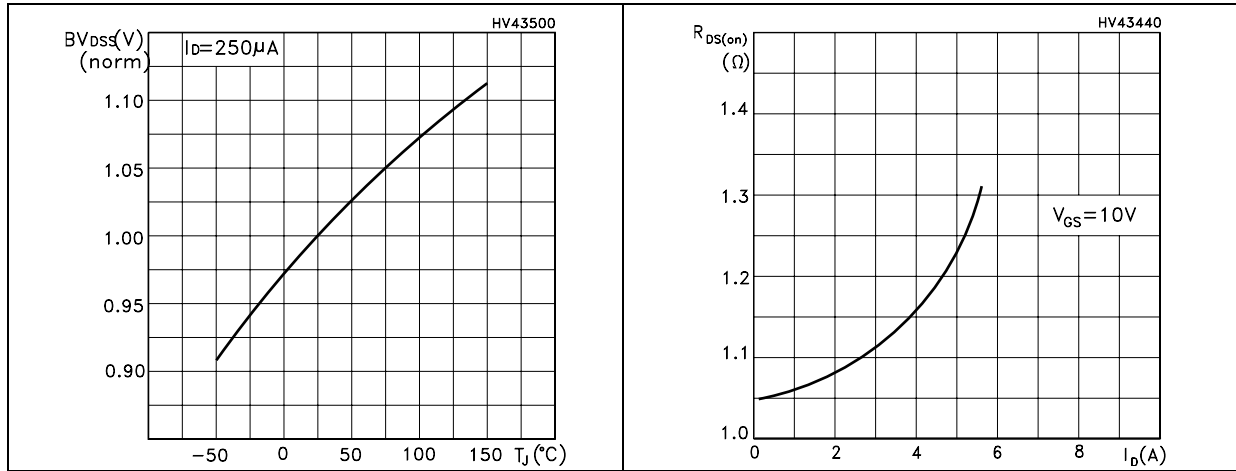


Figure 10. Gate charge vs gate-source voltage      Figure 11. Capacitance variations

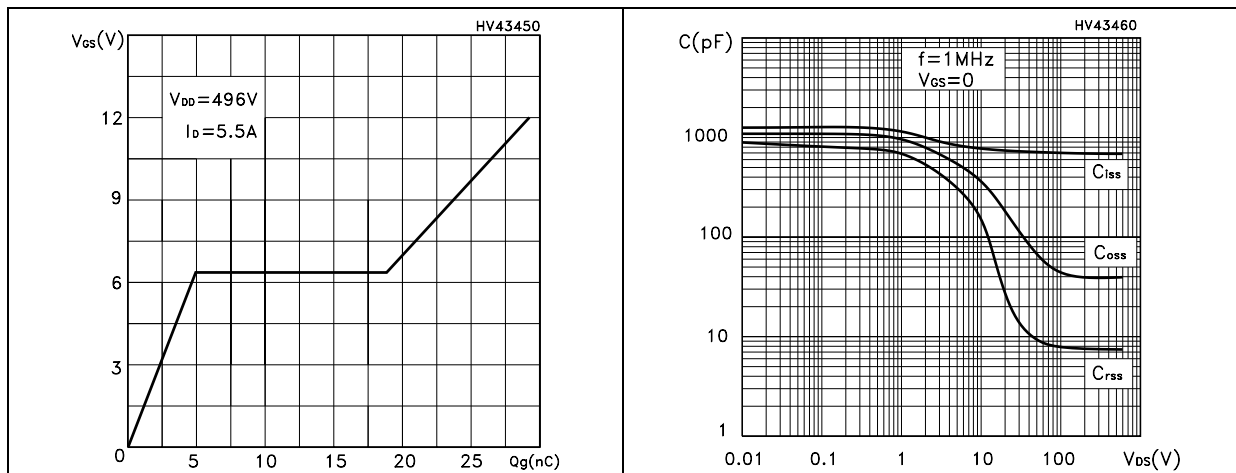


Figure 12. Normalized gate threshold voltage vs temperature      Figure 13. Normalized on resistance vs temperature

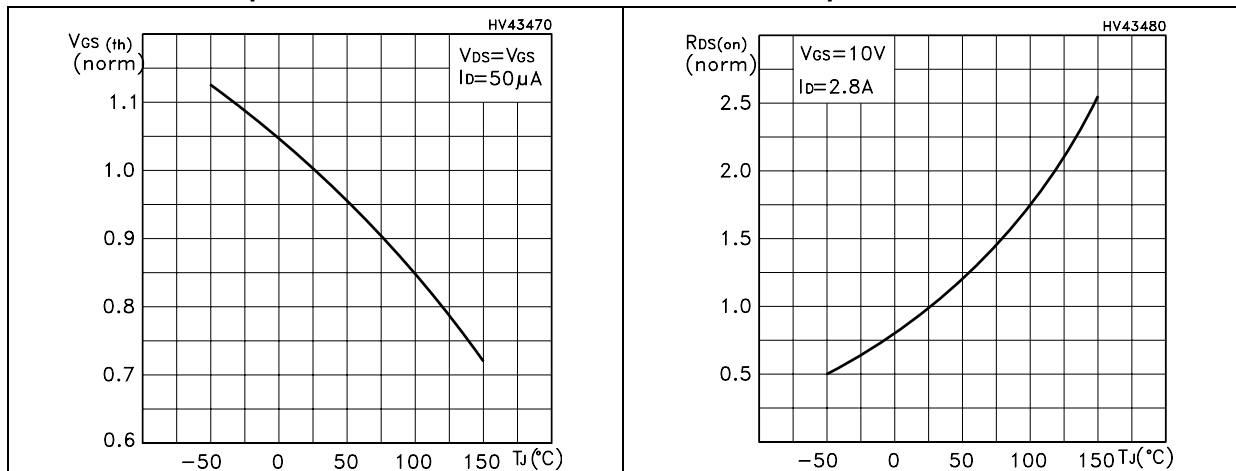


Figure 14. Source-drain diode forward characteristics

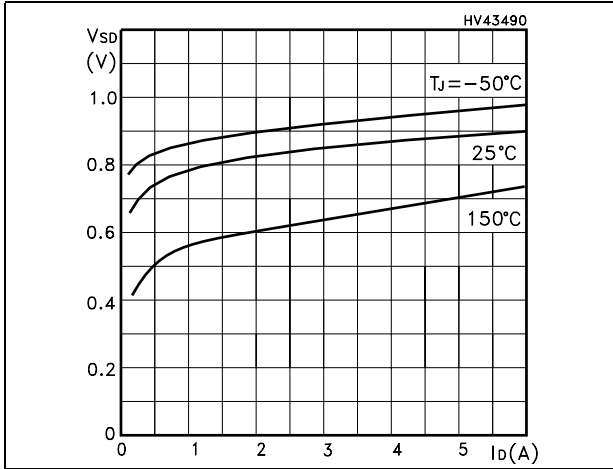
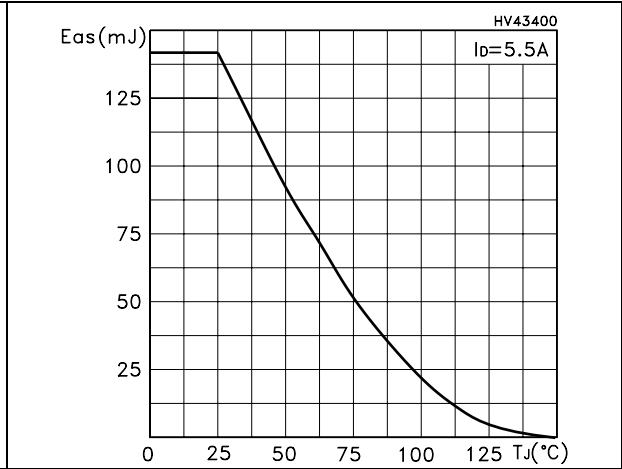


Figure 15. Maximum avalanche energy vs temperature





### 3 Test circuits

Figure 16. Switching times test circuit for resistive load

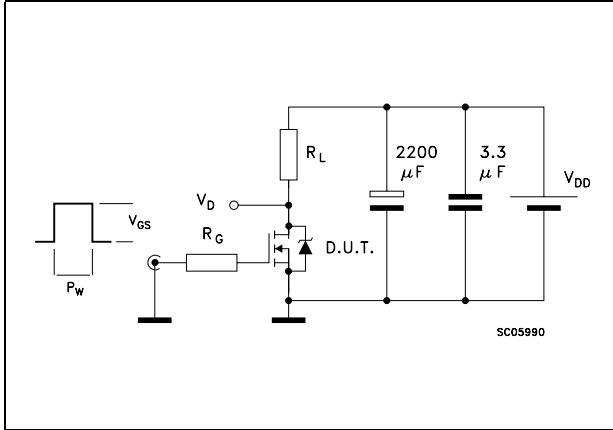


Figure 17. Gate charge test circuit

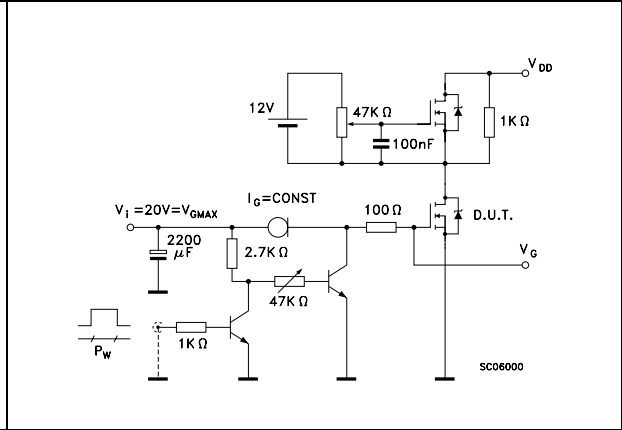


Figure 18. Test circuit for inductive load switching and diode recovery times

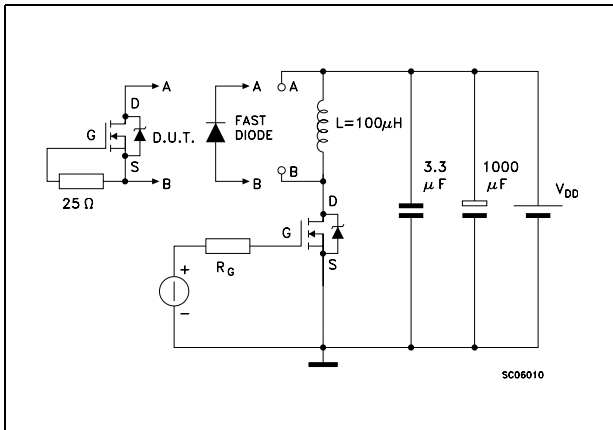


Figure 19. Unclamped Inductive load test circuit

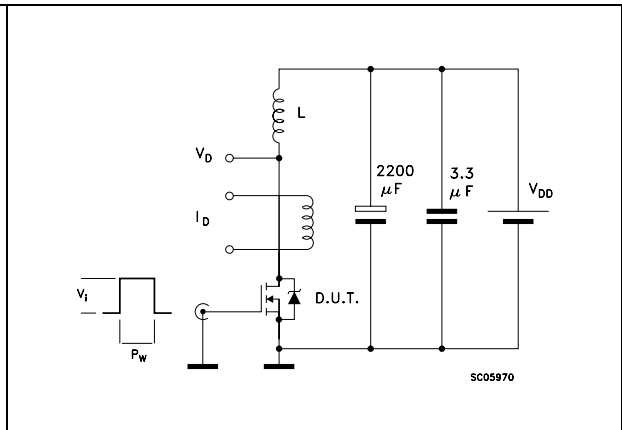


Figure 20. Unclamped inductive waveform

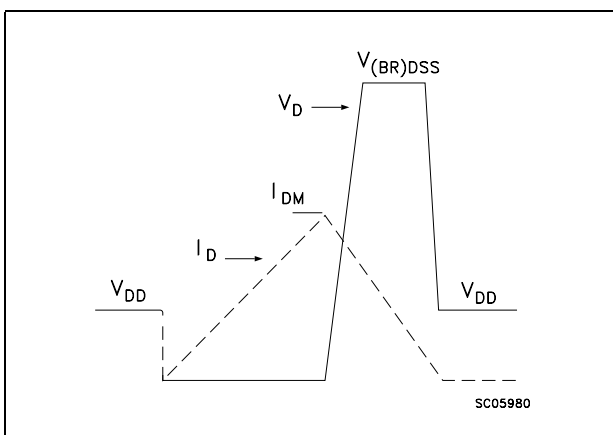
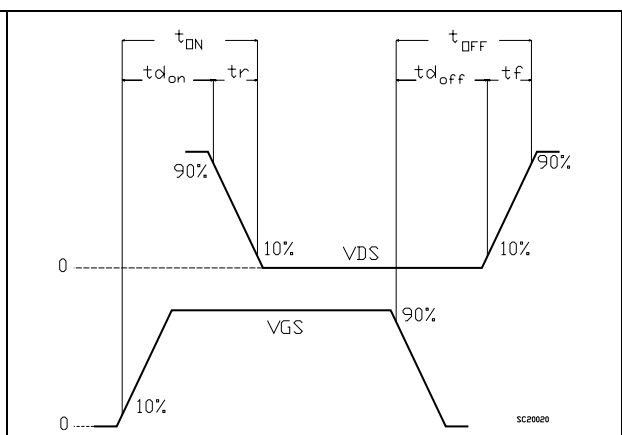


Figure 21. Switching time waveform

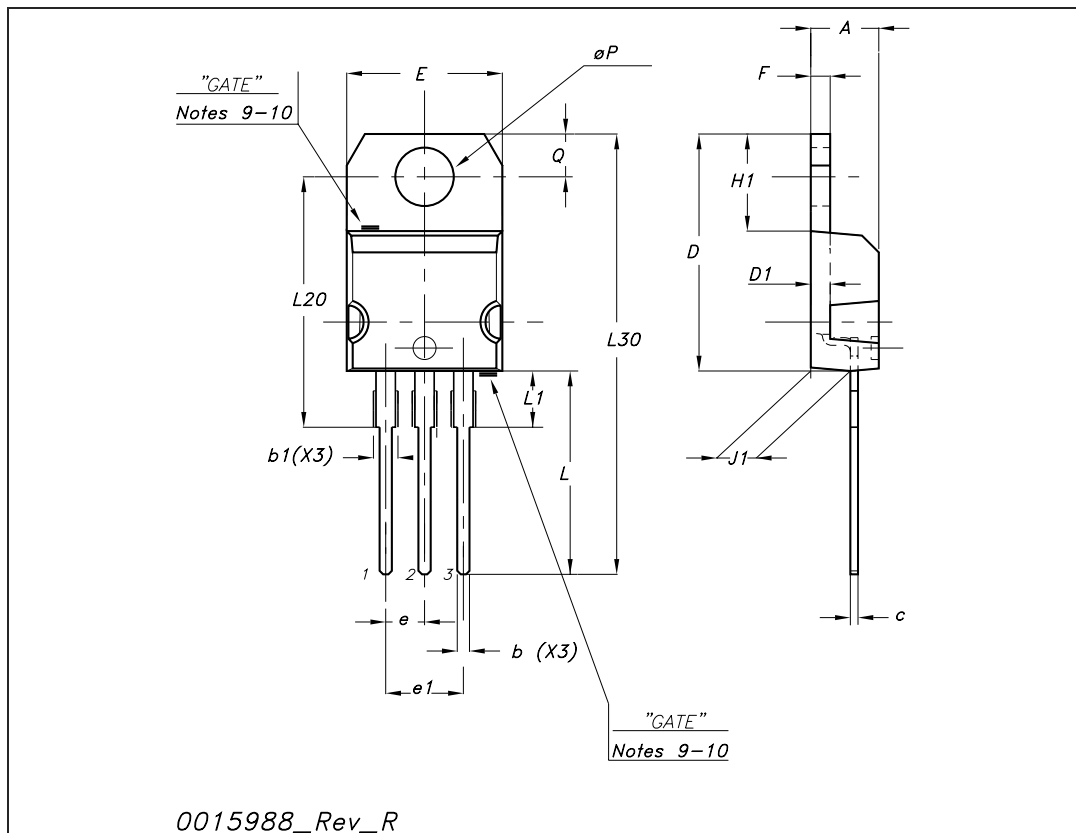


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

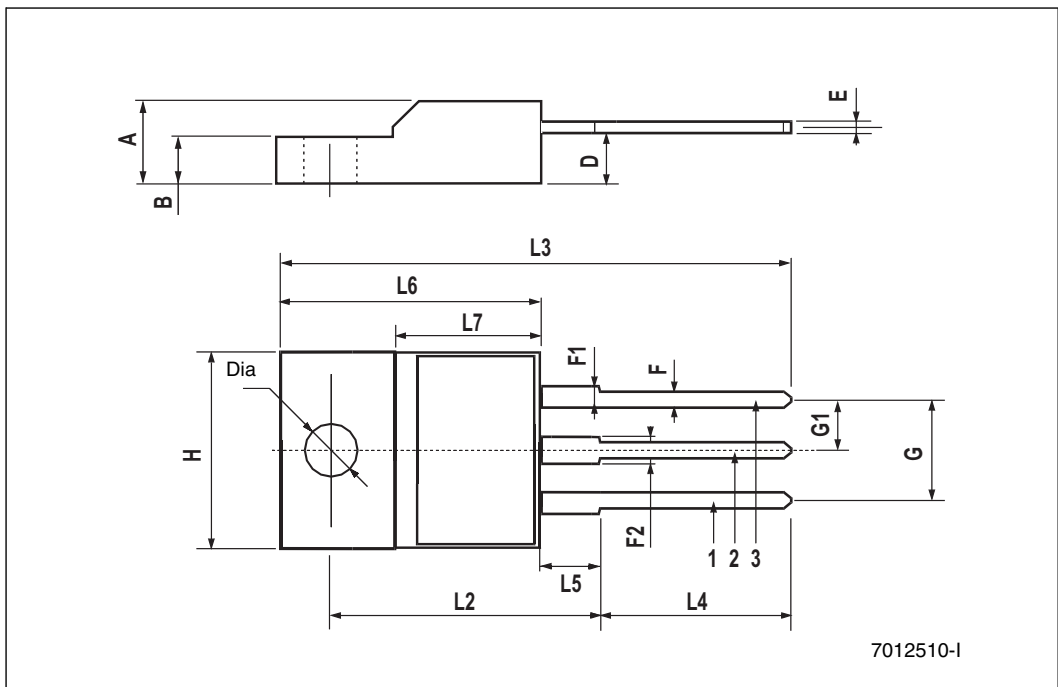
TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
∅P	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



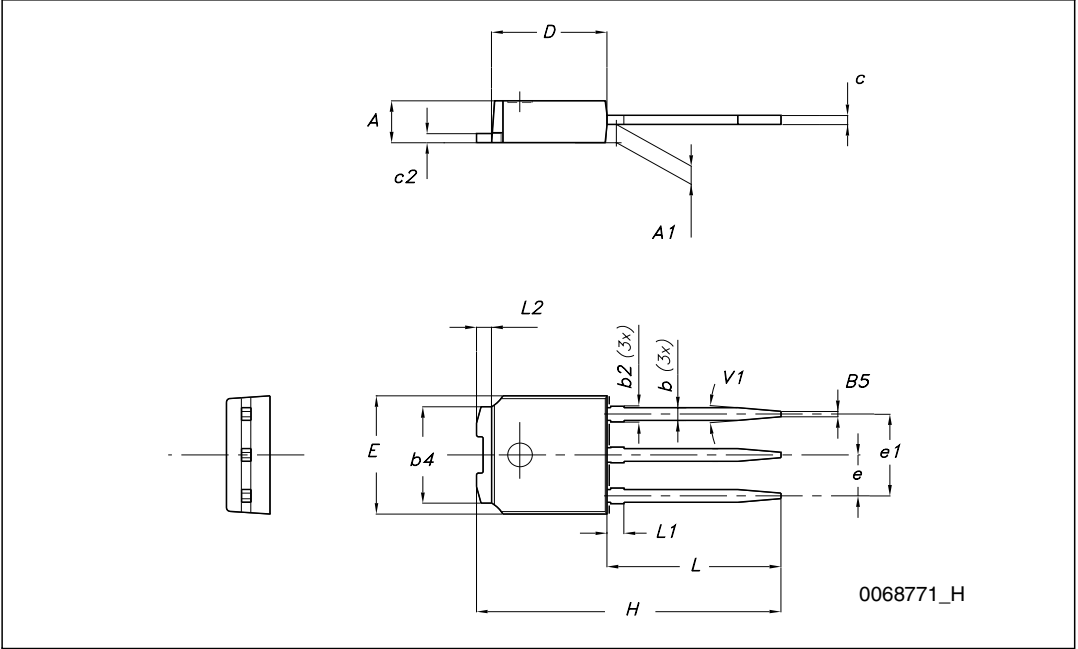
**TO-220FP mechanical data**

Dim.	mm.			inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.70	0.017		0.027
F	0.75		1.00	0.030		0.039
F1	1.15		1.50	0.045		0.067
F2	1.15		1.50	0.045		0.067
G	4.95		5.20	0.195		0.204
G1	2.40		2.70	0.094		0.106
H	10		10.40	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.80		10.60	0.385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.90		16.40	0.626		0.645
L7	9		9.30	0.354		0.366
Dia	3		3.2	0.118		0.126



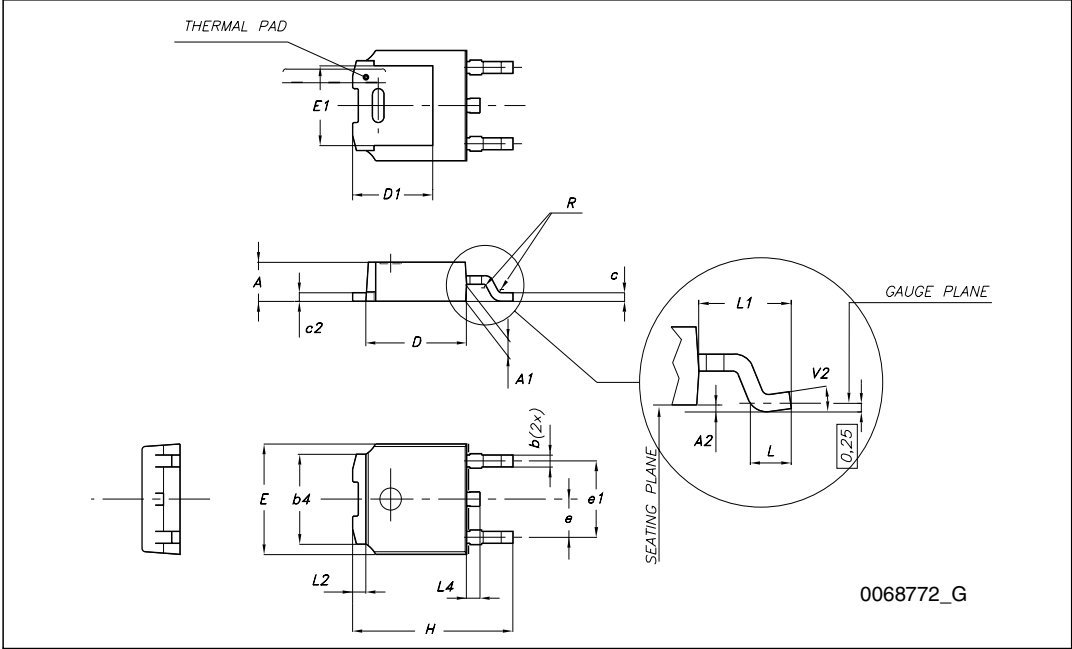
**TO-251 (IPAK) mechanical data**

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10°	



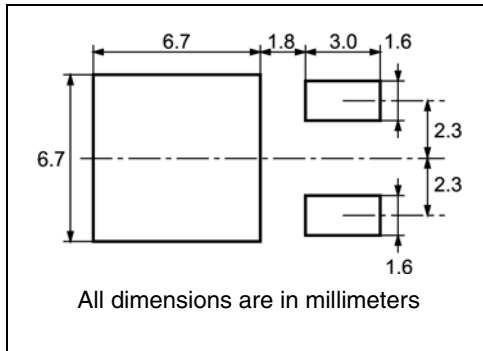
**TO-252 (DPAK) mechanical data**

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°



# 5 Package mechanical data

## DPAK FOOTPRINT



## TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

For machine ref. only including draft and radii concentric around B0

10 pitches cumulative tolerance on tape +/- 0.2 mm

Center line of cavity

User Direction of Feed

FEED DIRECTION

Bending radius R min.

## 6 Revision history

Table 10. Document revision history

Date	Revision	Changes
19-May-2006	1	First release



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