

# SN54LVC14A, SN74LVC14A HEX SCHMITT-TRIGGER INVERTERS

SCAS2850 – MARCH 1993 – REVISED MARCH 2002

- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Inputs Accept Voltages to 5.5 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

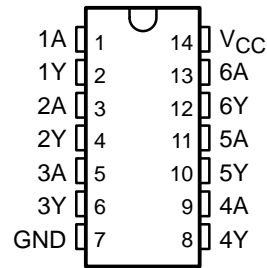
## description

The SN54LVC14A hex Schmitt-trigger inverter is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC14A hex Schmitt-trigger inverter is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

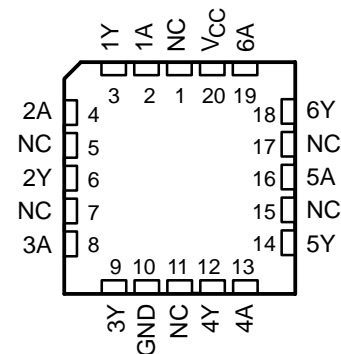
The devices contain six independent inverters, and perform the Boolean function  $Y = \bar{A}$ .

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

SN54LVC14A . . . J OR W PACKAGE  
SN74LVC14A . . . D, DB, DGV, NS, OR PW PACKAGE  
(TOP VIEW)



SN54LVC14 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tube	SN74LVC14AD	LVC14A
		Tape and reel	SN74LVC14ADR	
	SOP – NS	Tape and reel	SN74LVC14ANSR	LVC14A
	SSOP – DB	Tape and reel	SN74LVC14ADBR	LC14A
	TSSOP – PW	Tape and reel	SN74LVC14APWR	LC14A
–55°C to 125°C	TVSOP – DGV	Tape and reel	SN74LVC14ADGVR	LC14A
	CDIP – J	Tube	SNJ54LVC14AJ	SNJ54LVC14AJ
	CFP – W	Tube	SNJ54LVC14AW	SNJ54LVC14AW
	LCCC – FK	Tube	SNJ54LVC14AFK	SNJ54LVC14AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

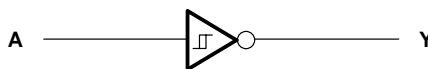
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**FUNCTION TABLE**  
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram, each inverter (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 6.5 V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3):	
D package .....	86°C/W
DB package .....	96°C/W
DGV package .....	127°C/W
NS package .....	76°C/W
PW package .....	113°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.
  3. The package thermal impedance is calculated in accordance with JESD 51-7.

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## recommended operating conditions (see Note 4)

		SN54LVC14A		SN74LVC14A		UNIT		
		MIN	MAX	MIN	MAX			
V <sub>CC</sub>	Supply voltage	Operating		2	3.6	1.65	3.6	V
		Data retention only		1.5		1.5		
V <sub>I</sub>	Input voltage	0	5.5	0	5.5		V	
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>		V	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V					-4	mA
		V <sub>CC</sub> = 2.3 V					-8	
		V <sub>CC</sub> = 2.7 V			-12		-12	
		V <sub>CC</sub> = 3 V			-24		-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V					4	mA
		V <sub>CC</sub> = 2.3 V					8	
		V <sub>CC</sub> = 2.7 V			12		12	
		V <sub>CC</sub> = 3 V			24		24	
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85		°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54LVC14A, SN74LVC14A HEX SCHMITT-TRIGGER INVERTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC14A			SN74LVC14A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>T+</sub> Positive-going threshold		2.7 V	0.8		2	0.8		2	V
		3 V	0.8		2	0.8		2	
		3.6 V	0.8		2	0.8		2	
V <sub>T-</sub> Negative-going threshold		2.7 V	0.4		1.4	0.4		1.4	V
		3 V	0.6		1.5	0.6		1.5	
		3.6 V	0.8		1.8	0.8		1.8	
ΔV <sub>T</sub> Hysteresis (V <sub>T+</sub> – V <sub>T-</sub> )		2.7 V	0.3		1.1	0.3		1.1	V
		3 V	0.3		1.2	0.3		1.2	
		3.6 V	0.3		1.2	0.3		1.2	
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA	1.65 V to 3.6 V				V <sub>CC</sub> –0.2			V
		2.7 V to 3.6 V	V <sub>CC</sub> –0.2						
	I <sub>OH</sub> = –4 mA	1.65 V			1.2				
	I <sub>OH</sub> = –8 mA	2.3 V			1.7				
	I <sub>OH</sub> = –12 mA	2.7 V	2.2			2.2			
		3 V	2.4			2.4			
I <sub>OH</sub> = –24 mA	3 V	2.2			2.2				
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V				0.2			V
		2.7 V to 3.6 V	0.2						
	I <sub>OL</sub> = 4 mA	1.65 V			0.45				
	I <sub>OL</sub> = 8 mA	2.3 V			0.7				
	I <sub>OL</sub> = 12 mA	2.7 V			0.4	0.4			
		3 V			0.55	0.55			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V			±5	±5			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			10	10			μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500	500			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			5	5			pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC14A				UNIT
			V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y		7.5	1	6.4	ns



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC14A						UNIT		
			V <sub>CC</sub> = 1.8 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V			V <sub>CC</sub> = 3.3 V ± 0.3 V	
			TYP		MIN	MAX	MIN	MAX		MIN	MAX
t <sub>pd</sub>	A	Y	13.7		7.8		7.5		1	6.4	ns
t <sub>sk(o)</sub>									1		ns

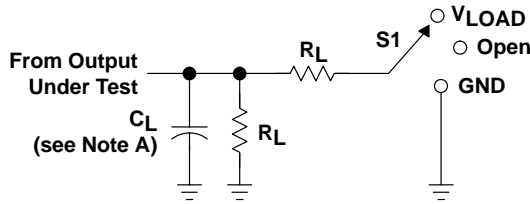
operating characteristics, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
		TYP	TYP	TYP	
C <sub>pd</sub> Power dissipation capacitance per inverter	f = 10 MHz	11	12	15	pF

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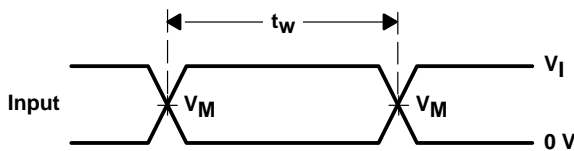
## PARAMETER MEASUREMENT INFORMATION



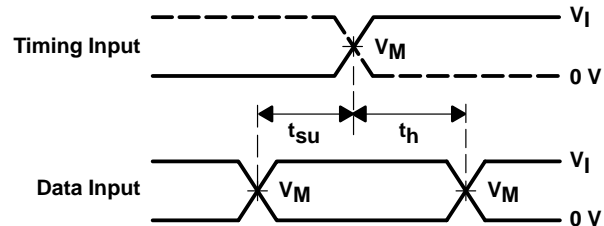
LOAD CIRCUIT

TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

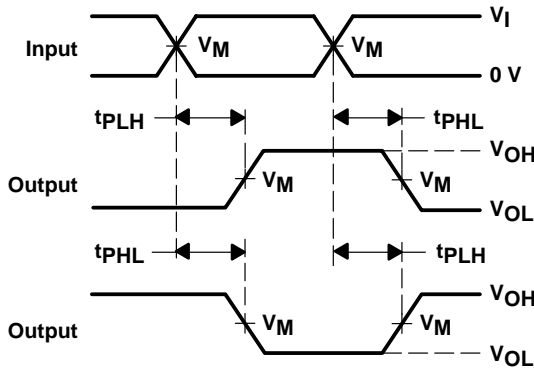
V <sub>CC</sub>	INPUTS		V <sub>M</sub>	V <sub>LOAD</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>Δ</sub>
	V <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>					
1.8 V ± 0.15 V	V <sub>CC</sub>	≤ 2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V <sub>CC</sub>	≤ 2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



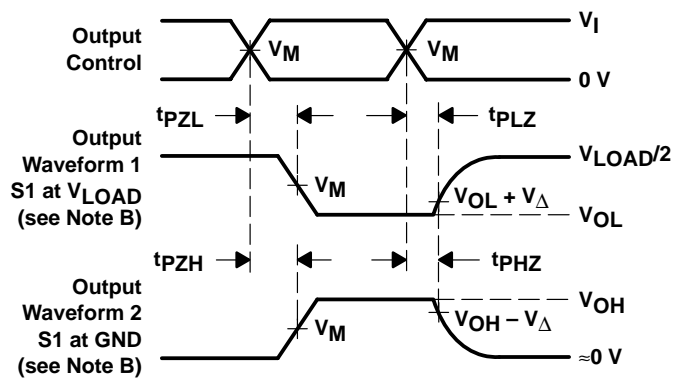
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C<sub>L</sub> includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω.
  - The outputs are measured one at a time with one transition per measurement.
  - t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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