N-Channel 60-V (D-S) Rated MOSFET

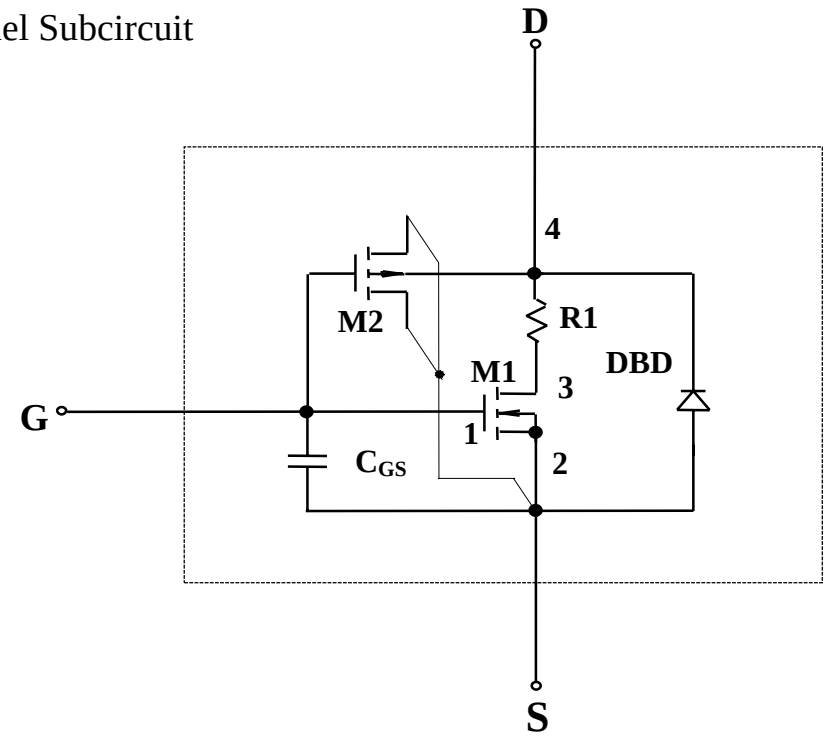
Characteristics

- N-channel Vertical DMOS
- Macro-Model (Subcircuit)
- Level 3 MOS
- Applicable for Both Linear and Switch Mode
- Applicable Over a -55 to 125°C Temperature Range
- Models Gate Charge, Transient, and Diode Reverse Recovery Characteristics

Description

The attached SPICE Model describes typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model was extracted and optimized over a 25°C to 125°C temperature range under pulse conditions for 0 to 10 volt gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold. A novel gate-to-drain feedback capacitance network is used to model gate charge characteristics while avoiding convergence problems of switched C_{gd} model. Model parameter values are optimized to provide a best fit to measured electrical data and are not intended as an exact physical description of a device.

Model Subcircuit



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

Model Evaluation
N-Channel Device (T_J=25°C Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Typ	Unit
Static				
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D= 250µA	**1.82**	V
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ **4.5V**, V_{GS} = **10**V	**30**	A
		V_{DS} ≥ **4.5**V, V_{GS} = **4.5**V	**11**	A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = **10**V, I_D = **2**A V_{GS} = **4.5**V, I_D = **1.7**A	**0.14** **0.17**	Ω
Forward Transconductance[a]	g_{fs}	V_{DS} = **4.5**V, I_D = **2**A	**4.2**	S
Diode Forward Voltage[a]	V_{SD}	I_S = **1**A, V_{GS} = 0V	**0.77**	V
Dynamic				
Total Gate Charge	Q_g	V_{DS} = **30**V, V_{GS} = **10**V, I_D = **2**A	**4.7**	nC
Gate-Source Charge	Q_{gs}		**0.8**	
Gate-Drain Charge	Q_{gd}		**1**	
Input Capacitance	C_{iss}	V_{DS} = **25**V, V_{GS} = **0**V, f = 1MHz	**229**	pF
Output Capacitance	C_{oss}		**48**	
Reverse Transfer Capacitance	C_{rss}		**13**	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = **30**V, R_L = **30**Ω I_D ≅ **1**A, V_{GEN} = **4.5**V, R_G = 6Ω	**8**	ns
Rise Time	t_r		**6**	
Turn-Off Delay Time	$t_{d(off)}$		**16**	
Fall Time	t_f		**6**	

Notes:
a) Pulse Test: pulse width ≤ 300 µs, duty cycle ≤ 2%

SPICE Device Model Si2308DS

Comparison of Model with Measured Data
(T_J=25°C Unless Otherwise Noted)