

## IRS20957S Protected Digital Audio Driver

### Features

- Floating PWM input enables easy half bridge implementation
- Programmable bidirectional over-current protection with self-reset function
- Programmable preset dead-time for improved THD performances
- High noise immunity
- $\pm 100V$  ratings deliver up to 500W in output power
- 3.3 V/ 5 V logic compatible input
- Operates up to 800kHz

### Typical Applications

- Home theatre systems
- Mini component stereo systems
- Powered speaker systems
- General purpose audio power amplifiers

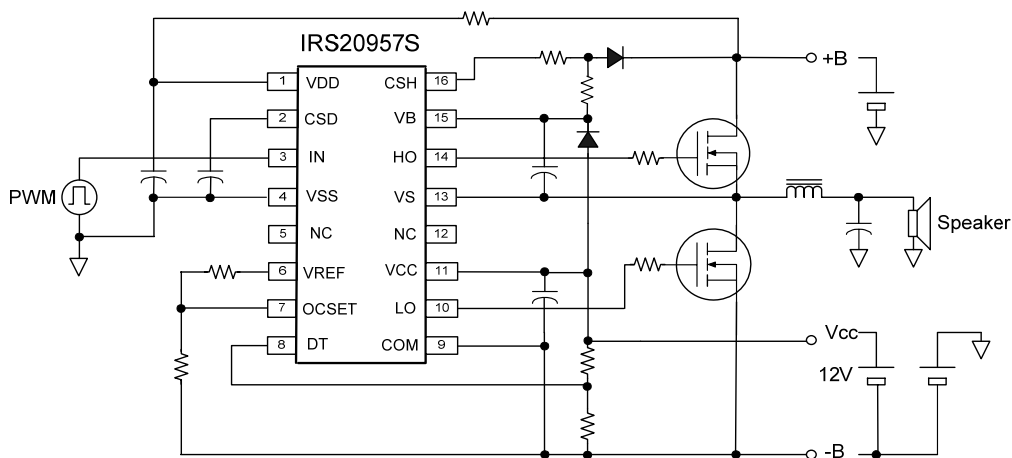
### Product Summary

Topology	Half-Bridge
$V_{\text{OFFSET (max)}}$	+/- 100 V
$I_{O+}$ & $I_{O-}$ (typical)	1.0 A & 1.2 A
Selectable deadtime	15/25/35/80ns
Ton & toff (typical)	95ns & 80ns
OC protection delay	500ns (max)
Shutdown propagation delay	250ns (max)

### Package



### Typical Connection Diagram



Note: Please refer to Lead Assignments for correct pin configuration. This diagram shows electrical connections only.

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**Description**

The IRS20957S is a high voltage, high speed MOSFET driver with a floating PWM input designed for Class D audio amplifier applications.

Bi-directional current sensing detects over current conditions during positive and negative load currents without any external shunt resistors. A built-in protection control block provides a secure protection sequence against over-current conditions and a programmable reset timer.

The internal dead-time generation block enables accurate gate switching and optimum dead-time setting for better audio performance, such as lower THD and lower audio noise floor.

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>		Industrial <sup>††</sup>	
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
<b>Moisture Sensitivity Level</b>		SOIC16N	MSL2 <sup>†††</sup> 260°C (per IPC/JEDEC J-STD-020)
<b>ESD</b>	<b>Machine Model</b>	Class B (per JEDEC standard EIA/JESD22-A115)	
	<b>Human Body Model</b>	Class 2 (per EIA/JEDEC standard JESD22-A114)	
<b>IC Latch-Up Test</b>		Class I , Level A (per JESD78)	
<b>RoHS Compliant</b>		Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

**Absolute Maximum Ratings**

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to  $V_{SS}$ ; all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
$V_B$	High side floating supply voltage	-0.3	215	V
$V_S$	High side floating supply voltage <sup>†</sup>	$V_B-15$	$V_B+0.3$	
$V_{HO}$	High side floating output voltage	$V_S-0.3$	$V_B+0.3$	
$V_{CSH}$	CSH pin input voltage	$V_S-0.3$	$V_B+0.3$	
$V_{CC}$	Low side fixed supply voltage <sup>†</sup>	-0.3	20	
$V_{LO}$	Low side output voltage	-0.3	$V_{CC} +0.3$	
$V_{DD}$	Floating input supply voltage	-0.3	210	
$V_{SS}$	Floating input supply voltage <sup>†</sup>	(See $I_{DDZ}$ )	$V_{DD}+0.3$	
$V_{IN}$	PWM input voltage	$V_{SS} -0.3$	$V_{DD}+0.3$	
$V_{CSD}$	CSD pin input voltage	$V_{SS} -0.3$	$V_{DD}+0.3$	
$V_{DT}$	DT pin input voltage	-0.3	$V_{CC} +0.3$	
$V_{OCSET}$	OCSET pin input voltage	-0.3	$V_{CC} +0.3$	
$V_{REF}$	VREF pin voltage	-0.3	$V_{CC} +0.3$	
$I_{DDZ}$	Floating input supply zener clamp current <sup>†</sup>	-	10	
$I_{CCZ}$	Low side supply zener clamp current <sup>†</sup>	-	10	
$I_{BSZ}$	Floating supply zener clamp current <sup>†</sup>	-	10	
$I_{OREF}$	Reference output current	-	5	
$d V_S /dt$	Allowable $V_S$ voltage slew rate	-	50	V/ns
$d V_{SS} /dt$	Allowable $V_{SS}$ voltage slew rate <sup>††</sup>	-	50	
$d V_{SS} /dt$	Allowable $V_{SS}$ voltage slew rate upon power-up <sup>†††</sup>	-	50	V/ms
$P_d$	Maximum power dissipation	-	1.0	W
$R_{thJA}$	Thermal resistance, Junction to ambient	-	115	°C/W
$T_J$	Junction Temperature	-	150	°C
$T_S$	Storage Temperature	-55	150	
$T_L$	Lead temperature (Soldering, 10 seconds)	-	300	

†  $V_{DD} - V_{SS}$ ,  $V_{CC} -COM$  and  $V_B - V_S$  contain internal shunt zener diodes. Please note that the voltage ratings of these can be limited by the clamping current.

†† For the rising and falling edges of step signal of 10V.  $V_{SS}=15V$  to 200V.

†††  $V_{SS}$  ramps up from 0V to 200V.

**Recommended Operating Conditions**

For proper operation, the device should be used within the recommended conditions below. The Vs and COM offset ratings are tested with supplies biased at  $I_{DD}=5\text{mA}$ ,  $V_{CC}=12\text{V}$  and  $V_B-V_S=12\text{V}$ .

Symbol	Definition	Min.	Max.	Units
$V_B$	High side floating supply absolute voltage	$V_S+10$	$V_S+14$	V
$V_S$	High side floating supply offset voltage	†	200	
$I_{DDZ}$	Floating input supply zener clamp current	1	5	mA
$V_{SS}$	Floating input supply absolute voltage	0	100	V
$V_{HO}$	High side floating output voltage	$V_S$	$V_B$	
$V_{CC}$	Low side fixed supply voltage	10	15	
$V_{LO}$	Low side output voltage	0	$V_{CC}$	
$V_{IN}$	PWM input voltage	$V_{SS}$	$V_{DD}$	
$V_{CSD}$	CSD pin input voltage	$V_{SS}$	$V_{DD}$	
$V_{DT}$	DT pin input voltage	0	$V_{CC}$	
$I_{OREF}$	Reference output current to COM <sup>†</sup>	0.3	0.8	mA
$V_{OCSET}$	OCSET pin input voltage	0.5	5	V
$T_A$	Ambient Temperature	-40	125	°C

† Logic operational for Vs equal to -5V to +200V. Logic state held for Vs equal to -5V to -V<sub>BS</sub>.

†† Nominal voltage for V<sub>REF</sub> is 5V. I<sub>OREF</sub> of 0.3 – 0.8mA dictates total external resistor value on VREF to be 6.3k to 16.7k Ω.

**Electrical Characteristics**

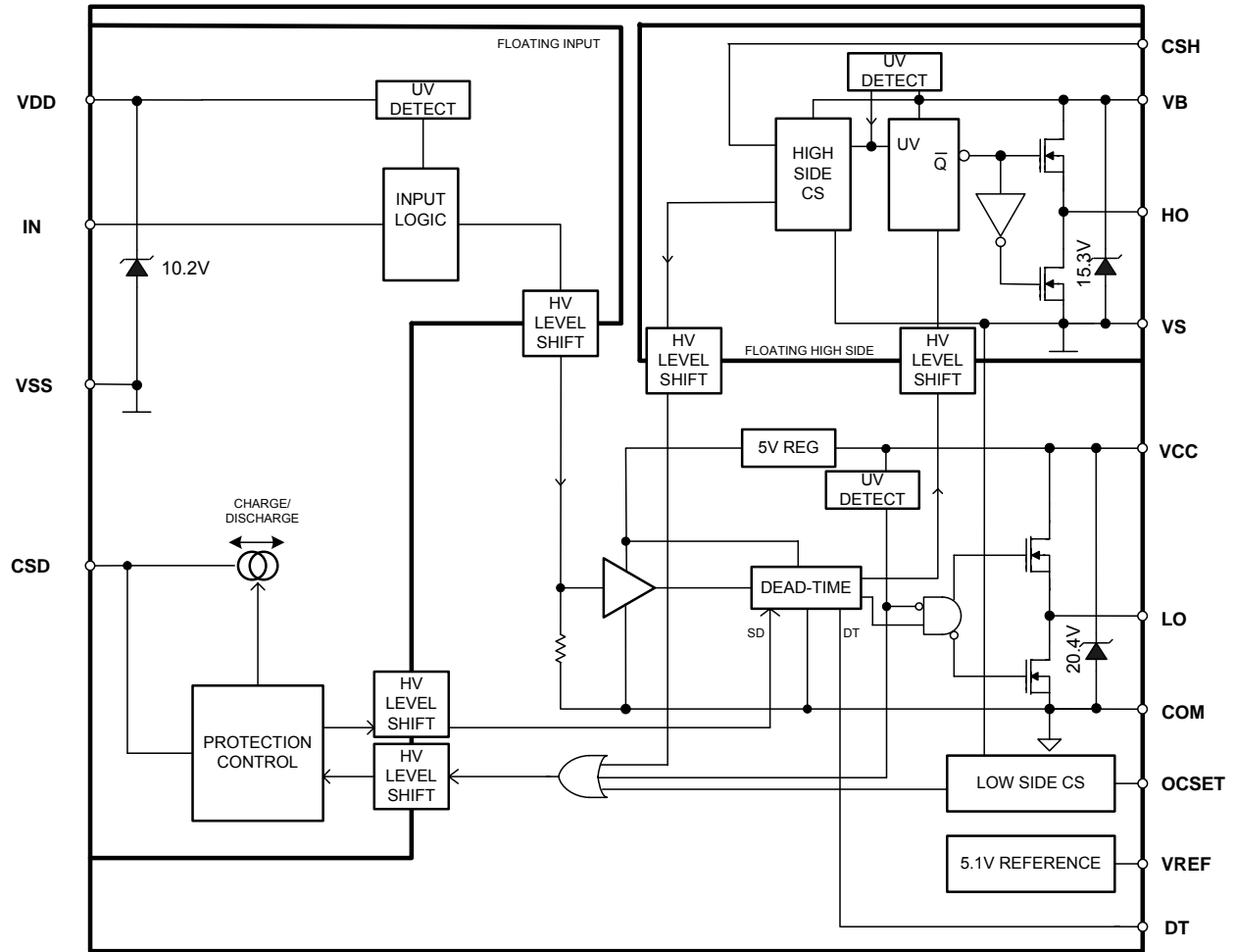
$V_{CC}, V_{BS} = 12\text{ V}$ ,  $I_{DD} = 5\text{ mA}$ ,  $V_{SS} = 20\text{ V}$ ,  $V_S = 0\text{ V}$ ,  $C_L = 1\text{ nF}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Description	Min	Typ	Max	Units	Test Conditions
<b>Low Side Supply</b>						
$UV_{CC+}$	$V_{CC}$ supply UVLO positive threshold	8.4	8.9	9.4	V	
$UV_{CC-}$	$V_{CC}$ supply UVLO negative threshold	8.2	8.7	9.2		
$I_{QCC}$	Low side quiescent current	-	-	3	mA	$V_{DT} = V_{CC}$
$V_{CLAMPL}$	Low side zener diode clamp voltage	19.6	20.4	21.6	V	$I_{CC} = 5\text{ mA}$
<b>High Side Floating Supply</b>						
$UV_{BS+}$	High side well UVLO positive threshold	8.0	8.5	9.0	V	
$UV_{BS-}$	High side well UVLO negative threshold	7.8	8.3	8.8		
$I_{QBS}$	High side quiescent current	-	-	1	mA	
$I_{LKH}$	High to Low side leakage current	-	-	50	$\mu\text{A}$	$V_B = V_S = 200\text{ V}$
$V_{CLAMPH}$	High side zener diode clamp voltage	14.7	15.3	16.2	V	$I_{BS} = 5\text{ mA}$
<b>Floating Input Supply</b>						
$UV_{DD+}$	$V_{DD}, V_{SS}$ floating supply UVLO positive threshold	8.2	8.7	9.2	V	$V_{SS} = 0\text{ V}$
$UV_{DD-}$	$V_{DD}, V_{SS}$ floating supply UVLO negative threshold	7.7	8.2	8.7		$V_{SS} = 0\text{ V}$
$I_{QDD}$	Floating Input quiescent current	-	-	1	mA	$V_{DD} = 9.5\text{ V} + V_{SS}$
$V_{CLAMPM}$	Floating Input zener diode clamp voltage	9.8	10.2	10.8	V	$I_{DD} = 5\text{ mA}$
$I_{LKM}$	Floating input side to Low side leakage current	-	-	50	$\mu\text{A}$	$V_{DD} = V_{SS} = 200\text{ V}$
<b>Floating PWM Input</b>						
$V_{IH}$	Logic high input threshold voltage	2.3	1.9	-	V	
$V_{IL}$	Logic low input threshold voltage	-	1.9	1.5		
$I_{IN+}$	Logic "1" input bias current	-	-	40	$\mu\text{A}$	$V_{IN} = 3.3\text{ V}$
$I_{IN-}$	Logic "0" input bias current	-	-	1		$V_{IN} = V_{SS}$
<b>Protection</b>						
$V_{REF}$	Reference output voltage	4.8	5.1	5.4	V	$I_{OREF} = 0.5\text{ mA}$
$V_{thOCL}$	Low side OC threshold in $V_S$	1.1	1.2	1.3		OCSET=1.2V, Figure 3
$V_{thOCH}$	High side OC threshold in $V_{CSH}$	$1.1 + V_S$	$1.2 + V_S$	$1.3 + V_S$		$V_S = 200\text{ V}$ , Figure 4
$V_{th1}$	CSD pin shutdown release threshold	$0.62 \times V_{DD}$	$0.70 \times V_{DD}$	$0.78 \times V_{DD}$		$V_{SS} = 0\text{ V}$
$V_{th2}$	CSD pin self reset threshold	$0.26 \times V_{DD}$	$0.30 \times V_{DD}$	$0.34 \times V_{DD}$		$V_{SS} = 0\text{ V}$
$I_{CSD+}$	CSD pin discharge current	70	100	130	$\mu\text{A}$	$V_{SD} = V_{SS} + 5\text{ V}$
$I_{CSD-}$	CSD pin charge current	70	100	130		$V_{SD} = V_{SS} + 5\text{ V}$

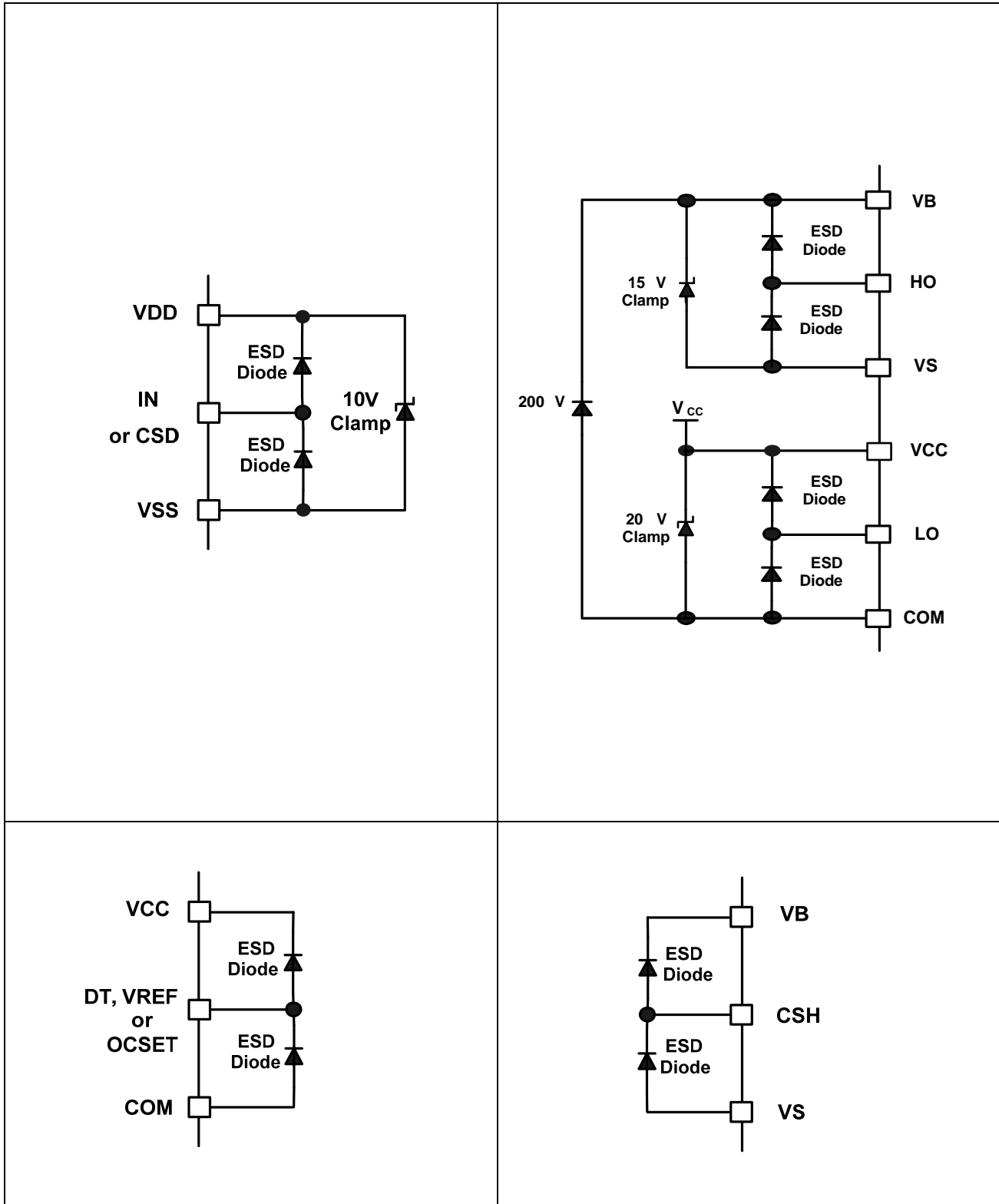
Protection (continued)						
Symbol	Description	Min	Typ	Max	Units	Test Conditions
$t_{SD}$	Shutdown propagation delay from $V_{CSD} > V_{SS} + V_{th_{OCH}}$ to Shutdown	-	-	250	ns	Figure 2
$t_{OCH}$	Propagation delay time from $V_{CSH} > V_{th_{OCH}}$ to Shutdown	-	-	500		Figure 4
$t_{OCL}$	Propagation delay time from $V_S > V_{th_{OCL}}$ to Shutdown	-	-	500		Figure 3
Gate Driver						
$I_{o+}$	Output high short circuit current (Source)	-	1.0	-	A	$V_o=0V$ , $PW \leq 10\mu S$
$I_{o-}$	Output low short circuit current (Sink)	-	1.2	-		$V_o=12V$ , $PW \leq 10\mu S$
$V_{OL}$	Low level out put voltage LO – COM, HO – VS	-	-	0.1	V	$I_o=0A$
$V_{OH}$	High level out put voltage VCC – LO, VB – HO	-	-	1.4		$I_o=0A$
$t_r$	Turn-on rise time	-	15	-	ns	
$t_f$	Turn-off fall time	-	10	-		
Ton_1	High and low side turn-on propagation delay, floating inputs	-	95	-		$V_{DT} = V_{CC}$ , $V_S = 100V$ , $V_{SS} = 100V$
Toff_1	High and low side turn-off propagation delay, floating inputs	-	80	-		$V_{DT} = V_{CC}$ , $V_S = 100V$ , $V_{SS} = 100V$
Ton_2	High and low side turn-on propagation delay, non-floating inputs	-	95	-		$V_{DT} = V_{CC}$ , $V_S = 100V$ , $V_{SS} = COM$
Toff_2	High and low side turn-off propagation delay, non-floating inputs	-	80	-		$V_{DT} = V_{CC}$ , $V_S = 100V$ , $V_{SS} = COM$
DT1	Deadtime: LO turn-off to HO turn-on ( $DT_{LO-HO}$ ) & HO turn-off to LO turn-on ( $DT_{HO-LO}$ )	8	15	22		$V_{DT} > V_{DT1}$ , $V_{SS} = COM$
DT2	Deadtime: LO turn-off to HO turn-on ( $DT_{LO-HO}$ ) & HO turn-off to LO turn-on ( $DT_{HO-LO}$ )	15	25	35		$V_{DT1} > V_{DT} > V_{DT2}$ , $V_{SS} = COM$
DT3	Deadtime: LO turn-off to HO turn-on ( $DT_{LO-HO}$ ) & HO turn-off to LO turn-on ( $DT_{HO-LO}$ )	20	35	50		$V_{DT2} > V_{DT} > V_{DT3}$ , $V_{SS} = COM$
DT4	Deadtime: LO turn-off to HO turn-on ( $DT_{LO-HO}$ ) & HO turn-off to LO turn-on ( $DT_{HO-LO}$ ) $V_{DT} = V_{DT4}$	50	80	110		$V_{DT3} > V_{DT}$ , $V_{SS} = COM$
$V_{DT1}$	DT mode select threshold 1	0.51xVcc	0.57xVcc	0.63xVcc		V
$V_{DT2}$	DT mode select threshold 2	0.32xVcc	0.36xVcc	0.40xVcc		
$V_{DT3}$	DT mode select threshold 3	0.21xVcc	0.23xVcc	0.25xVcc		



**Functional Block Diagram**



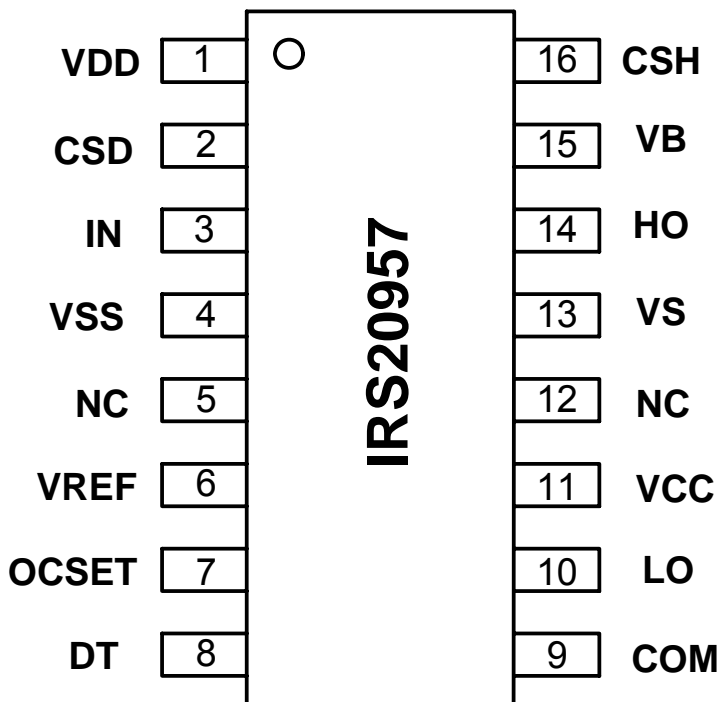
**I/O Pin Equivalent Circuit Diagrams**



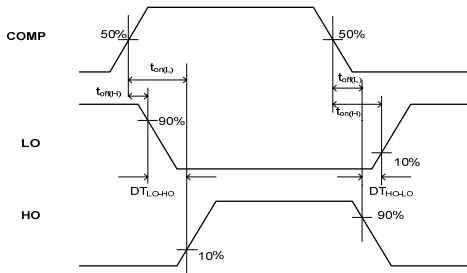
**Lead Definitions**

Pin #	Symbol	Description
1	VDD	Floating input positive supply
2	CSD	Shutdown timing capacitor, referenced to VSS
3	IN	PWM non-inverting input, in phase with HO
4	VSS	Floating input supply return
5	NC	
6	VREF	5V reference output for setting OCSET
7	OCSET	Low side over current threshold setting, referenced to COM
8	DT	Input for programmable dead-time, referenced to COM
9	COM	Low side supply return
10	LO	Low side output
11	VCC	Low side logic supply
12	NC	
13	VS	High side floating supply return
14	HO	High side output
15	VB	High side floating supply
16	CSH	High side over current sensing input, referenced to VS

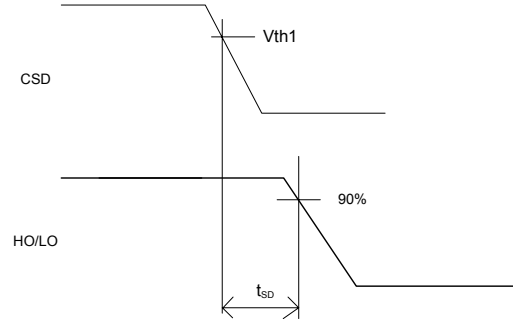
**Lead Assignments**



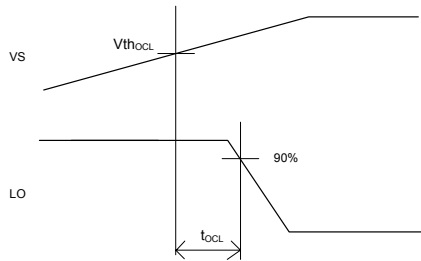
**Waveform definitions**



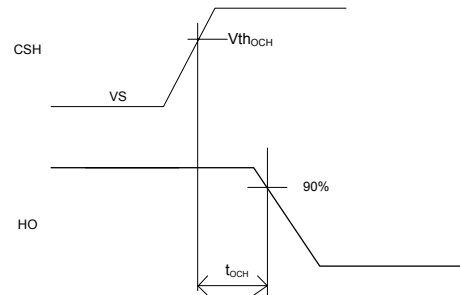
**Figure 1: Switching Time Waveform Definitions**



**Figure 2: CSD to Shutdown Waveform Definitions**



**Figure 3:  $V_S > V_{thOCL}$  to Shutdown Waveform**

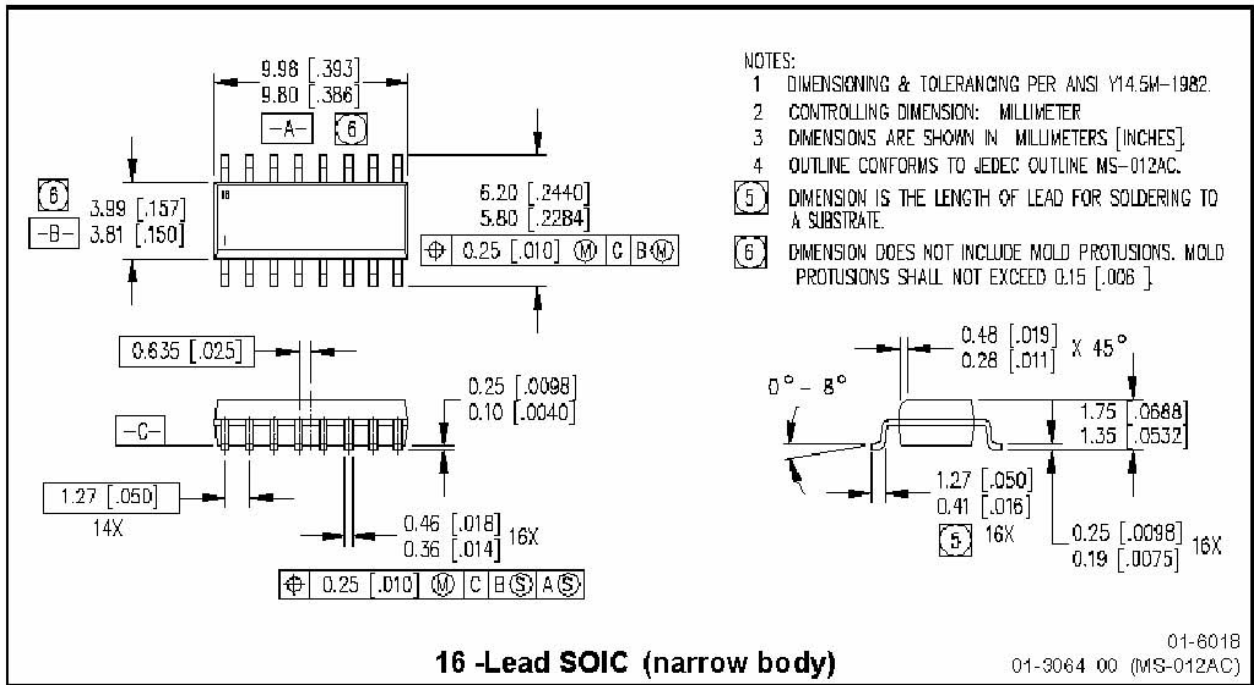


**Figure 4:  $V_{CSH} > V_{thOCH}$  to Shutdown Waveform**

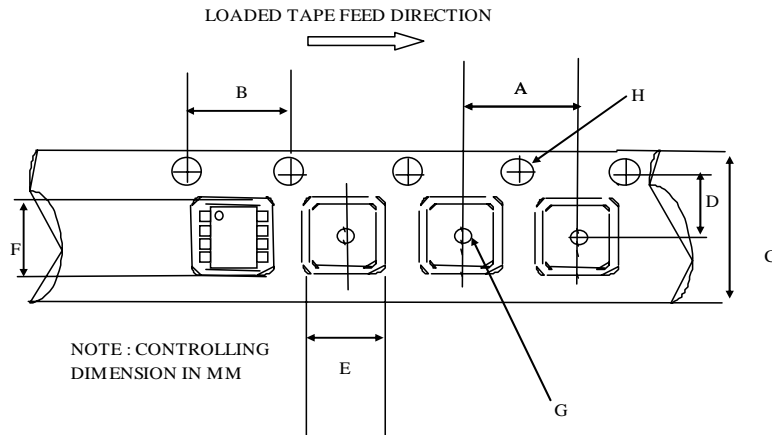
**Application information and additional information**

Please refer to AN-1144 for IRS20957 functional description.

**Package Details: SOIC16N**

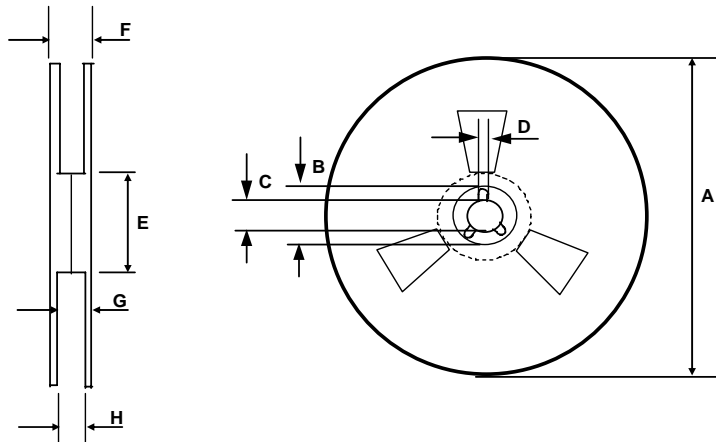


**Package Details: SOIC16N, Tape and Reel**



**CARRIER TAPE DIMENSION FOR 16SOICN**

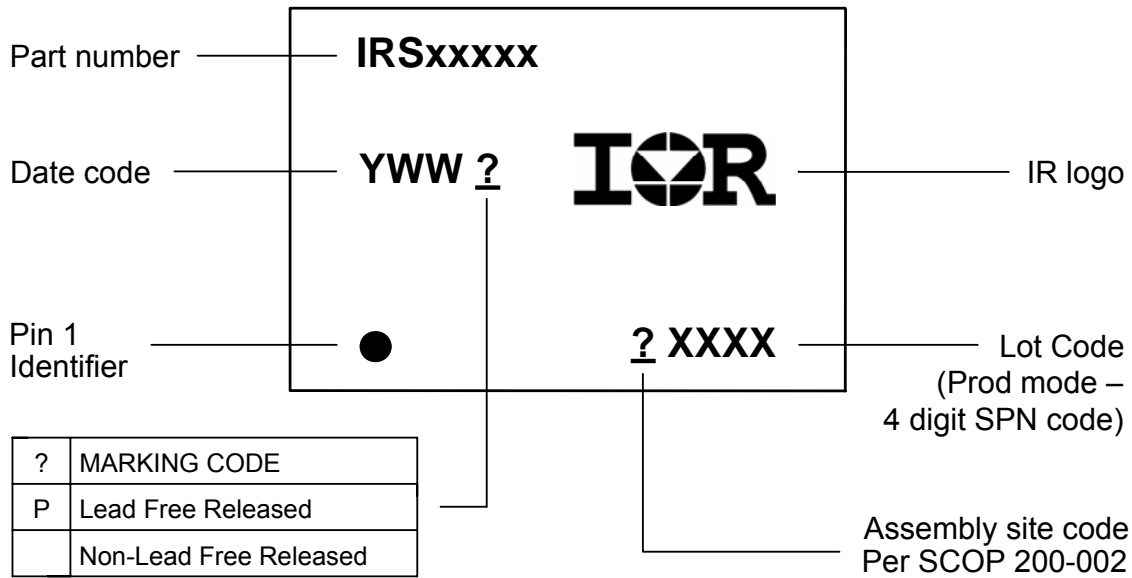
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	10.20	10.40	0.402	0.409
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



**REEL DIMENSIONS FOR 16SOICN**

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

**Part Marking Information**



**Ordering Information**

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS20957S	SOIC16N	Tube/Bulk	45	IRS20957SPBF
		Tape and Reel	2500	IRS20957STRPBF

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