

**70A, 60V, 0.014 Ohm, N-Channel Power MOSFETs**

These are N-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA78440.

**Ordering Information**

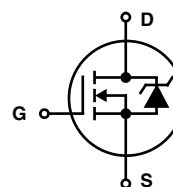
PART NUMBER	PACKAGE	BRAND
RFG70N06	TO-247	RFG70N06
RFP70N06	TO-220AB	RFP70N06
RF1S70N06	TO-262AA	F1S70N06
RF1S70N06SM	TO-263AB	F1S70N06

NOTE: When ordering use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, e.g. RF1S70N06SM9A.

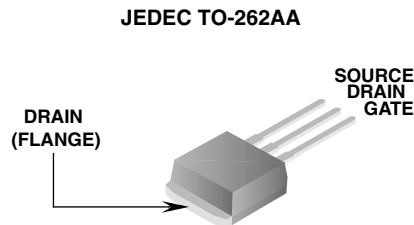
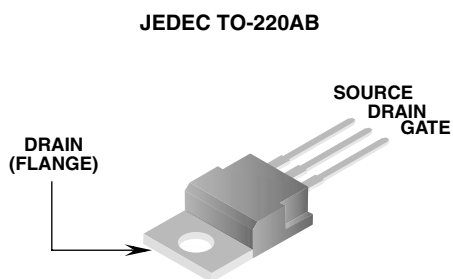
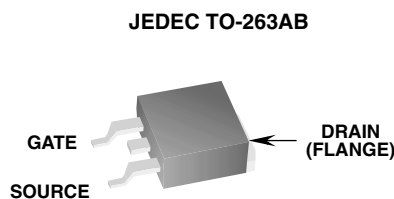
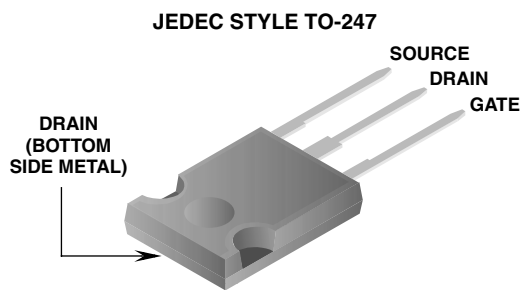
**Features**

- 70A, 60V
- $r_{DS(on)} = 0.014\Omega$
- Temperature Compensated PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve (Single Pulse)
- 175°C Operating Temperature
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

**Symbol**



**Packaging**



# RFG70N06, RFP70N06, RF1S70N06, RF1S70N06SM

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	RFG70N06, RFP70N06 RF1S70N06, RF1S70N06SM	UNITS
Drain to Source Voltage (Note 1) . . . . .	60	V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . .	60	V
Continuous Drain Current . . . . .	70	A
Pulsed Drain Current (Note 3) . . . . .	Refer to Peak Current Curve	
Gate to Source Voltage . . . . .	$\pm 20$	V
Single Pulse Avalanche Rating . . . . .	Refer to UIS Curve	A
Power Dissipation . . . . .	150	W
Linear Derating Factor . . . . .	1.0	$W/^\circ\text{C}$
Operating and Storage Temperature . . . . .	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s. . . . .	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	260	$^\circ\text{C}$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

1.  $T_J = 25^\circ\text{C}$  to  $150^\circ\text{C}$ .

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$ (Figure 11)	60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$ (Figure 10)	2	-	4	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{V}$ , $V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ , $T_C = 150^\circ\text{C}$	-	-	25	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 70\text{A}$ , $V_{GS} = 10\text{V}$ (Figure 9)	-	-	0.014	$\Omega$
Turn-On Time	$t_{(ON)}$	$V_{DD} = 30\text{V}$ , $I_D \approx 70\text{A}$ , $R_L = 0.43\Omega$ , $V_{GS} = 10\text{V}$ , $R_{GS} = 2.5\Omega$ (Figure 13)	-	-	125	ns
Turn-On Delay Time	$t_{d(ON)}$		-	12	-	ns
Rise Time	$t_r$		-	50	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	40	-	ns
Fall Time	$t_f$		-	15	-	ns
Turn-Off Time	$t_{(OFF)}$		-	-	125	ns
Total Gate Charge	$Q_g(TOT)$		$V_{GS} = 0\text{V}$ to $20\text{V}$	-	185	215
Gate Charge at 10V	$Q_g(10)$	$V_{GS} = 0\text{V}$ to $10\text{V}$	-	100	115	nC
Threshold Gate Charge	$Q_g(TH)$	$V_{GS} = 0\text{V}$ to $2\text{V}$	-	5.5	6.5	nC
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$ (Figure 12)	-	3000	-	pF
Output Capacitance	$C_{OSS}$		-	900	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	300	-	pF
Thermal Resistance, Junction to Case	$R_{\theta JC}$		-	-	1.0	$^\circ\text{C/W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	TO-220 and TO-263	-	-	62	$^\circ\text{C/W}$
		TO-247	-	-	30	$^\circ\text{C/W}$

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 70\text{A}$		-	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 70\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$		-	125	ns

**NOTES:**

2. Pulse test: pulse width  $\leq 300\text{ms}$ , duty cycle  $\leq 2\%$ .
3. Repetitive rating: pulse width is limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3) and Peak Current Capability Curve (Figure 5).

Typical Performance Curves  $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

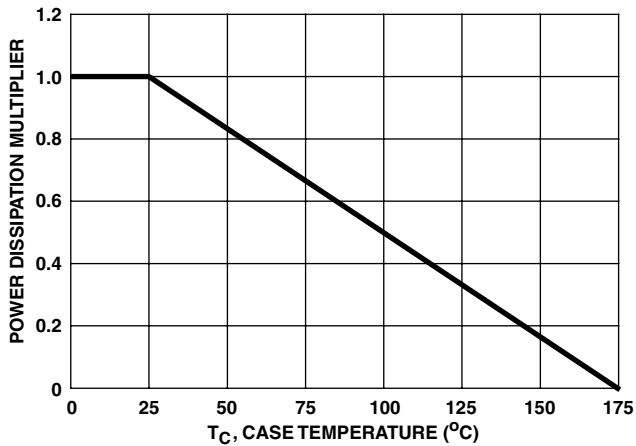


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

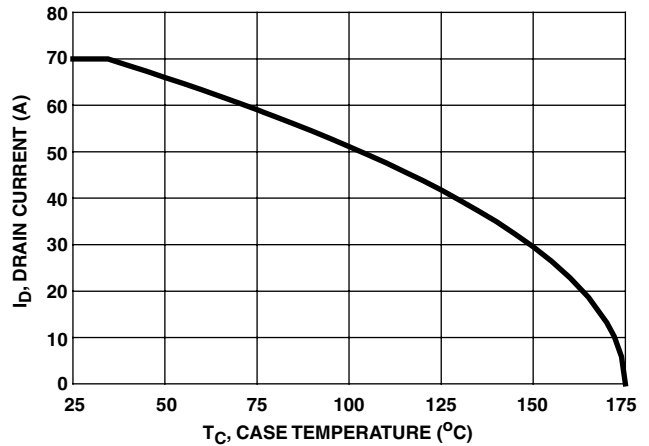


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

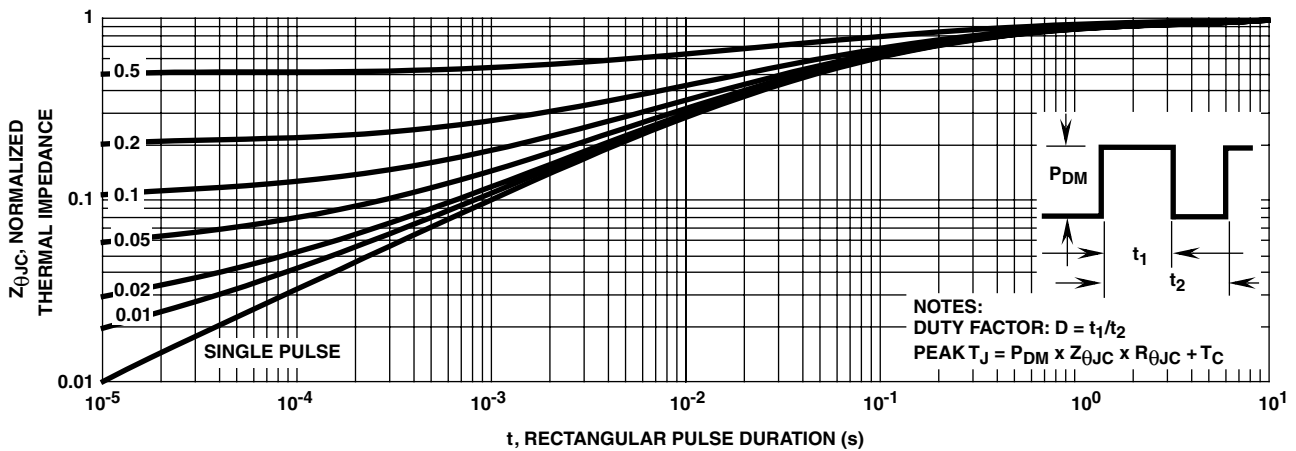


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

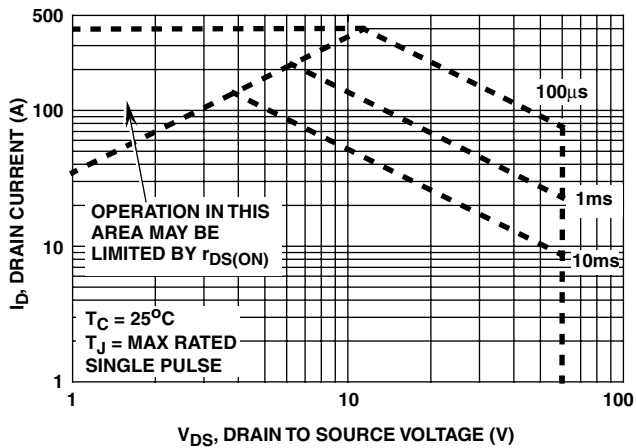


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

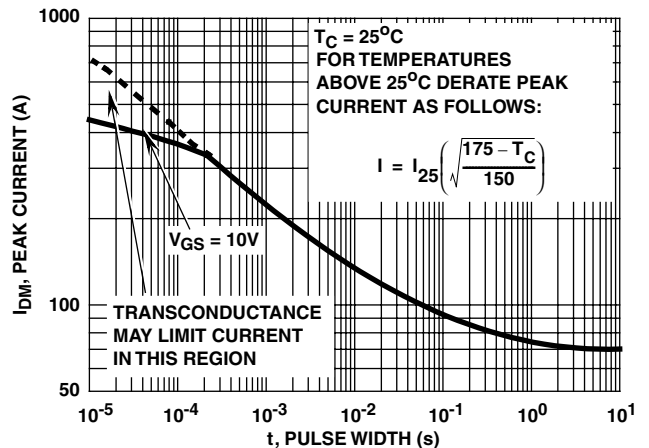
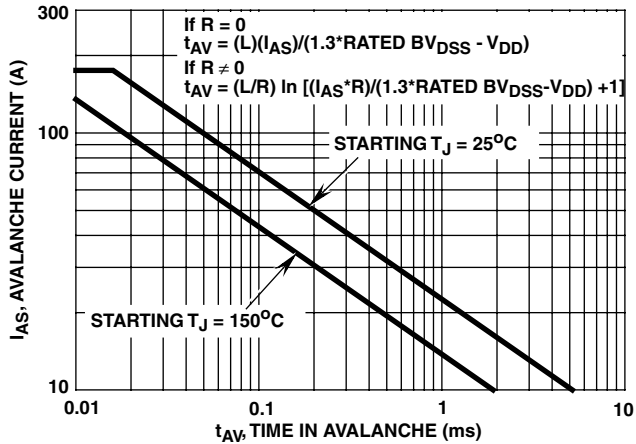
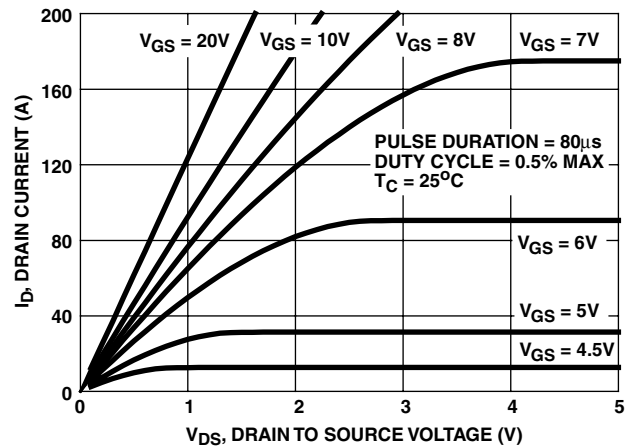


FIGURE 5. PEAK CURRENT CAPABILITY

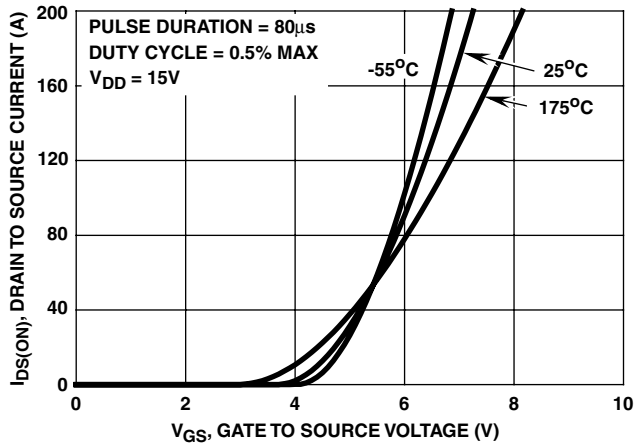
Typical Performance Curves  $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified (Continued)



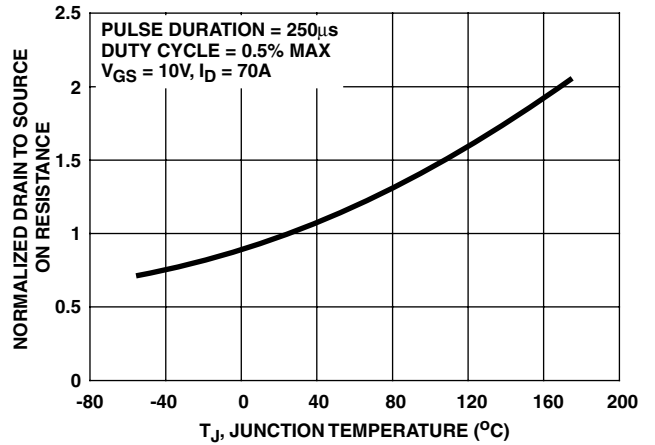
NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.  
**FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY**



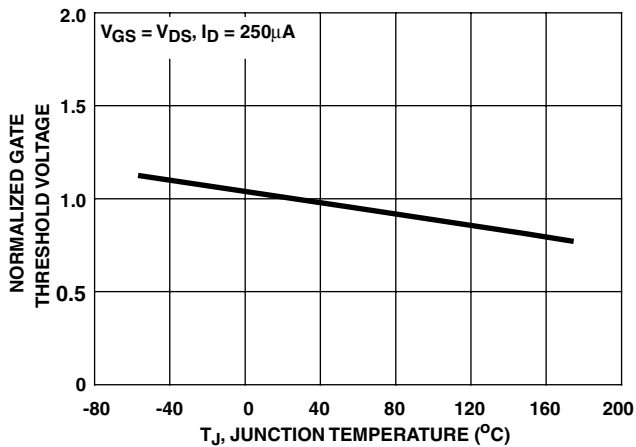
**FIGURE 7. SATURATION CHARACTERISTICS**



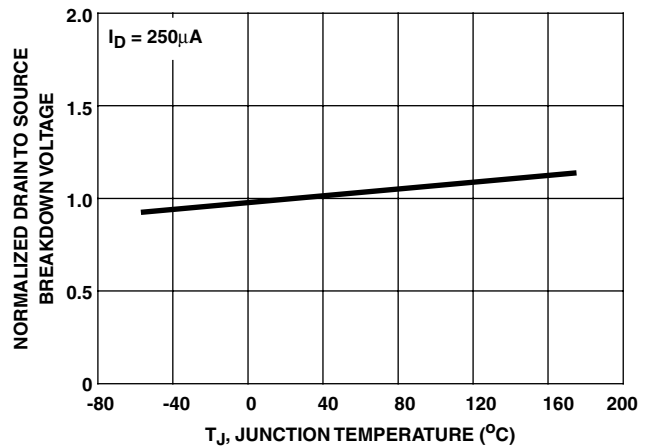
**FIGURE 8. TRANSFER CHARACTERISTICS**



**FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE**



**FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE**



**FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE**

**Typical Performance Curves**  $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified (Continued)

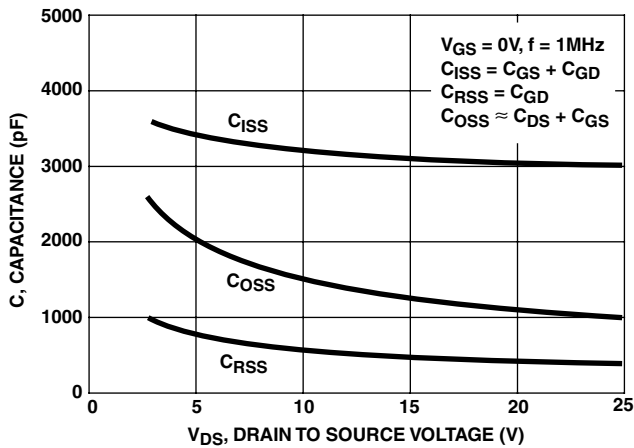
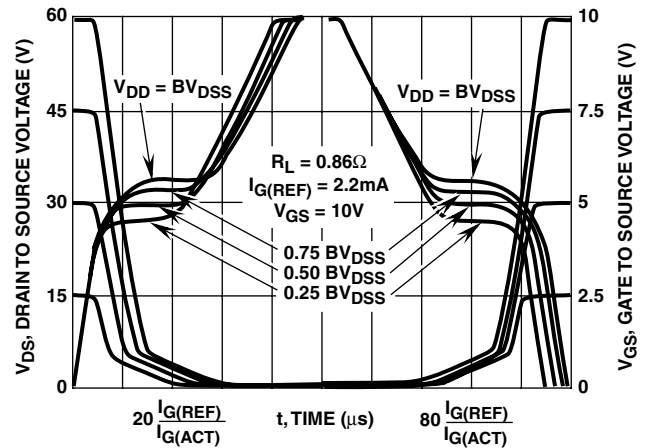


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

**Test Circuits and Waveforms**

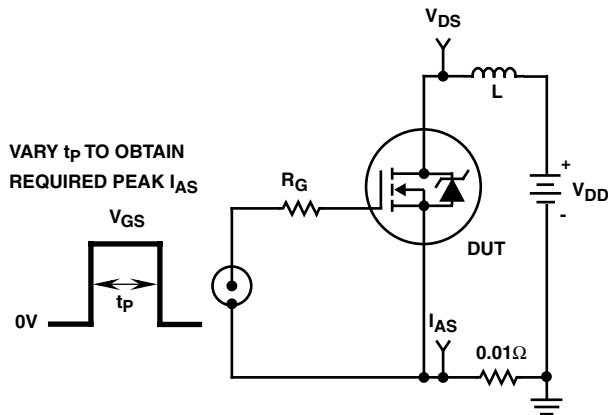


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

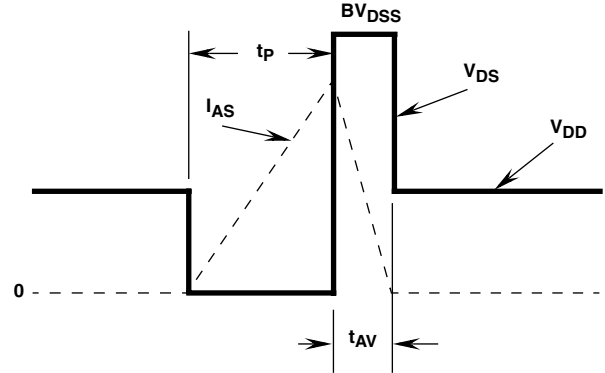


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

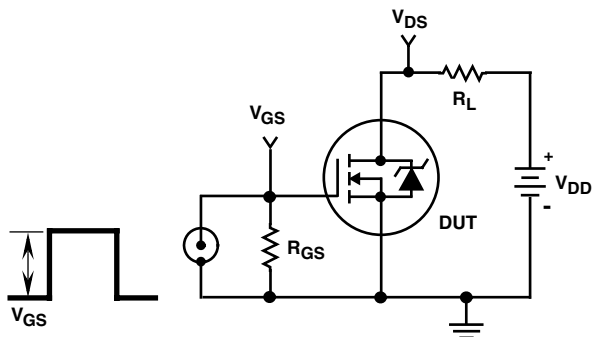


FIGURE 16. SWITCHING TIME TEST CIRCUIT

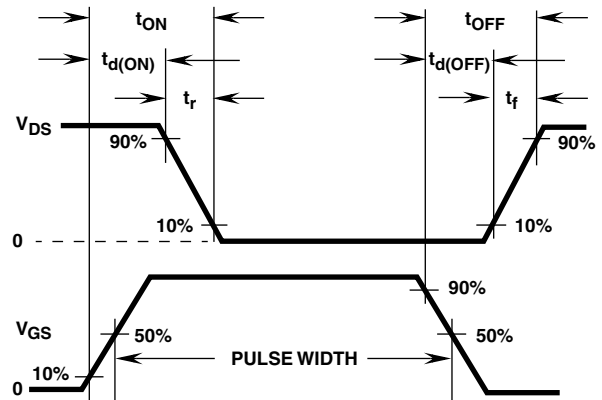


FIGURE 17. SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

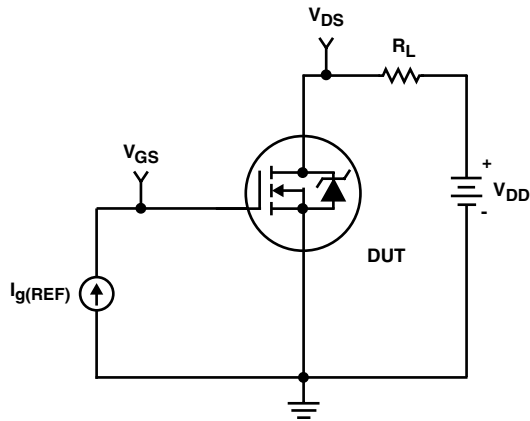


FIGURE 18. GATE CHARGE TEST CIRCUIT

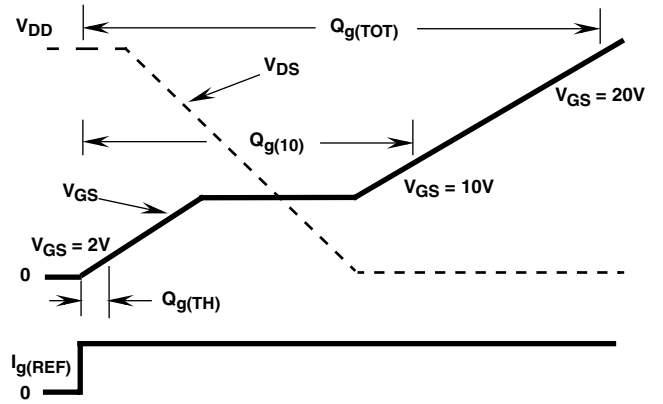


FIGURE 19. GATE CHARGE WAVEFORM

**PSPICE Electrical Model**

.SUBCKT RFG70N06 2 1 3 ; rev 3/20/92

CA 12 8 5.56e-9  
 CB 15 14 5.30e-9  
 CIN 6 8 2.63e-9

DBODY 7 5 DBDMOD  
 DBREAK 5 11 DBKMOD  
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 65.18  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 6 8 1  
 EVTO 20 6 18 8 1

IT 8 17 1

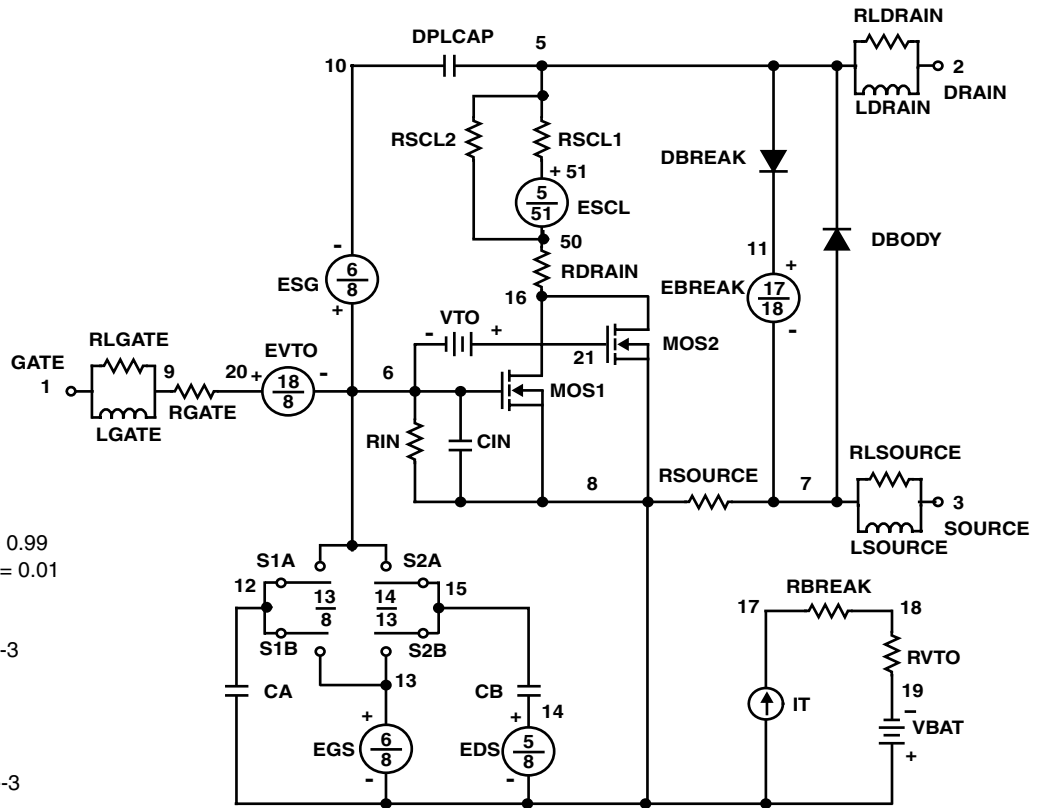
LDRAIN 2 5 1e-9  
 LGATE 1 9 3.10e-9  
 LSOURCE 3 7 1.82e-9

MOS1 16 6 8 8 MOSMOD M = 0.99  
 MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1  
 RDRAIN 50 16 RDSMOD 4.66e-3  
 RLDRAIN 2 5 10  
 RGATE 9 20 1.21  
 RLGATE 1 9 31  
 RIN 6 8 1e9  
 RSOURCE 8 7 RDSMOD 3.92e-3  
 RLSOURCE 3 7 18.2  
 RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1  
 VTO 21 6 0.605



.MODEL DBDMOD D (IS = 7.91e-12 RS = 3.87e-3 TRS1 = 2.71e-3 TRS2 = 2.50e-7 CJO = 4.84e-9 TT = 4.51e-8)  
 .MODEL DBKMOD D (RS = 3.9e-2 TRS1 = 1.05e-4 TRS2 = 3.11e-5)  
 .MODEL DPLCAPMOD D (CJO = 4.8e-9 IS = 1e-30 N = 10)  
 .MODEL MOSMOD NMOS (VTO = 3.46 KP = 47 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)  
 .MODEL RBKMOD RES (TC1 = 8.46e-4 TC2 = -8.48e-7)  
 .MODEL RDSMOD RES (TC1 = 2.23e-3 TC2 = 6.56e-6)  
 .MODEL RVTOMOD RES (TC1 = -3.29e-3 TC2 = 3.49e-7)  
 .MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -8.35 VOFF = -6.35)  
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.35 VOFF = -8.35)  
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.0 VOFF = 3.0)  
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 3.0 VOFF = -2.0)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

## TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE <sub>x</sub> <sup>TM</sup>	FAST <sup>®</sup>	OPTOLOGIC <sup>TM</sup>	SMART START <sup>TM</sup>	VCX <sup>TM</sup>
Bottomless <sup>TM</sup>	FAST <sub>r</sub> <sup>TM</sup>	OPTOPLANAR <sup>TM</sup>	STAR*POWER <sup>TM</sup>	
CoolFET <sup>TM</sup>	FRFET <sup>TM</sup>	PACMAN <sup>TM</sup>	Stealth <sup>TM</sup>	
CROSSVOLT <sup>TM</sup>	GlobalOptoisolator <sup>TM</sup>	POP <sup>TM</sup>	SuperSOT <sup>TM</sup> -3	
DenseTrench <sup>TM</sup>	GTO <sup>TM</sup>	Power247 <sup>TM</sup>	SuperSOT <sup>TM</sup> -6	
DOMET <sup>TM</sup>	HiSeC <sup>TM</sup>	PowerTrench <sup>®</sup>	SuperSOT <sup>TM</sup> -8	
EcoSPARK <sup>TM</sup>	ISOPLANAR <sup>TM</sup>	QFET <sup>TM</sup>	SyncFET <sup>TM</sup>	
E <sup>2</sup> CMOS <sup>TM</sup>	LittleFET <sup>TM</sup>	QST <sup>TM</sup>	TinyLogic <sup>TM</sup>	
EnSigna <sup>TM</sup>	MicroFET <sup>TM</sup>	QT Optoelectronics <sup>TM</sup>	TruTranslation <sup>TM</sup>	
FACT <sup>TM</sup>	MicroPak <sup>TM</sup>	Quiet Series <sup>TM</sup>	UHC <sup>TM</sup>	
FACT Quiet Series <sup>TM</sup>	MICROWIRE <sup>TM</sup>	SILENT SWITCHER <sup>®</sup>	UltraFET <sup>®</sup>	

STAR\*POWER is used under license

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.