PCA9509

Level translating I^{2}C-bus/SMBus repeater

Rev. 01 — 27 June 2006 **Product data sheet**

1. General description

The PCA9509 is a level translating I^{2}C-bus/SMBus repeater that enables processor low voltage 2-wire serial bus to interface with standard I^{2}C-bus or SMBus I/O. While retaining all the operating modes and features of the I^{2}C-bus system during the level shifts, it also permits extension of the I^{2}C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enabling the I^{2}C-bus or SMBus maximum capacitance of 400 pF on the higher voltage side. The SDA and SCL pins are over-voltage tolerant and are high-impedance when the PCA9509 is unpowered.

The bus port B drivers are compliant with SMBus I/O levels, while port A uses a current sensing mechanism to detect the input or output LOW signal which prevents bus lock-up. Port A uses a 1 mA current source for pull-up and a 200 Ω pull-down driver. This results in a LOW on the port A accommodating smaller voltage swings. The output pull-down on the port A internal buffer LOW is set for approximately 0.2 V, while the input threshold of the internal buffer is set about 50 mV lower than that of the output voltage LOW. When the port A I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the port B drives a hard LOW and the input level is set at 0.3 of SMBus or I^{2}C-bus voltage level which enables port B to connect to any other I^{2}C-bus devices or buffer.

The PCA9509 drivers are not enabled unless $V_{CC(A)}$ is above 0.8 V and $V_{CC(B)}$ is above 2.5 V. The enable (EN) pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the EN pin when the bus is idle.

2. Features

- Bidirectional buffer isolates capacitance and allows 400 pF on port B of the device
- Voltage level translation from port A (1 V to $V_{CC(B)}$ – 1.0 V) to port B (3.0 V to 5.5 V)
- Requires no external pull-up resistors on lower voltage port A
- Active HIGH repeater enable input
- Open-drain inputs/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates Standard-mode and Fast-mode I^{2}C-bus devices and multiple masters
- Powered-off high-impedance I^{2}C-bus pins
- Operating supply voltage range of 1.0 V to $V_{CC(B)}$ – 1.0 V on port A, 3.0 V to 5.5 V on port B
- 5 V tolerant port B SCL, SDA and enable pins

- 0 Hz to 400 kHz clock frequency

  Remark: The maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater.
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: TSSOP8, SO8

3. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9509DP	9509	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCA9509D	PCA9509	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Functional diagram

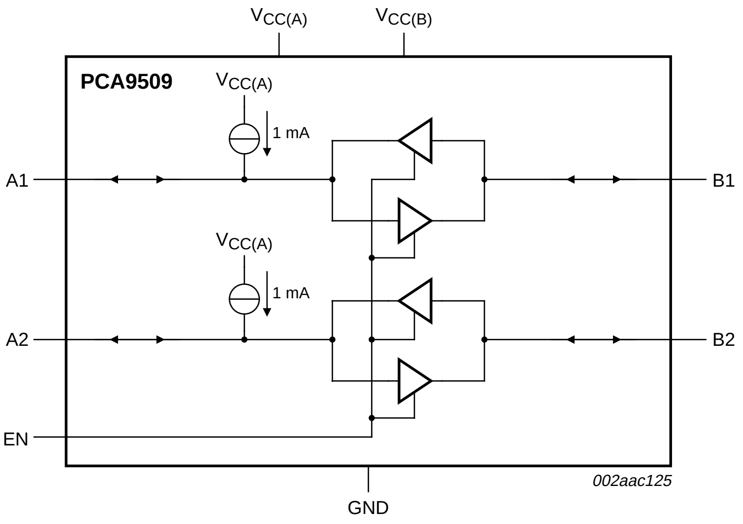


Fig 1. Functional diagram of PCA9509

5. Pinning information

5.1 Pinning

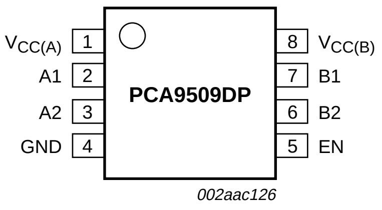


Fig 2. Pin configuration for TSSOP8

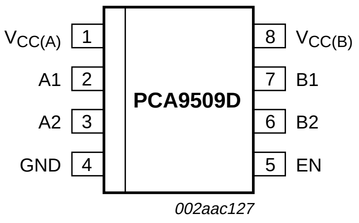


Fig 3. Pin configuration for SO8

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	port A power supply
A1[1]	2	port A (lower voltage side)
A2[1]	3	port A
GND	4	ground (0 V)
EN	5	enable input (active HIGH)
B2[1]	6	port B (SMBus/I²C-bus side)
B1[1]	7	port B
$V_{CC(B)}$	8	port B power supply

[1] Port A and port B can be used for either SCL or SDA.

6. Functional description

Refer to Figure 1 “Functional diagram of PCA9509”.

The PCA9509 enables I²C-bus or SMBus translation down to $V_{CC(A)}$ as low as 1.0 V without degradation of system performance. The PCA9509 contains 2 bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage and 3.3 V SMBus or 5 V I²C-bus. The port B I/Os are over-voltage tolerant to 5.5 V even when the device is unpowered.

The PCA9509 includes a power-up circuit that keeps the output drivers turned off until $V_{CC(B)}$ is above 2.5 V and the $V_{CC(A)}$ is above 0.8 V. $V_{CC(B)}$ and $V_{CC(A)}$ can be applied in any sequence at power-up. After power-up and with the EN pin HIGH, a LOW level on port A (below approximately 0.15 V) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to about 0 V. When port A rises above approximately 0.15 V, the port B pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When port B falls first and goes below $0.3V_{CC(B)}$, the port A driver is turned on and port A pulls down to 0.2 V (typical). The port B pull-down is not enabled unless the port A voltage goes below V_{ILc}. If the port A low voltage goes below V_{ILc}, the port B pull-down driver is enabled until port A rises above approximately 0.15 V (V_{ILc}), then port B, if not externally driven LOW, will continue to rise being pulled up by the external pull-up resistor.

Remark: Ground offset between the PCA9509 ground and the ground of devices on port A of the PCA9509 must be avoided.

The reason for this cautionary remark is that a CMOS/NMOS open-drain capable of sinking 3 mA of current at 0.4 V will have an output resistance of 133 Ω or less (R = E / I). Such a driver will share enough current with the port A output pull-down of the PCA9509 to be seen as a LOW as long as the ground offset is zero. If the ground offset is greater than 0 V, then the driver resistance must be less. Since V_{ILc} can be as low as 90 mV at cold temperatures and the low end of the current distribution, the maximum ground offset should not exceed 50 mV.

Bus repeaters that use an output offset are not interoperable with the port A of the PCA9509 as their output LOW levels will not be recognized by the PCA9509 as a LOW. If the PCA9509 is placed in an application where the V_{IL} of port A of the PCA9509 does not go below its V_{ILc} it will pull port B LOW initially when port A input transitions LOW but the port B will return HIGH, so it will not reproduce the port A input on port B. Such applications should be avoided.

Port B is interoperable with all I^{2}C-bus slaves, masters and repeaters.

6.1 Enable

The EN pin is active HIGH and allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I^{2}C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I^{2}C-bus parts being enabled.

The enable pin should only change state when the bus and the repeater port are in an idle state to prevent system failures.

6.2 I^{2}C-bus systems

As with the standard I^{2}C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I^{2}C-bus). The size of these pull-up resistors depends on the system. Each of the port A I/Os has an internal pull-up current source and does not require the external pull-up resistor. Port B is designed to work with Standard-mode and Fast-mode I^{2}C-bus devices in addition to SMBus devices. Standard-mode I^{2}C-bus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I^{2}C-bus system where Standard-mode devices and multiple masters are possible. Under certain conditions higher termination currents can be used.

7. Application design-in information

A typical application is shown in Figure 4. In this example, the CPU is running on a 1.1 V I^2C-bus while the master is connected to a 3.3 V bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

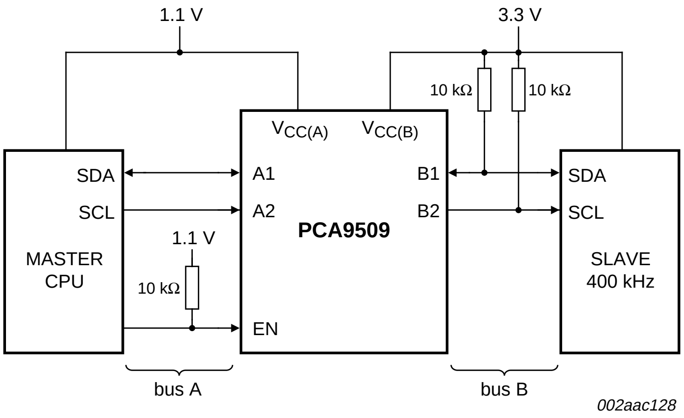


Fig 4. Typical application

When port B of the PCA9509 is pulled LOW by a driver on the I^2C-bus, a CMOS hysteresis detects the falling edge when it goes below $0.3V_{CC(B)}$ and causes the internal driver on port A to turn on, causing port A to pull down to about 0.2 V. When port A of the PCA9509 falls, first a comparator detects the falling edge and causes the internal driver on port B to turn on and pull the port B pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 5 and Figure 6. If the bus master in Figure 4 were to write to the slave through the PCA9509, waveforms shown in Figure 5 would be observed on the B bus. This looks like a normal I^2C-bus transmission.

On the A bus side of the PCA9509, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PCA9509. After the 8th clock pulse, the data line will be pulled to the V_{OL} of the master device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the PCA9509 for a short delay while the B bus side rises above $0.5V_{CC(B)}$, then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the A bus side at the input of the PCA9509 (V_{IL}) is below V_{ILc} to be recognized by the PCA9509 and then transmitted to the B bus side.

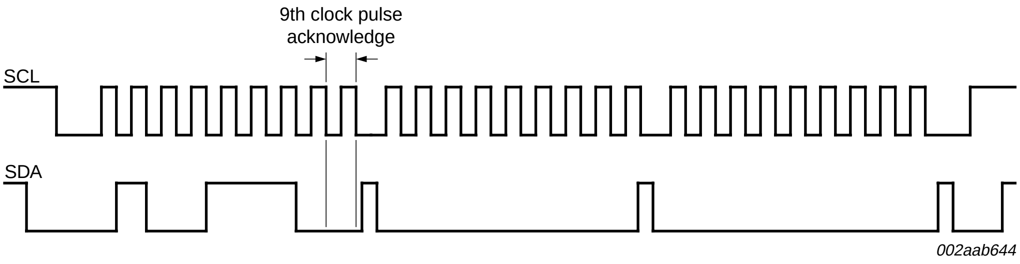


Fig 5. Bus B SMBus/I^2C-bus waveform

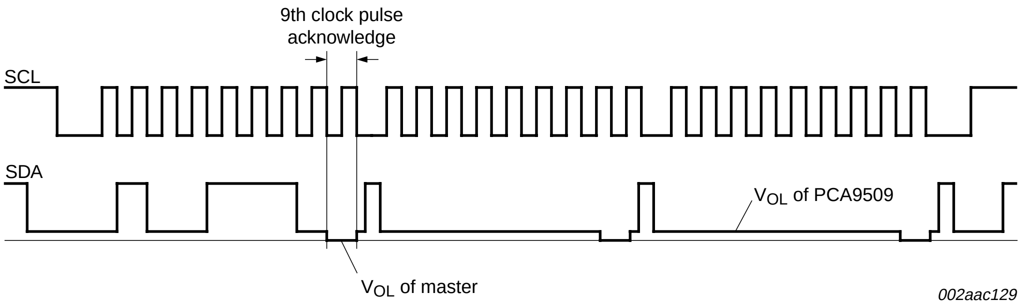


Fig 6. Bus A lower voltage waveform

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(B)}$	supply voltage port B		–0.5	+6.0	V
$V_{CC(A)}$	supply voltage port A		–0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin	port A	–0.5	+6.0	V
		port B; enable pin (EN)	–0.5	+6.0	V
$I_{I/O}$	input/output current		-	±20	mA
I_I	input current		-	±20	mA
P_{tot}	total power dissipation		-	100	mW
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature	operating in free air	–40	+85	°C
T_j	junction temperature		-	+125	°C
T_{sp}	solder point temperature	10 s max.	-	300	°C

9. Static characteristics

Table 4. Static characteristics

GND = 0 V; T_{amb} = –40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Supplies						
$V_{CC(B)}$	supply voltage port B		3.0	-	5.5	V
$V_{CC(A)}$	supply voltage port A		1.0	-	$V_{CC(B)} - 1$	V
$I_{CC(A)}$	supply current port A	all port A static HIGH	0.25	0.45	0.9	mA
		all port A static LOW	1.25	3.0	5	mA
$I_{CC(B)}$	supply current port B	all port B static HIGH	0.5	0.9	1.1	mA
Input and output of port A (A1 to A2)						
V_{IH}	HIGH-level input voltage	port A	$0.7V_{CC(A)}$	-	$V_{CC(A)}$	V
V_{IL}	LOW-level input voltage	port A [2]	–0.5	-	+0.3	V
V_{ILc}	contention LOW-level input voltage	[2]	–0.5	+0.15	-	V
V_{IK}	input clamping voltage	I_L = –18 mA	–1.5	-	–0.5	V
I_{LI}	input leakage current	$V_I = V_{CC(A)}$	-	-	±1	µA
I_{IL}	LOW-level input current	[3]	–1.5	–1.0	–0.45	mA
V_{OL}	LOW-level output voltage	[4]	-	0.2	0.35	V
$V_{OL}–V_{ILc}$	difference between LOW-level output and LOW-level input voltage contention	[5]	-	50	-	mV
I_{LOH}	HIGH-level output leakage current	V_O = 1.1 V	-	-	10	µA
C_{io}	input/output capacitance		-	6	7	pF
Input and output of port B (B1 to B2)						
V_{IH}	HIGH-level input voltage	port B	$0.7V_{CC(B)}$	-	$V_{CC(B)}$	V
V_{IL}	LOW-level input voltage	port B	–0.5	-	$+0.3V_{CC(B)}$	V
V_{IK}	input clamping voltage	I_L = –18 mA	–1.5	-	–0.5	V
I_{LI}	input leakage current	V_I = 3.6 V	–1.0	-	+1.0	µA
I_{IL}	LOW-level input current	V_I = 0.2 V	-	-	10	µA
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA	-	0.1	0.2	V
I_{LOH}	HIGH-level output leakage current	V_O = 3.6 V	-	-	10	µA
C_{io}	input/output capacitance		-	3	5	pF
Enable						
V_{IL}	LOW-level input voltage		–0.5	-	$+0.1V_{CC(A)}$	V
V_{IH}	HIGH-level input voltage		$0.9V_{CC(A)}$	-	$V_{CC(B)}$	V
$I_{IL(EN)}$	LOW-level input current on pin EN	V_I = 0.2 V, EN; V_{CC} = 3.6 V	–1	-	+1	µA
I_{LI}	input leakage current		–1	-	+1	µA
C_i	input capacitance	V_I = 3.0 V or 0 V	-	2	3	pF

[1] Typical values with $V_{CC(A)}$ = 1.1 V, $V_{CC(B)}$ = 5.0 V.

[2] V_{IL} specification is for the falling edge seen by the port A input. V_{ILc} is for the static LOW levels seen by the port A input resulting in port B output staying LOW.

[3] The port A current source has a typical value of about 1 mA, but varies with both $V_{CC(A)}$ and $V_{CC(B)}$. Below $V_{CC(A)}$ of about 0.7 V the port A current source current drops to 0 mA. The current source current dropping across the internal pull-down driver resistance of about 200 Ω defines the V_{OL}.

[4] As long as the chip ground is common with the input ground reference the driver resistance may be as large as 120 Ω. However, ground offset will rapidly decrease the maximum allowed driver resistance.

[5] Guaranteed by design.

10. Dynamic characteristics

Table 5. Dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{CC(A)}$ = 1.1 V; $V_{CC(B)}$ = 3.3 V							
t_{PLH}	LOW-to-HIGH propagation delay	port B to port A	[1]	69	109	216	ns
t_{PHL}	HIGH-to-LOW propagation delay	port B to port A	[1]	63	86	140	ns
t_{TLH}	LOW to HIGH output transition time	port A	[1]	14	22	96	ns
t_{THL}	HIGH to LOW output transition time	port A	[1]	5	8.1	16	ns
t_{PLH}	LOW-to-HIGH propagation delay	port A to port B	[1]	–69	–91	–139	ns
t_{PLH2}	LOW to HIGH propagation delay 2	port A to port B; measured from the 50 % of initial LOW on port A to 1.5 V rising on port B	[1]	91	153	226	ns
t_{PHL}	HIGH-to-LOW propagation delay	port A to port B	[1]	73	122	183	ns
t_{TLH}	LOW to HIGH output transition time	port B	[1][2]	-	61	-	ns
t_{THL}	HIGH to LOW output transition time	port B	[1]	15	24	40	ns
t_{su}	setup time	EN HIGH before START condition		100	-	-	ns
t_h	hold time	EN HIGH after STOP condition		100	-	-	ns
$V_{CC(A)}$ = 1.9 V; $V_{CC(B)}$ = 5.0 V							
t_{PLH}	LOW-to-HIGH propagation delay	port B to port A	[1]	69	105	216	ns
t_{PHL}	HIGH-to-LOW propagation delay	port B to port A	[1]	63	86	140	ns
t_{TLH}	LOW to HIGH output transition time	port A	[1]	14	27	96	ns
t_{THL}	HIGH to LOW output transition time	port A	[1]	5	8	35	ns
t_{PLH}	LOW-to-HIGH propagation delay	port A to port B	[1]	–69	–89	–139	ns
t_{PLH2}	LOW to HIGH propagation delay 2	port A to port B; measured from the 50 % of initial LOW on port A to 1.5 V rising on port B	[1]	91	131	226	ns
t_{PHL}	HIGH-to-LOW propagation delay	port A to port B	[1]	73	99	183	ns
t_{TLH}	LOW to HIGH output transition time	port B	[1][2]	-	65	-	ns
t_{THL}	HIGH to LOW output transition time	port B	[1]	15	31	40	ns
t_{su}	setup time	EN HIGH before START condition		100	-	-	ns
t_h	hold time	EN HIGH after STOP condition		100	-	-	ns

[1] Load capacitance = 50 pF; load resistance on port B = 1.35 kΩ.

[2] Value is determined by RC time constant of bus line.

10.1 AC waveforms

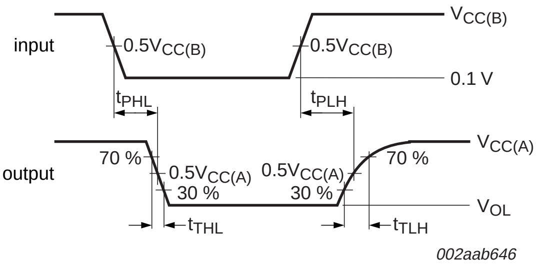


Fig 7. Propagation delay and transition times; port B to port A

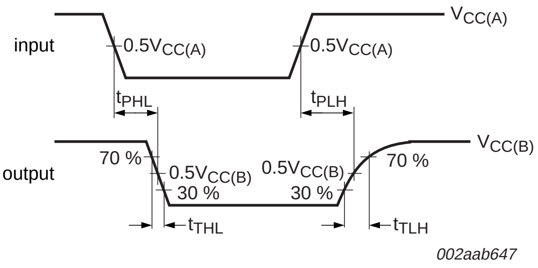


Fig 8. Propagation delay and transition times; port A to port B

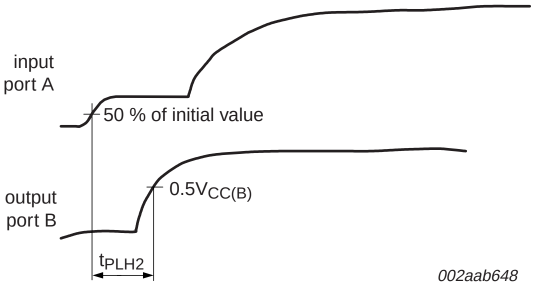
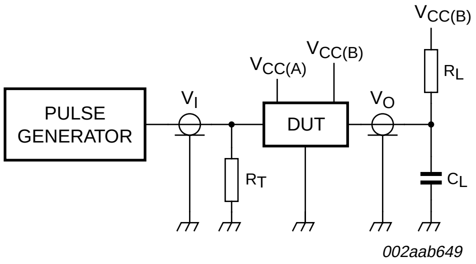


Fig 9. Propagation delay from the port A's external driver switching off to port B LOW-to-HIGH transition; port A to port B

11. Test information



R$_L$ = load resistor; 1.35 kΩ on port B

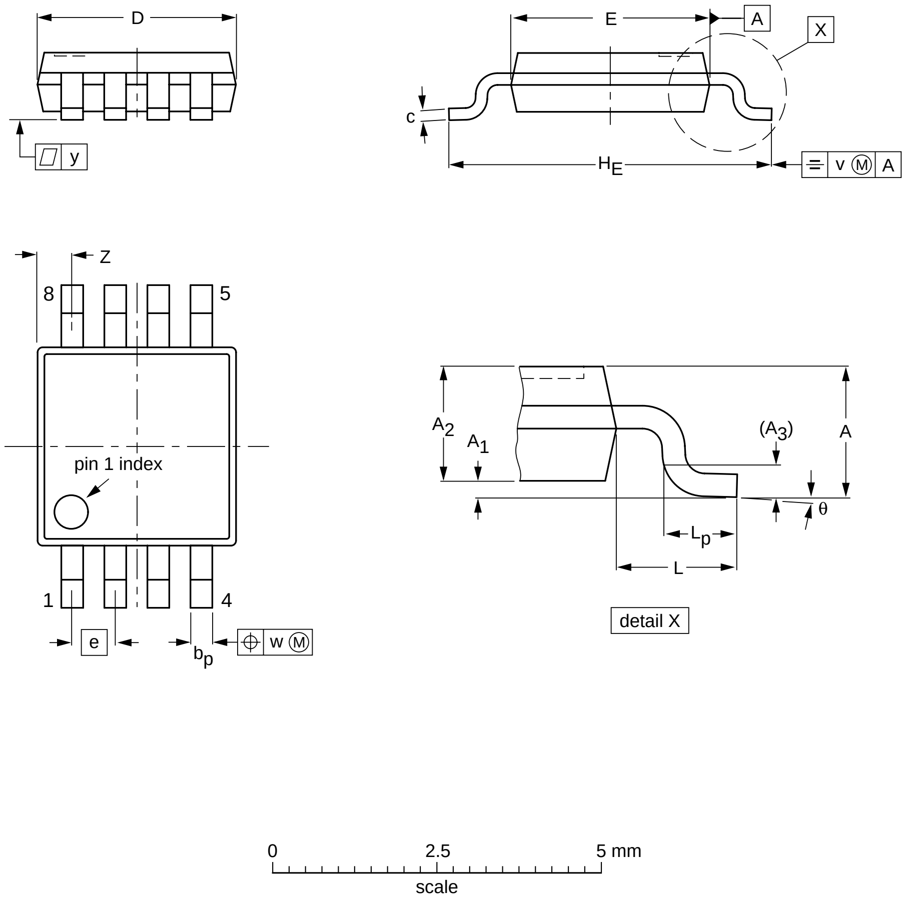
C$_L$ = load capacitance includes jig and probe capacitance; 50 pF

R$_T$ = termination resistance should be equal to Z$_o$ of pulse generators

Fig 10. Test circuit for open-drain outputs

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

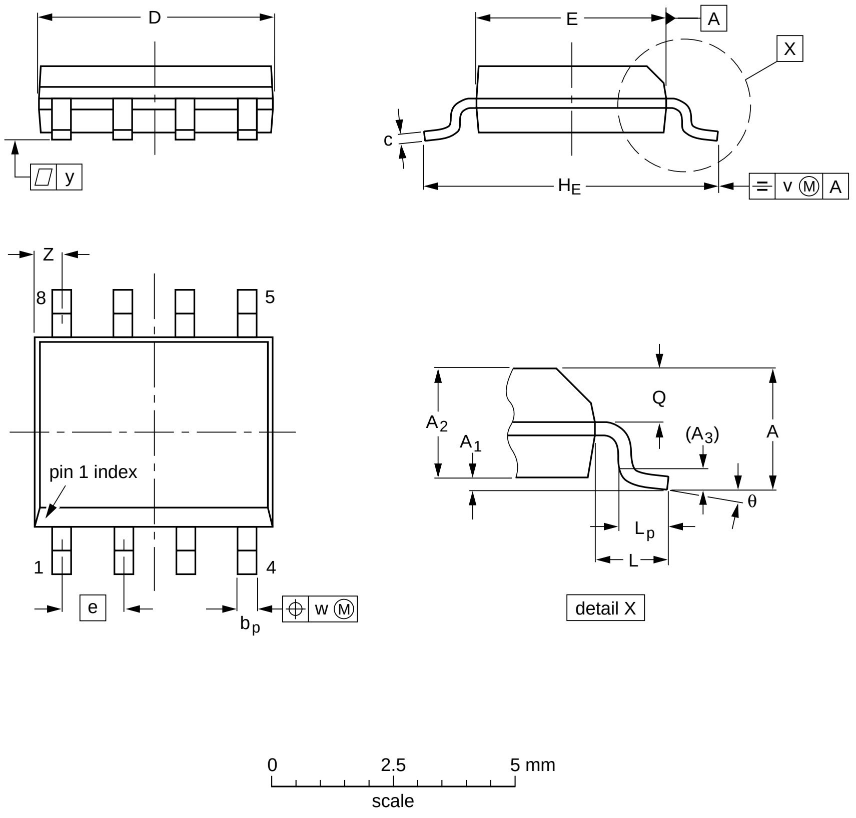
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 11. Package outline SOT505-1 (TSSOP8)

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A$_1$	A$_2$	A$_3$	b$_p$	c	D$^{(1)}$	E$^{(2)}$	e	H$_E$	L	L$_p$	Q	v	w	y	Z$^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

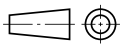
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 12. Package outline SOT96-1 (SO8)

13. Soldering

13.1 Introduction to soldering surface mount packages

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow temperatures range from 215 °C to 260 °C depending on solder paste material. The peak top-surface temperature of the packages should be kept below:

Table 6. SnPb eutectic process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
< 2.5 mm	240 °C + 0/–5 °C	225 °C + 0/–5 °C
≥ 2.5 mm	225 °C + 0/–5 °C	225 °C + 0/–5 °C

Table 7. Pb-free process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 350 to 2000	Volume mm^3 > 2000
< 1.6 mm	260 °C + 0 °C	260 °C + 0 °C	260 °C + 0 °C
1.6 mm to 2.5 mm	260 °C + 0 °C	250 °C + 0 °C	245 °C + 0 °C
≥ 2.5 mm	250 °C + 0 °C	245 °C + 0 °C	245 °C + 0 °C

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):

  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

13.5 Package related soldering information

Table 8. Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	**Soldering method**	
	Wave	**Reflow**[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

14. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
ESD	ElectroStatic Discharge
HBM	Human Body Model
I/O	Input/Output
I^2C-bus	Inter-Integrated Circuit bus
MM	Machine Model
NMOS	Negative-channel Metal Oxide Semiconductor
RC	Resistor-Capacitor network
SMBus	System Management Bus

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9509_1	20060627	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	**Product status**[3]	**Definition**
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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18. Contents

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