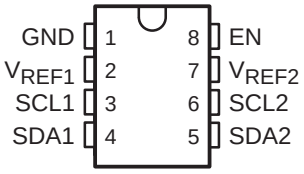
DUAL BIDIRECTIONAL I^2C BUS AND SMBus VOLTAGE-LEVEL TRANSLATOR

SCPS113 – OCTOBER 2004

- **2-Bit Bidirectional Translator for SDA and SCL Lines in Mixed-Mode I^2C Applications**
- **I^2C and SMBus Compatible**
- **Less Than 1.5-ns Maximum Propagation Delay to Accommodate Standard-Mode and Fast-Mode I^2C Devices and Multiple Masters**
- **Allows Voltage-Level Translator Between**
  - **1.2-V V_{REF1} and 2.5-V, 3.3-V, or 5-V V_{REF2}**
  - **1.8-V V_{REF1} and 3.3-V or 5-V V_{REF2}**
  - **2.5-V V_{REF1} and 5-V V_{REF2}**
  - **3.3-V V_{REF1} and 5-V V_{REF2}**
- **Provides Bidirectional Voltage Translation With No Direction Pin**
- **Low 3.5-Ω ON-State Connection Between Input and Output Ports Provides Less Signal Distortion**
- **Open-Drain I^2C I/O Ports (SCL1, SDA1, SCL2, and SDA2)**
- **5-V Tolerant I^2C I/O Ports to Support Mixed-Mode Signal Operation**
- **High Impedance SCL1, SDA1, SCL2, and SDA2 Pins for EN = Low**
- **Lock-Up Free Operation for Isolation When EN = Low**
- **Flow-Through Pinout for Ease of Printed Circuit Board Trace Routing**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DCT OR DCU PACKAGE
(TOP VIEW)



PIN	SYMBOL	FUNCTION
1	GND	Ground, 0 V
2	V_{REF1}	Low-voltage side reference supply voltage for SCL1 and SDA1
3	SCL1	Serial clock, low-voltage side. Connect to V_{REF1} through a pullup resistor.
4	SDA1	Serial data, low-voltage side. Connect to V_{REF1} through a pullup resistor.
5	SDA2	Serial data, high-voltage side. Connect to V_{REF2} through a pullup resistor.
6	SCL2	Serial clock, high-voltage side. Connect to V_{REF2} through a pullup resistor.
7	V_{REF2}	High-voltage side reference supply voltage for SCL2 and SDA2
8	EN	Switch enable input. Connect to V_{REF2} and pulled up through a high resistor.

description/ordering information

This dual bidirectional I²C and SMBus voltage-level translator with an enable (EN) input is operational from 1.2-V to 3.3-V V_{REF1} and 2.5-V to 5.5-V V_{REF2}.

The PCA9306 allows bidirectional voltage translations between 1.2 V and 5 V, without the use of a direction pin. The low ON-state resistance (r_{on}) of the switch allows connections to be made with minimal propagation delay. When EN is high, the translator switch is ON, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is low, the translator switch is off, and a high-impedance state exists between ports.

In I²C applications, the bus capacitance limit of 400 pF restricts the number of devices and bus length. Using the PCA9306 enables the system designer to isolate two halves of a bus, thus more I²C devices or longer trace length can be accommodated.

The PCA9306 can also be used to run two buses, one at 400-kHz operating frequency and the other at 100-kHz operating frequency. If the two buses are operating at different frequencies, the 100-kHz bus must be isolated when the 400-kHz operation of the other bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater.

As with the standard I²C system, pullup resistors are required to provide the logic high levels on the translator's bus. The PCA9306 has a standard open-collector configuration of the I²C bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with standard-mode and fast-mode I²C devices in addition to SMBus devices. Standard-mode I²C devices only specify 3 mA in a generic I²C system where standard-mode devices and multiple masters are possible. Under certain conditions, high termination currents can be used.

When the SDA1 or SDA2 port is low, the clamp is in the ON state and a low resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is high, the voltage on the SDA1 port is limited to the voltage set by V_{REF1}. When the SDA1 port is high, the SDA2 port is pulled to the drain pullup supply voltage (V_{DPU}) by the pullup resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices and at the same time protect less ESD resistant devices.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	SSOP − DCT	Reel of 3000	PCA9306DCTR	7BD_ _ _
		Reel of 250	PCA9306DCTT	
	VSSOP − DCU	Reel of 3000	PCA9306DCUR	7BD_
		Reel of 250	PCA9306DCUT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

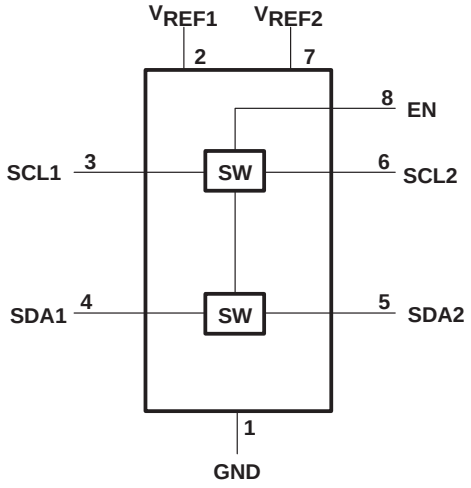
‡ DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.

FUNCTION TABLE

INPUT EN†	TRANSLATOR FUNCTION
H	SCL1 = SCL2, SDA1 = SDA2
L	Disconnect

† EN is controlled by the V_{REF2} logic levels and should be at least 1 V higher than V_{REF1} for best translator operation.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

DC reference voltage range, V_{REF1} . . . . . −0.5 V to 7 V
DC reference bias voltage range, V_{REF2} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 7 V
Input/output voltage range, $V_{I/O}$ (see Note 1) . . . . . −0.5 V to 7 V
Continuous channel current . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . −50 mA
Package thermal impedance, θ_{JA} (see Note 2): DCT package . . . . . 220°C/W
DCU package . . . . . 227°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	SCL1, SDA1, SCL2, SDA2	0	5	V
V_{REF1}‡	Reference voltage		0	5	V
V_{REF2}‡	Reference voltage		0	5	V
EN	Enable Input voltage		0	5	V
I_{PASS}	Pass switch current			64	mA
T_A	Operating free-air temperature		−40	85	°C

‡ $V_{REF1} \le V_{REF2} - 1$ V for best results in level-shifting applications

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP§	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA,	EN = 0 V				−1.2	V
I_{IH}	Input leakage current		V_I = 5 V,	EN = 0 V				5	μA
C_i(EN)	Input capacitance		V_I = 3 V or 0				11		pF
$C_{io(off)}$	Off capacitance	SCLn, SDAn	V_O = 3 V or 0,	EN = 0 V			4	6	pF
$C_{io(on)}$	On capacitance	SCLn, SDAn	V_O = 3 V or 0,	EN = 3 V			10.5	12.5	pF
r_{on}¶	On resistance	SCLn, SDAn	V_I = 0,	I_O = 64 mA	EN = 4.5 V		3.5	5.5	Ω
					EN = 3 V		4.7	7	
					EN = 2.3 V		6.3	9.5	
					EN = 1.5 V		25.5	32	
			V_I = 2.4 V	I_O = 15 mA	EN = 4.5 V		4.8	7.5	
					EN = 3 V		14.7	23	
			V_I = 1.7 V		EN = 2.3 V		11.3	16.5	

§ All typical values are at T_A = 25°C.
¶ Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two terminals.

ac performance (translating down)

switching characteristics over recommended operating free-air temperature range, EN = 3.3 V, V_{IH} = 3.3 V, V_{IL} = 0, and V_M = 1.15 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	0	0.8	0	0.6	0	0.3	ns
t_{PHL}			0	1.2	0	1	0	0.5	

switching characteristics over recommended operating free-air temperature range, EN = 2.5 V, V_{IH} = 2.5 V, V_{IL} = 0, and V_M = 0.75 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL2 or SDA2	SCL1 or SDA1	0	1	0	0.7	0	0.4	ns
t_{PHL}			0	1.3	0	1	0	0.6	

ac performance (translating up)

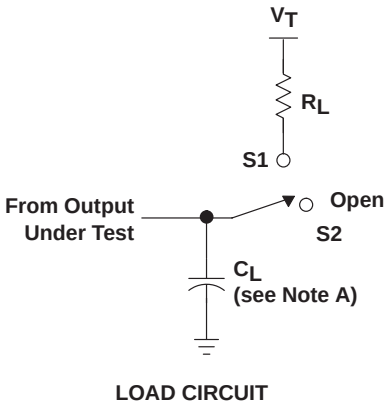
switching characteristics over recommended operating free-air temperature range, EN = 3.3 V, V_{IH} = 2.3 V, V_{IL} = 0, V_T = 3.3 V, V_M = 1.15 V, and R_L = 300 Ω (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL1 or SDA1	SCL2 or SDA2	0	0.9	0	0.6	0	0.4	ns
t_{PHL}			0	1.4	0	1.1	0	0.7	

switching characteristics over recommended operating free-air temperature range, EN = 2.5 V, V_{IH} = 1.5 V, V_{IL} = 0, V_T = 2.5 V, V_M = 0.75 V, and R_L = 300 Ω (unless otherwise noted) (see Figure 1)

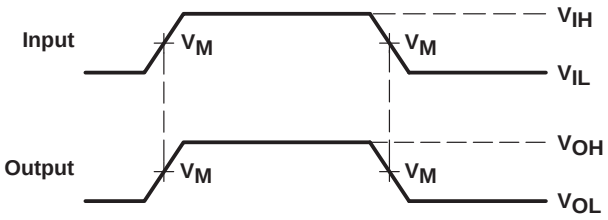
PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	SCL1 or SDA1	SCL2 or SDA2	0	1	0	0.6	0	0.4	ns
t_{PHL}			0	1.3	0	1.3	0	0.8	

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

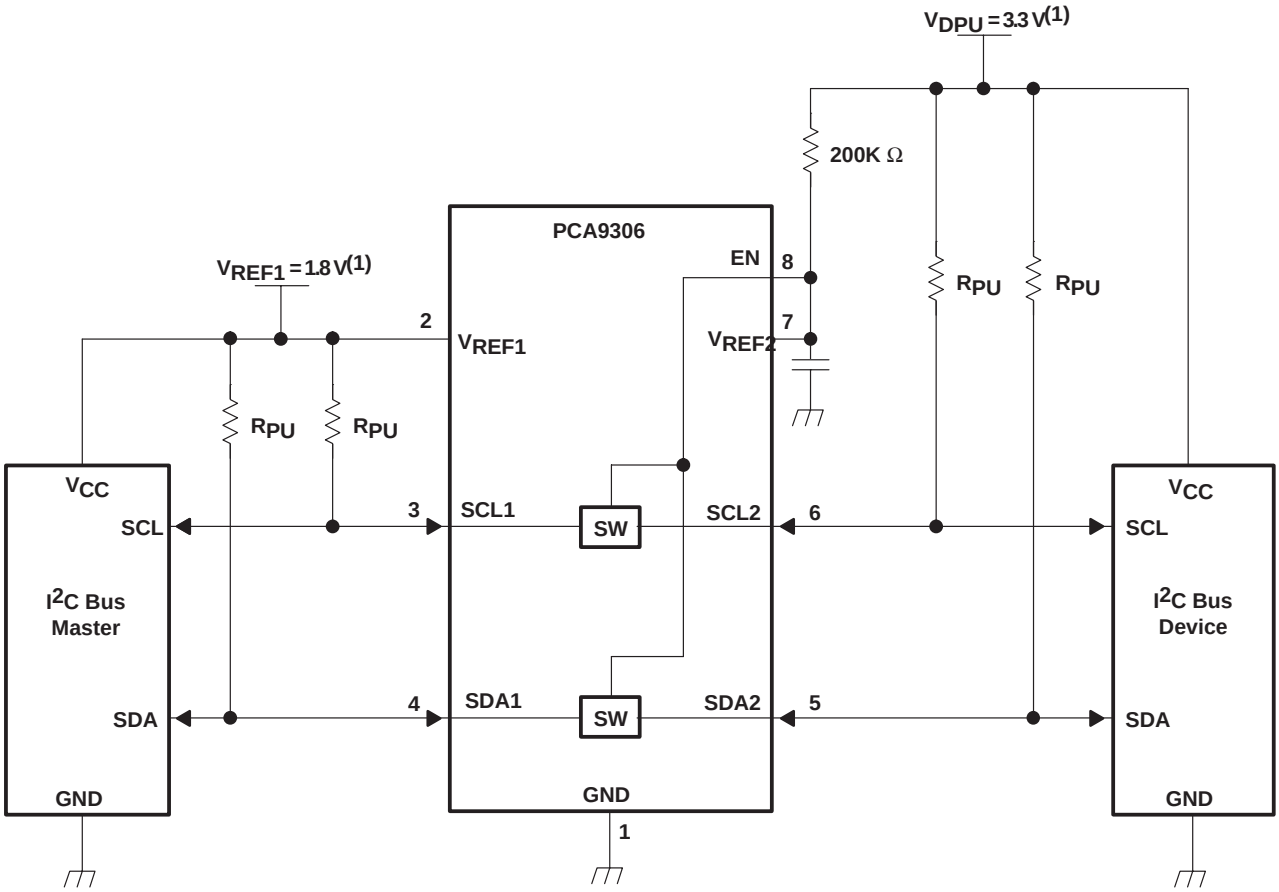
USAGE	SWITCH
Translating up	S1
Translating down	S2



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit for Outputs

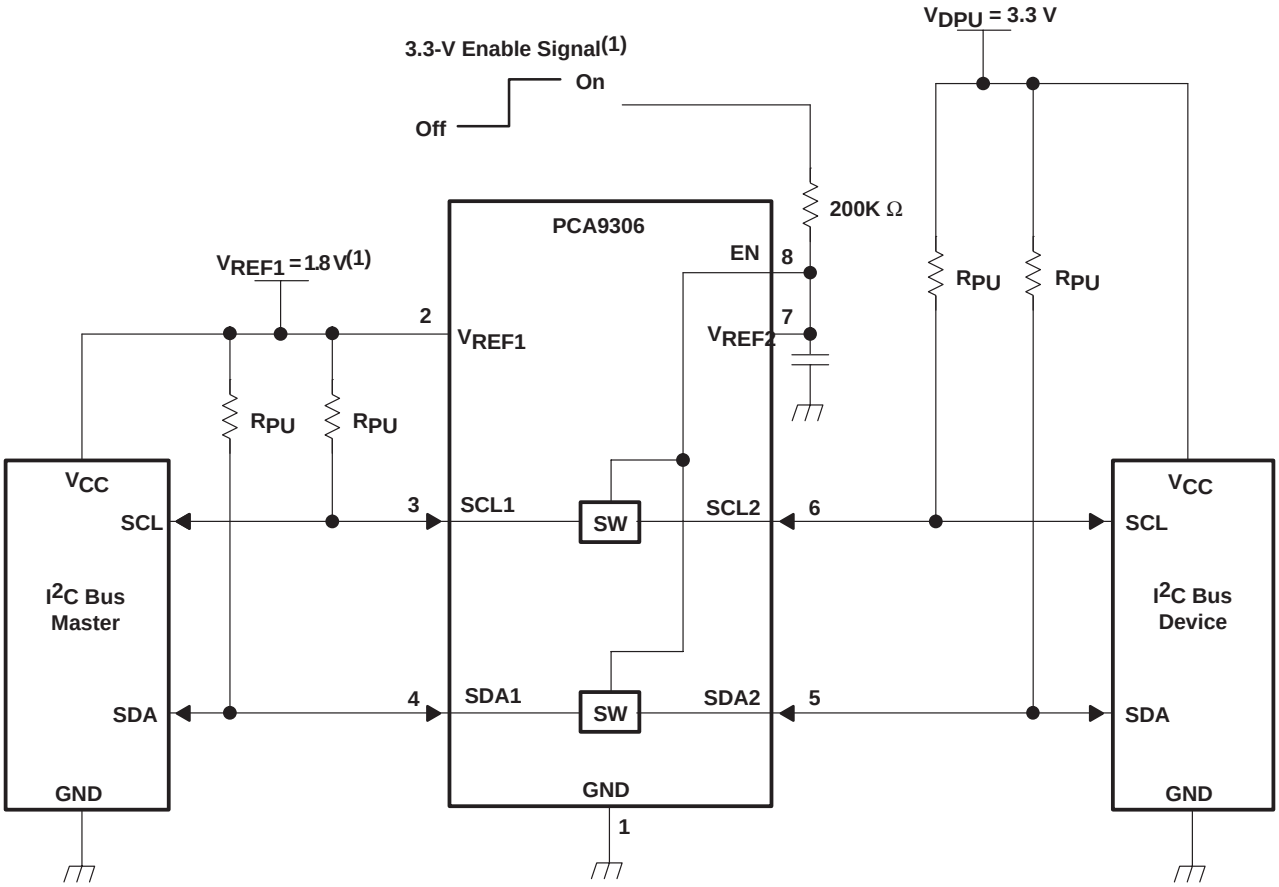
APPLICATION INFORMATION



(1) The applied voltages at V_{REF1} and V_{DPU} should be such that V_{REF2} is at least 1 V higher than V_{REF1} for best translator operation.

Figure 2. Typical Application Circuit (Switch Always Enabled)

APPLICATION INFORMATION



(1) In the enabled mode, the applied enable voltage and the applied voltage at V_{REF1} should be such that V_{REF2} is at least 1 V higher than V_{REF1} for best translator operation.

Figure 3. Typical Application Circuit (Switch Enable Control)

bidirectional translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to V_{REF2} and both pins pulled to high side V_{DPU} through a pullup resistor (typically 200 kΩ). This allows V_{REF2} to regulate the EN input. A filter capacitor on V_{REF2} is recommended. The I²C bus master output can be totem pole or open drain (pullup resistors may be required) and the I²C bus device output can be totem pole or open drain (pullup resistors are required to pull the SCL2 and SDA2 outputs to V_{DPU}). However, if either output is totem pole, data must be unidirectional or the outputs must be 3-statable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction. If both outputs are open drain, no direction control is needed.

The reference supply voltage (V_{REF1}) is connected to the processor core power supply voltage. When V_{REF2} is connected through a 200-kΩ resistor to a 3.3-V to 5.5-V V_{DPU} power supply, and V_{REF1} is set between 1.0 V and V_{DPU} −1 V, the output of each SCL1 and SDA1 has a maximum output voltage equal to V_{REF1}, and the output of each SCL2 and SDA2 has a maximum output voltage equal to V_{DPU}.

APPLICATION INFORMATION

application operating conditions (see Figure 2)

		MIN	TYP†	MAX	UNIT
V_{REF2}	Reference voltage	V_{REF1} + 0.6	2.1	5	V
EN	Enable input voltage	V_{REF1} + 0.6	2.1	5	V
V_{REF1}	Reference voltage	0	1.5	4.4	V
I_{PASS}	Pass switch current		14		mA
I_{REF}	Reference-transistor current		5		µA
T_A	Operating free-air temperature	−40		85	°C

† All typical values are at T_A = 25°C.

sizing pullup resistor

The pullup resistor value needs to limit the current through the pass transistor when it is in the on state to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the on state. To set the current through each pass transistor at 15 mA, the pullup resistor value is calculated as:

$$R_{PU} = \frac{V_{DPU} - 0.35\ V}{0.015\ A}$$

The following table summarizes resistor values reference voltages and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column or a larger value should be used to ensure that the pass voltage of the transistor would be 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the PCA9306 device at 0.175 V, although the 15 mA only applies to current flowing through the PCA9306 device.

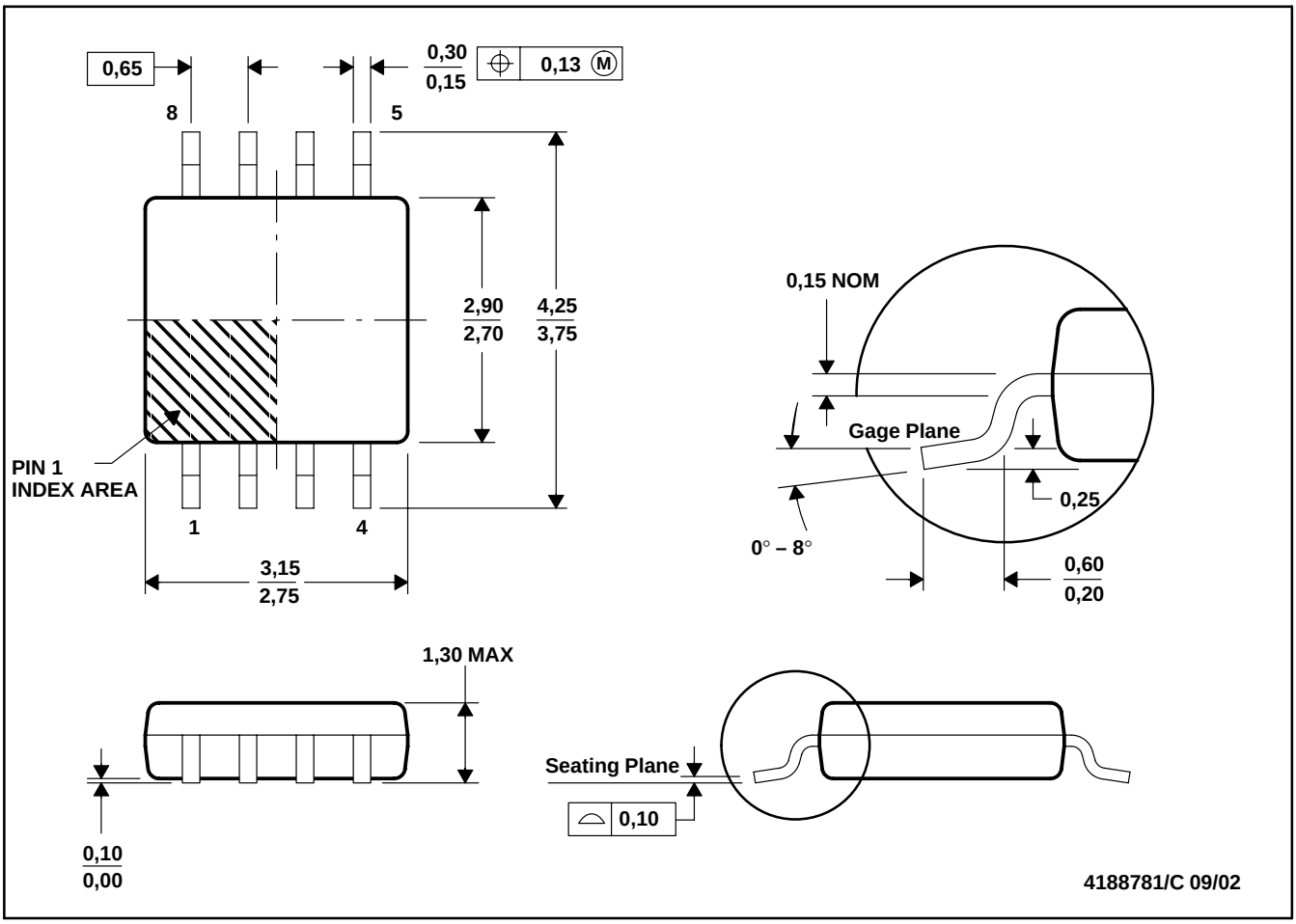
pullup resistor values‡§

PULLUP RESISTOR VALUE (Ω)						
V_{DPU}	15 mA		10 mA		3 mA	
	NOMINAL	+10%¶	NOMINAL	+10%¶	NOMINAL	+10%¶
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

‡ Calculated for V_{OL} = 0.35 V
§ Assumes output driver V_{OL} = 0.175 V at stated current
¶ +10% to compensate for V_{DD} range and resistor tolerance

MPDS049B – MAY 1999 – REVISED OCTOBER 2002

DCT (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. Falls within JEDEC MO-187 variation DA.

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