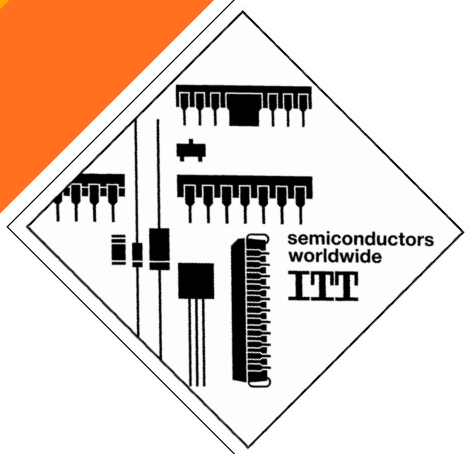

NVM 3060
4096-Bit EEPROM

Edition Feb. 14, 1990
6251-309-2/E

ITT Semiconductors

Contents

4096-Bit EEPROM

1. Introduction

Electrically erasable programmable read-only memory (EEPROM) in N-channel floating-gate technology with a capacity of 512 words, 8 bits each.

The NVM 3060 is intended for use as a reprogrammable non-volatile memory in conjunction with the CCU 2030/2050/2070/3000 series Central Control Units or the SAA 12xx and TVPO 2066 Remote Control and Tuning ICs. It serves for storing the tuning information as well as several analog settings, further alignment information given in the factory when producing the TV set. The stored information remains stored even with the supply voltages switched off. Reading and programming operations are executed via the IM bus (see section 5.). Input and output signals are TTL level. An address option input provides the possibility to operate two memories in parallel, to obtain a total storage capacity of 8192 bits.

The device contains an on-chip charge pump for high programming voltage generation and an on-chip clock oscillator.

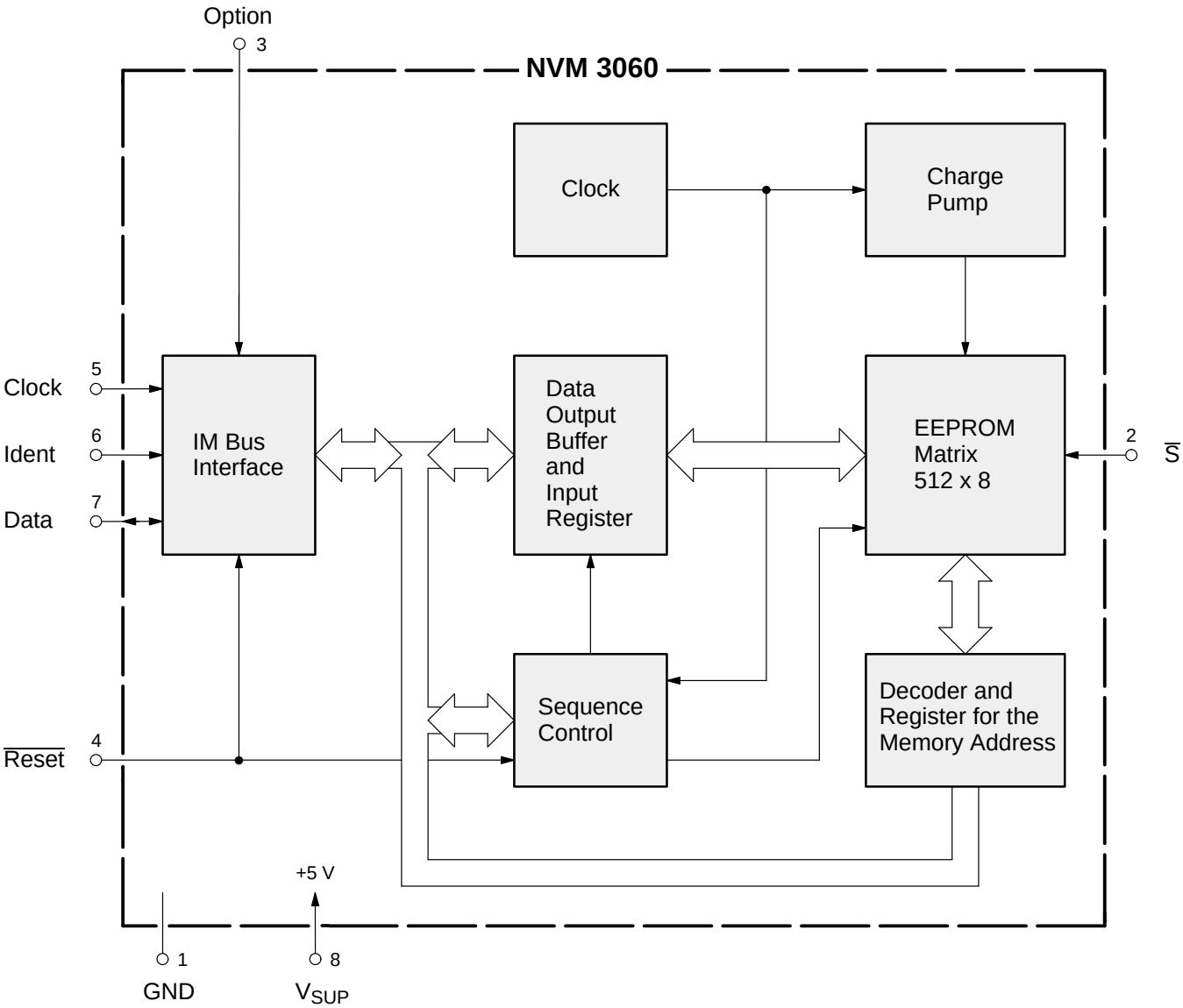

Fig. 1–1: Block diagram of the NVM 3060 EEPROM

2. Specifications

2.1. Outline Dimensions

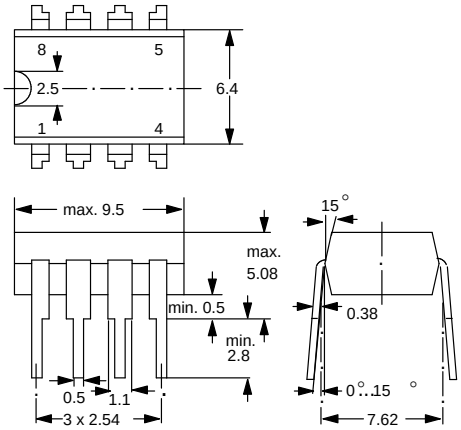

Fig. 2–1: NVM 3060 in 8-pin Dil Plastic Package 20 A 8 according to DIN 41870

Weight approx. 0.5 g Dimensions in mm

2.2. Pin Connections

1 Ground, 0

2 Safe Input $\overline{S}$

3 Option Input

4 $\overline{\text{Reset}}$ Input

5 IM Bus Clock Input

6 IM Bus Ident Input

7 IM Bus Data Input/Output

8 Supply Voltage V_{SUP}

2.3. Pin Descriptions

Pin 1 – Ground, 0
This pin must be connected to the negative of the supplies.

Pin 2 – Safe Input $\overline{S}$
Fig. 2–2 shows the internal configuration of this input. Normally, with pin 2 at ground potential (low), one portion of the programming matrix is protected so that this part of the memory cannot be reprogrammed inadvertently. Only when pin 2 receives high potential continuously, the protected portion of the memory matrix can be programmed. Pin 2 is internally tied to ground via a transistor equivalent to a 40 kΩ resistor.

Pin 3 – Option Input Fig. 2–2 shows the internal configuration of this input. With pin 3 at ground potential (low) or floating, the NVM 3060 reacts upon the IM bus addresses 128,129 and 131. With pin 3 continuously at V_{SUP} potential (high), the NVM 3060 reacts upon this IM bus addresses 132,133 and 135 (see Fig.2–6). In this way, parallel operation of two NVM 3060 is permitted, to obtain 8192 bits of non-volatile storage directly accessible via the IM bus. Pin 3 is internally tied to ground via a transistor equivalent to a 40 kΩ resistor.

Pin 4 – $\overline{\text{Reset}}$ Input
This input has a configuration as shown in Fig. 2–3. Via this input, the NVM 3060, together with the other circuits belonging to the system, receives the $\overline{\text{Reset}}$ signal which is derived from V_{SUP} via an external RC circuit. A low level is required during power-up and power-down procedures. Low level at pin 4 (max. 1.3 V) cancels a programming procedure and an IM bus operation in progress. The memory address register is not erased. During operation, pin 4 requires high level (min. 2.4 V).

Pins 5 to 7 – IM Bus Connections
These pins serve to connect the NVM 3060 EEPROM to the IM bus (see section 5.), via which it communicates with the CCU 2030/2050/2070/3000 Central Control Units or the SAA 12xx and TVPO 2066 Remote Control and Tuning ICs. Pins 5 (IM Bus Clock Input) and 6 (IM Bus Ident Input) are inputs as shown in Fig. 2–3 and pin 7 (IM Bus Data) is an input/output as shown in Fig. 2–4. The signal diagram for the IM bus is illustrated in Figs. 2–6 and Fig. 5–1. The required addresses which the NVM 3060 EEPROM receives from the microcomputer, are also shown in Fig. 2–6.

Pin 8 – Supply Voltage V_{SUP}
The supply voltage required is +5V (±5%), and the current consumption in active operation is approx. 30 mA. Inserting or removing the NVM 3060 from a live socket may alter programmed data!

2.4. Pin Circuits

The following figures show schematically the circuitry at the various pins. The integrated protection structures are not shown. The letter "E" means enhancement, the letter "D" depletion.

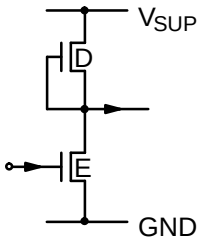

Fig. 2–3:
Pins 4, 5, and 6, Inputs

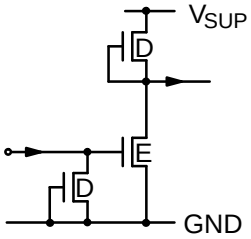

Fig. 2–2:
Pins 2 and 3, Input $\overline{S}$

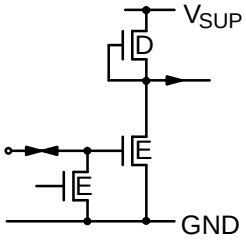

Fig. 2–4:
Pin 7, Input/Output

2.5. Electrical Characteristics

All Voltages are referred to ground.

2.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_S	Storage Temperature	–	–40	+125*	°C
V_{SUP}	Supply Voltage	8	–0.5	+6	V
V_I	Input Voltage	2 to 7	–0.3 V	V_{SUP}	–
I_O	Output Current	7	–	5	mA

* Stored data may be affected by T_S above +85 °C

2.5.2. Recommended Operating Conditions

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{SUP}	Supply Voltage	8	4.75	5.0	5.25	V
V_{IL}	Input Low Voltage	2, 3, 5 to 7	–	–	0.8	V
V_{IH}	Input High Voltage		2.4	–	–	V
V_{REIL}	$\overline{\text{Reset}}$ Input Low Voltage	4	–	–	1.3	V
V_{REIH}	$\overline{\text{Reset}}$ Input High Voltage		2.4	–	–	V
t_4	$V_{SUP} – V_{REI}$ Delay Time*	4, 8	0	–	–	ms
t_7	$V_{REI} – V_{SUP}$ Delay Time*		0	–	–	ms

*see Fig. 2–5

Recommended Operating Conditions, continued

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
V_{IMIL}	IM Bus Input Low Voltage	5 to 7	–	–	0.8	V
V_{IMIH}	IM Bus Input High Voltage		2.4	–	–	V
$f_{\Phi I}$	ΦI IM Bus Clock Frequency		0.05	–	170	kHz
t_{IM1}	ΦI Clock Input Delay Time after IM Bus Ident Input		0	–	–	–
t_{IM2}	ΦI Clock Input Low Pulse Time		3.0	–	–	µs
t_{IM3}	ΦI Clock Input High Pulse Time		3.0	–	–	µs
t_{IM4}	ΦI Clock Input Setup Time before Ident Input High		0	–	–	–
t_{IM5}	ΦI Clock Input Hold Time after Ident Input High		1.5	–	–	µs
t_{IM6}	ΦI Clock Input Setup Time before Ident End-Pulse Input		6.0	–	–	µs
t_{IM7}	IM Bus Input Delay Time after ΦI Clock Input		0	–	–	–
t_{IM8}	IM Bus Data Input Setup Time before ΦI Clock Input		0	–	–	–
t_{IM9}	IM Bus Data Input Hold Time after ΦI Clock Input		0	–	–	–
t_{IM10}	IM Bus Ident End-Pulse Low Time		3.0	–	–	µs

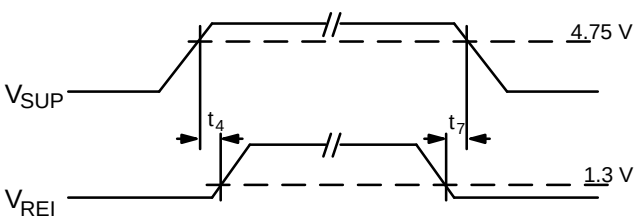

Fig. 2–5: Power on/off timing

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