NCP5500, NCV5500, NCP5501, NCV5501

500 mA Linear Regulator

These linear regulators provide up to 500 mA over a user−adjustable output range of 1.25 V to 5.0 V, or at a fixed output voltage of 1.5 V or 5.0 V*, with typical output voltage accuracy better than 3%. NCV versions are qualified for demanding automotive applications that require site and change control. NCP5500 and NCV5500 versions include an Enable/Shutdown function and are available in a DPAK−5L power package. In shutdown, current consumption is reduced to 30 μA. An internal PNP pass transistor permits low dropout voltage and operation at full load current at the minimum input voltage. NCP5501 and NCV5501 versions are available in DPAK−3L for applications that do not require logical on/off control.

This regulator family is ideal for applications that require a broad input voltage range, including both automotive and portable battery powered devices. Integral protection features include short circuit current and thermal shutdown.

Features

- Output Current up to 500 mA
- 2.9% Output Voltage Accuracy
- Low Dropout Voltage
- Enable Control Pin (NCP5500 / NCV5500)
- Reverse Battery Protection
- Reverse Bias Protection
- Short Circuit Protection
- Thermal Shutdown
- Operating Temperature Range of −40°C to +125°C (NCV5500 / NCV5501)
- NCV Prefix for Applications that Require Site and Change Control
- These are Pb−Free Devices

Typical Applications

- Automotive
- Industrial and Consumer
- Post SMPS Regulation
- Point of Use Regulation

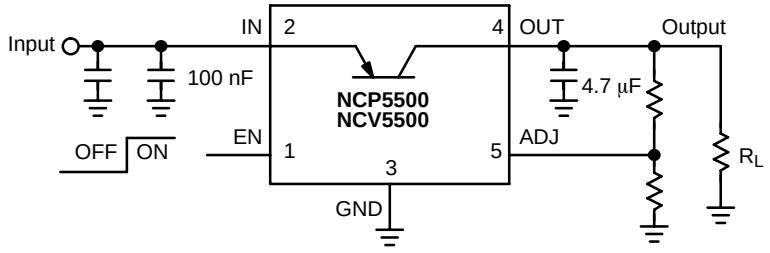


Figure 1. Typical Application Circuit

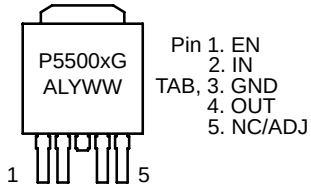
ON Semiconductor®

http://onsemi.com

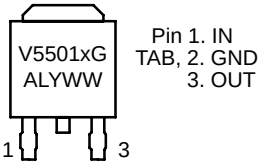
DPAK 5
CENTER LEAD CROP
CASE 175AA

DPAK
SINGLE GAUGE
CASE 369C

MARKING DIAGRAMS



DPAK 5



DPAK

P or V	= P (NCP), V (NCV)
5500/1	= Device Code
x	= Output Voltage
	L = 1.5 V
	U = 5.0 V
	W = Adjustable
G	= Pb−Free Package
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week

*Contact ON Semiconductor for other fixed voltages.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

PIN FUNCTION DESCRIPTIONS

Pin No.	Symbol	Description
NCP5500 / NCV5500 − DPAK 5 Lead Center Lead Crop		
1	EN	Output Enable; high level turns on the output.
2	IN	Input; battery/unregulated supply input voltage.
3, TAB	GND	Ground; Pin 3 connected internally to the Tab heat sink.
4	OUT	Output; bypass to ground.
5	NC / ADJ	No connection (Fixed output versions only). Voltage−adjust input. Use an external voltage divider to set the output voltage over a range of 1.25 V to 5.0 V. Adjustable version only.
NCP5501 / NCV5501 − DPAK 3 Lead		
1	IN	Input; battery/unregulated supply input voltage.
2, TAB	GND	Ground; Pin 3 connected internally to the Tab heat sink.
3	OUT	Output; bypass to ground.

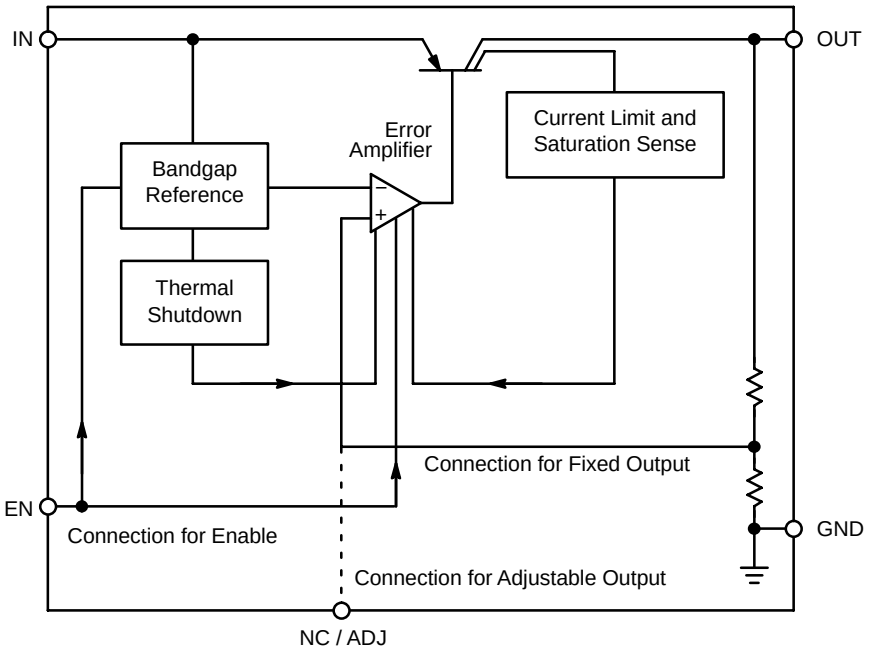


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = −40°C to +85°C (NCP5500, NCP5501), T_A = −40°C to +125°C (NCV5500, NCV5501), unless otherwise noted.

Pin Symbol, Parameter	Symbol	Min	Max	Units
IN, V_{IN}, DC Input Voltage	V_{IN}	−7.0	+18	V
OUT, EN, V_{OUT}, V_{EN}, DC Voltage	V	−0.3	+16 V_{IN} + 0.3 (Note 4)	V
Junction Temperature	T_J		+150	°C
Package Dissipation DPAK 5 Power Dissipation at T_A = 25°C Thermal Resistance, Junction−to−Air Thermal Resistance, Junction−to−Case DPAK Power Dissipation at T_A = 25°C Thermal Resistance, Junction−to−Air Thermal Resistance, Junction−to−Case	 P_D $R_{\theta JA}$ $R_{\theta JC}$ P_D $R_{\theta JA}$ $R_{\theta JC}$		 Internally Limited 75 8.0 Internally Limited 101 6.6	°C/W
Storage Temperature	T_{Stg}	−55	+150	°C
Moisture Sensitivity Level	MSL	1		−
ESD Capability, Human Body Model (Note 1)	ESD_{HBM}	4000	−	V
ESD Capability, Machine Model (Note 1)	ESD_{MM}	200	−	V
ESD Capability, Charged Device Model (Note 1)	ESD_{CDM}	1000	−	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	 T_{sld}		 265 Peak	°C

OPERATING RANGES

IN, V_{IN}, Operating DC Input Voltage	V_{IN}	V_{OUT} + V_{DO}, 2.5 V (Note 5)	16	V
OUT, V_{OUT} Adjust Range (adjustable version only)	V_{OUT}	1.25	5.0	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   ESD Charged Device Model tested per EIA/JES D22/C101, Field Induced Charge Model
2. Latch−up Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78.
3. Pb−Free, 60 sec –150 sec above 217°C, 40 sec max at peak temperature
4. Maximum = +16 V or (V_{IN} +0.3 V), whichever is lower.
5. Minimum V_{IN} = 2.5 V or (V_{OUT} + V_{DO}), whichever is higher.

ELECTRICAL CHARACTERISTICS V_{IN} = 2.5 V or (V_{OUT} + 1.0 V), whichever is higher, C_O = 4.7 μF, −40°C < T_A < 85°C (<125°C for NCV versions), T_J < 150°C unless otherwise noted.

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
OUTPUT						
Output Voltage (Note 6) Fixed Output Versions Adjustable Voltage Versions	V_{OUT}	 T_A = 25°C, I_O = 50 mA T_A = 25°C, I_O = 50 mA		 ±2.9% ±2.9%		V
Output Voltage (Notes 6 and 7)	V_{OUT}	1.0 mA < I_O < 500 mA	−4.9%		+4.9%	V
Line Regulation (Note 7)	REG_{LINE}	I_O = 50 mA 2.5 V or (V_{OUT} + 1.0 V) < V_{IN} < 16 V		0.1	1.0	%
Load Regulation (Note 7)	REG_{LOAD}	1.0 mA < I_O < 500 mA		0.35	1.0	%
Dropout Voltage Fixed Output Versions	V_{DO} (Note 8)	I_O = 1.0 mA, ΔV_{OUT} = −2% I_O = 500 mA, ΔV_{OUT} = −2%		20 300	90 700	mV
Dropout Voltage Adjustable Output Versions	V_{DO} (Note 9)	I_O = 1.0 mA, ΔV_{OUT} = −2% I_O = 500 mA, ΔV_{OUT} = −2%		20 300	90 700	mV
Ground Current	I_{GND}	I_O = 100 μA I_O = 500 mA (Note 7)		300 10	500 20	μA mA
Quiescent Current in Shutdown (NCP5500, NCV5500)	Iq	Adjustable and 1.5 V versions All other versions		30 40	50 50	μA
Current Limit	$I_{OUT(LIM)}$	V_{OUT} = 0 V (Note 7)	500	700	900	mA
Ripple Rejection Ratio	RR	f = 120 Hz		75		dB
Output Noise Voltage (Note 10)	V_n	f = 10 Hz to 100 kHz, V_{IN} = 2.5 V V_{OUT} = 1.25 V, I_O = 1.0 mA f = 10 Hz to 100 kHz, V_{IN} = 2.5 V V_{OUT} = 1.25 V, I_O = 100 mA		 20 34		μVrms
Minimum Output Capacitance / ESR for Stability	C_{OUT} / ESR	5.0 mA < I_O < 500 mA T_A = 25°C	4.7 μF / 3 Ω			
ENABLE (NCP5500, NCV5500 Only)						
Enable Voltage	V_{ENoff} V_{ENon}	OFF (shutdown) State ON (enabled) State	 2.0		0.4	V
Enable Pin Bias Current	I_{EN}	V_{EN} = V_{IN}, V_{IN} = 2.5 V, I_O = 1.0 mA		−	1.0	μA
ADJUST						
Adjust Pin Current (Note 11)	I_{ADJ}	V_{EN} = V_{IN}, V_{ADJ} = 1.25 V, V_{OUT} = 1.25 V		−	60	nA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 11)	TSD	I_O = 100 μA	150	−	210	°C

6. Deviation from nominal. For adjustable versions, Pin ADJ connected to OUT.
7. Use pulse loading to limit power dissipation (duration < 100 mS and duty cycle < 1%).
8. V_{DO} = V_{IN} − V_{OUT}. For <2.5 V versions, V_{DO} will be constrained by the minimum input voltage of 2.5 V.
9. V_{DO} = V_{IN} − V_{OUT}. For output voltage set to <2.5 V, V_{DO} will be constrained by the minimum input voltage.
10. V_n for other fixed voltage versions, as well as adjustable versions set to other output voltages, can be calculated from the following formula: V_n = $V_{n(x)}$ * (V_{OUT} − 1.25) / 1.25, where $V_{n(x)}$ is the typical value from the table above.
11. Not tested in production. Limits are guaranteed by design.

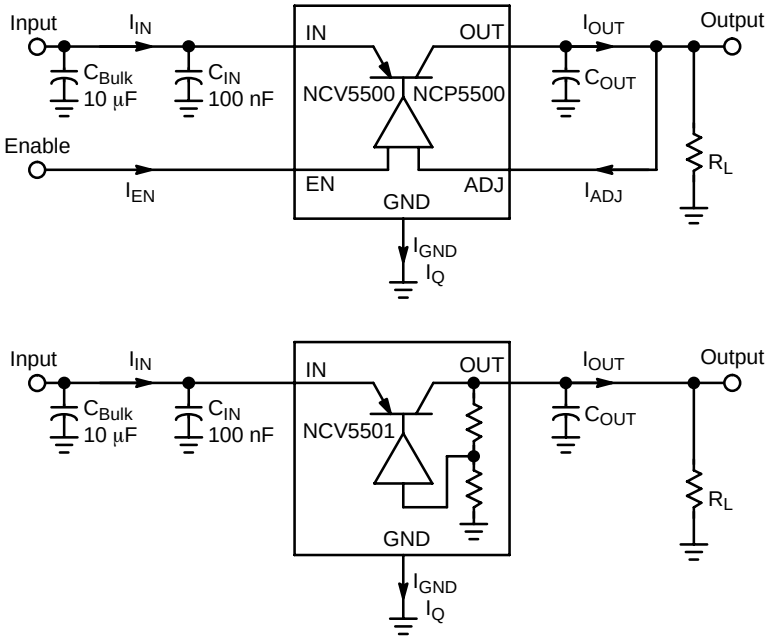


Figure 3. Measuring Circuits

Circuit Description

The NCP5500/NCP5501/NCV5500/NCV5501 are integrated linear regulators with a DC load current capability of 500 mA. The output voltage is regulated by a PNP pass transistor controlled by an error amplifier and band gap reference. The choice of a PNP pass element provides the lowest possible dropout voltage, particularly at reduced load currents. Pass transistor base drive current is controlled to prevent oversaturation. The regulator is internally protected by both current limit and thermal shutdown. Thermal shutdown occurs when the junction temperature exceeds 150°C. The NCV5500 includes an enable/shutdown pin to turn off the regulator to a low current drain standby state.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_{OUT}) and drives the base of a PNP series pass transistor via a buffer. The reference is a bandgap design for enhanced temperature stability. Saturation control of the PNP pass transistor is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

Regulator Stability Considerations

The input capacitors (C_{BULK} and C_{IN}) are necessary to stabilize the input impedance to reduce transient line influences. The output capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with its almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution. However, if the circuit operates at low temperatures (−25°C to −40°C), both capacitor value and ESR will vary considerably. The capacitor manufacturer's data sheet usually provides temperature performance data. Stability is guaranteed for C_{OUT} = 4.7 μF and ESR < 3 Ω.

Enable Input (NCP5500, NCV5500)

The enable pin is used to turn the regulator on or off. By holding the pin at a voltage less than 0.5 V, the output of the regulator will be turned off to a minimal current drain state. When the voltage at the Enable pin is greater than 2.0 V, the output of the regulator will be enabled and rise to the regulated output voltage. The Enable pin may be connected directly to the input pin to provide a constant enable to the regulator.

Active Load Protection in Shutdown (NCP5500, NCV5500)

When a linear regulator is disabled (shutdown), the output (load) voltage should be zero. However, stray PC board leakage paths, output capacitor dielectric absorption, and inductively coupled power sources can cause an undesirable regulator output voltage if load current is low or zero. The NCV5500 features a load protection network that is active only during Shutdown mode. This network switches in a shunt current path (~500 μA) from V_{OUT} to Ground. This feature also provides a controlled ("soft") discharge path for the output capacitor after a transition from Enable to Shutdown.

DEFINITION OF TERMS

Dropout Voltage: The input−to−output voltage differential at which the circuit ceases to regulate against further reduction input voltage. Measured when the output voltage has dropped 2% relative to the value measured at 6.0 V input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature. Pulse loading techniques are employed such that the average chip temperature is not significantly affected.

Quiescent Current: The part of the positive input current that does not contribute to the positive load current. The regulator ground pin current with no load.

Ripple Rejection: The ratio of the peak−to−peak input ripple voltage to the peak−to−peak output ripple voltage.

Current Limit: Peak current that can be delivered to the output.

Calculating Power Dissipation

The maximum power dissipation for a single output regulator (Figure 3) is:

$$P_{D(max)} = \left[V_{IN(max)} - V_{OUT(min)}\right]I_{OUT(max)} + V_{IN(max)}I_q \quad \text{(eq. 1)}$$

Where
$V_{IN(max)}$ is the maximum input voltage,
$V_{OUT(min)}$ is the minimum output voltage,
$I_{OUT(max)}$ is the maximum output current for the application,
I_{GND} is the ground current at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{(150^{\circ}C - T_A)}{P_D} \quad \text{(eq. 2)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$ less than the calculated value in Equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required.

Heat sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 3)}$$

where
$R_{\theta JC}$ is the junction−to−case thermal resistance,
$R_{\theta CS}$ is the case−to−heatsink thermal resistance,
$R_{\theta SA}$ is the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heat sink and the interface between them. These values appear in data sheets of heat sink manufacturers.

Thermal, mounting, and heat sink considerations are further discussed in ON Semiconductor Application Note AN1040/D.

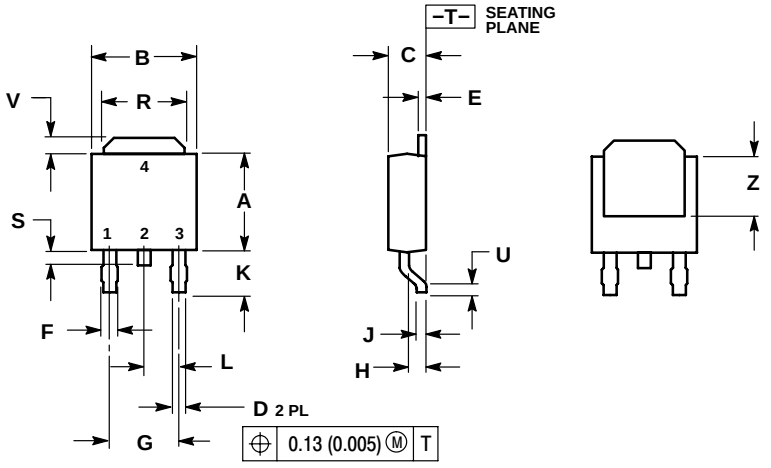
ORDERING INFORMATION

Device	Nominal Output Voltage	Package Marking	Package	Shipping†
NCP5500DT15RKG	1.5	P5500LG	DPAK−5 (Pb−Free)	2500 / Tape & Reel
NCV5500DT15RKG		V5500LG	DPAK−5 (Pb−Free)	2500 / Tape & Reel
NCP5501DT15RKG		P5501LG	DPAK (Pb−Free)	2500 / Tape & Reel
NCP5501DT15G		P5501LG	DPAK (Pb−Free)	75 Units / Rail
NCV5501DT15RKG		V5501LG	DPAK (Pb−Free)	2500 / Tape & Reel
NCV5501DT15G		V5501LG	DPAK (Pb−Free)	75 Units / Rail
NCP5500DT50RKG	5.0	P5500UG	DPAK−5 (Pb−Free)	2500 / Tape & Reel
NCP5501DT50RKG		P5501UG	DPAK (Pb−Free)	2500 / Tape & Reel
NCP5501DT50G		P5501UG	DPAK (Pb−Free)	75 Units / Rail
NCP5500DTADJRKG	Adjustable	P5500WG	DPAK−5 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

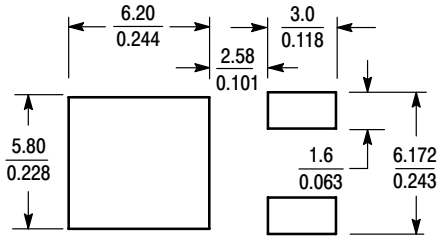
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

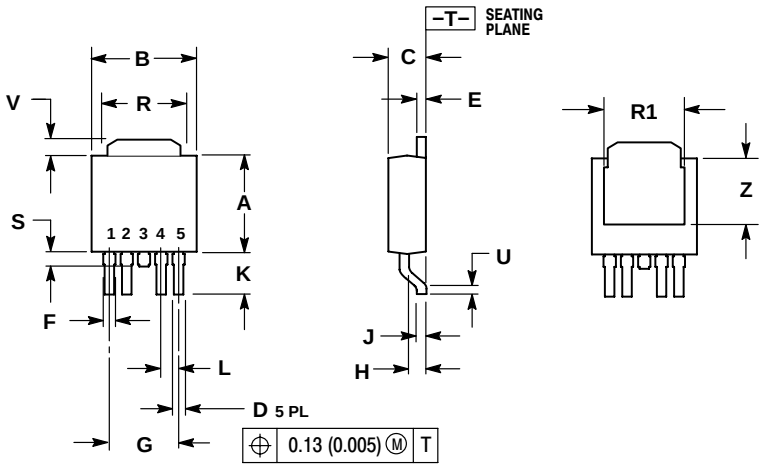
RECOMMENDED FOOTPRINT



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

PACKAGE DIMENSIONS

DPAK 5, CENTER LEAD CROP
CASE 175AA−01
ISSUE A



NOTES:
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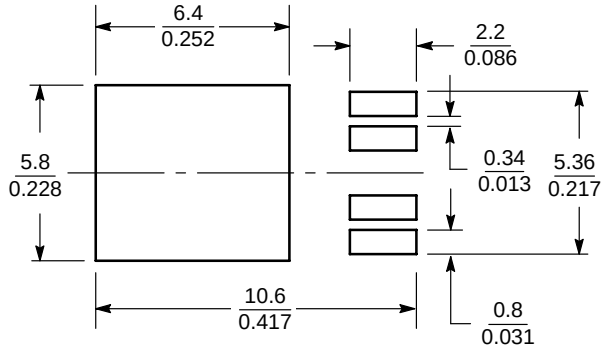
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

SOLDERING FOOTPRINT*



SCALE 4:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
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Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

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