

Silicon Power Transistors

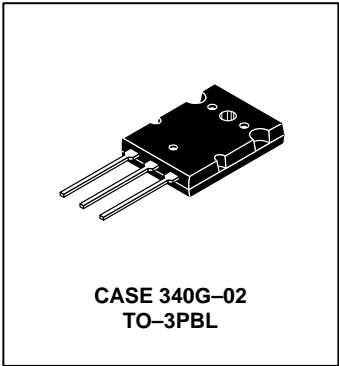
The MJL21193 and MJL21194 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

- Total Harmonic Distortion Characterized
- High DC Current Gain –
 $h_{FE} = 25 \text{ Min @ } I_C$
 $= 8 \text{ Adc}$
- Excellent Gain Linearity
- High SOA: 2.25 A, 80 V, 1 Second

PNP
MJL21193*
NPN
MJL21194*

*ON Semiconductor Preferred Device

16 AMPERE
COMPLEMENTARY
SILICON POWER
TRANSISTORS
250 VOLTS
200 WATTS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	250	Vdc
Collector–Base Voltage	V_{CBO}	400	Vdc
Emitter–Base Voltage	V_{EBO}	5	Vdc
Collector–Emitter Voltage – 1.5 V	V_{CEX}	400	Vdc
Collector Current — Continuous Peak (1)	I_C	16 30	Adc
Base Current – Continuous	I_B	5	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above 25°C	P_D	200 1.43	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J , T_{stg}	–65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
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OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ($I_C = 100 \text{ mAdc}$, $I_B = 0$)	$V_{CEO(sus)}$	250	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 200 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	—	100	μAdc

(1) Pulse Test: Pulse Width = 5.0 μs , Duty Cycle $\leq 10\%$.

(continued)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
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OFF CHARACTERISTICS

Emitter Cutoff Current ($V_{CE} = 5\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	—	100	μAdc
Collector Cutoff Current ($V_{CE} = 250\text{ Vdc}$, $V_{BE(\text{off})} = 1.5\text{ Vdc}$)	I_{CEX}	—	—	100	μAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased ($V_{CE} = 50\text{ Vdc}$, $t = 1\text{ s}$ (non-repetitive)) ($V_{CE} = 80\text{ Vdc}$, $t = 1\text{ s}$ (non-repetitive))	$I_{S/b}$	4.0 2.25	— —	— —	A _{dc}
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ON CHARACTERISTICS

DC Current Gain ($I_C = 8\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 16\text{ Adc}$, $I_B = 5\text{ Adc}$)	h_{FE}	25 8	— —	75 —	
Base-Emitter On Voltage ($I_C = 8\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	$V_{BE(\text{on})}$	—	—	2.2	V _{dc}
Collector-Emitter Saturation Voltage ($I_C = 8\text{ Adc}$, $I_B = 0.8\text{ Adc}$) ($I_C = 16\text{ Adc}$, $I_B = 3.2\text{ Adc}$)	$V_{CE(\text{sat})}$	— —	— —	1.4 4	V _{dc}

DYNAMIC CHARACTERISTICS

Total Harmonic Distortion at the Output $V_{RMS} = 28.3\text{ V}$, $f = 1\text{ kHz}$, $P_{LOAD} = 100\text{ W}_{RMS}$ (Matched pair $h_{FE} = 50 @ 5\text{ A}/5\text{ V}$)	T_{HD}	—	0.8 0.08	—	%
Current Gain Bandwidth Product ($I_C = 1\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$, $f_{\text{test}} = 1\text{ MHz}$)	f_T	4	—	—	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f_{\text{test}} = 1\text{ MHz}$)	C_{ob}	—	—	500	pF

(1) Pulse Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$

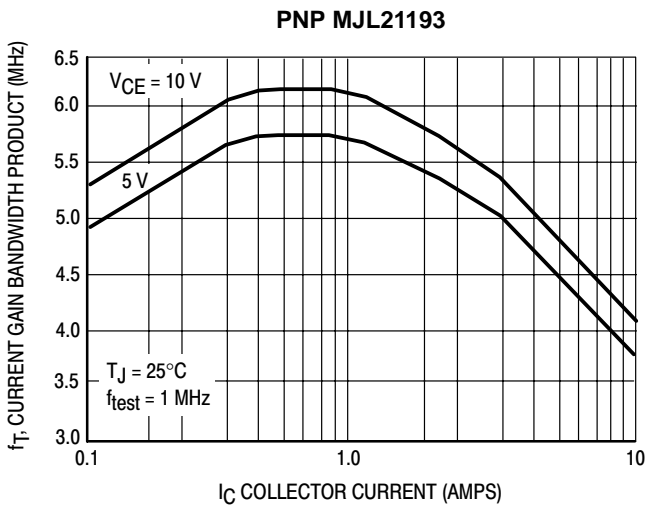


Figure 1. Typical Current Gain Bandwidth Product

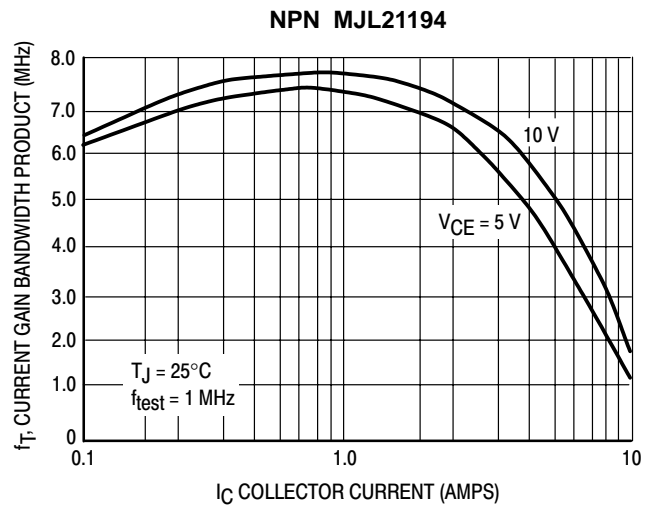


Figure 2. Typical Current Gain Bandwidth Product

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TYPICAL CHARACTERISTICS

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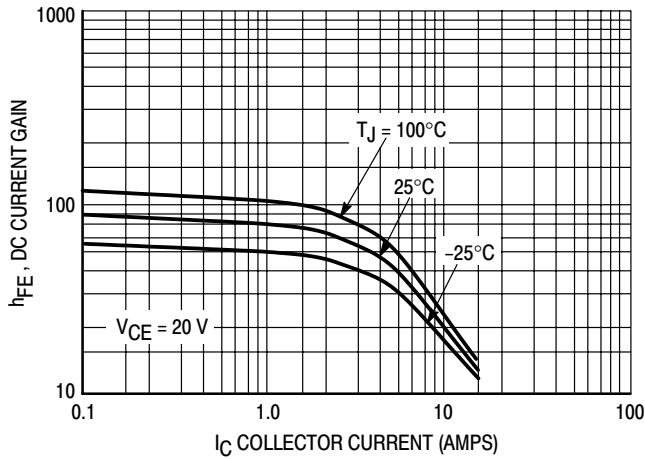


Figure 3. DC Current Gain, $V_{CE} = 20\text{ V}$

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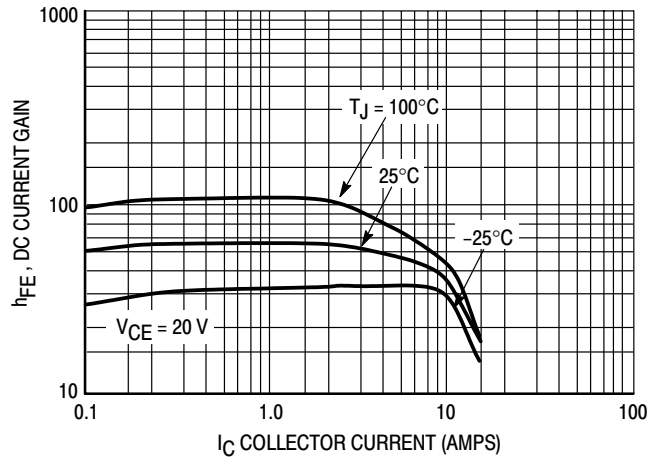


Figure 4. DC Current Gain, $V_{CE} = 20\text{ V}$

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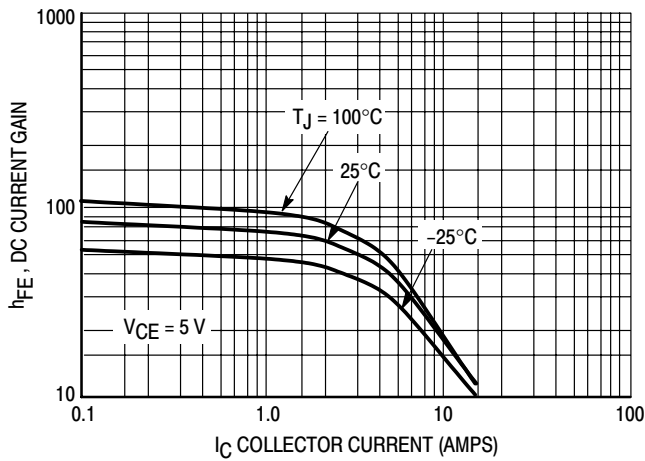


Figure 5. DC Current Gain, $V_{CE} = 5\text{ V}$

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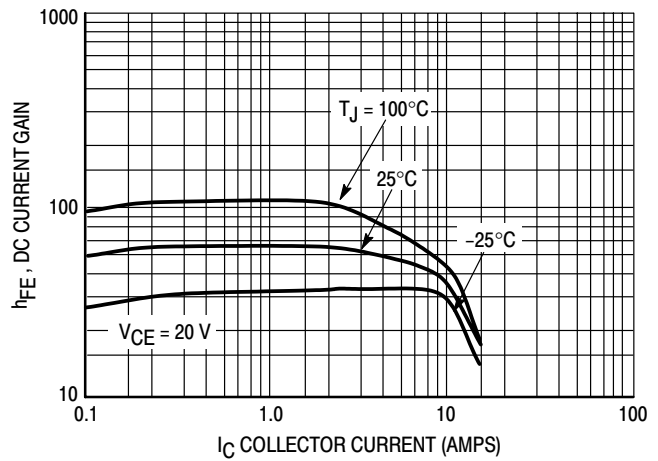
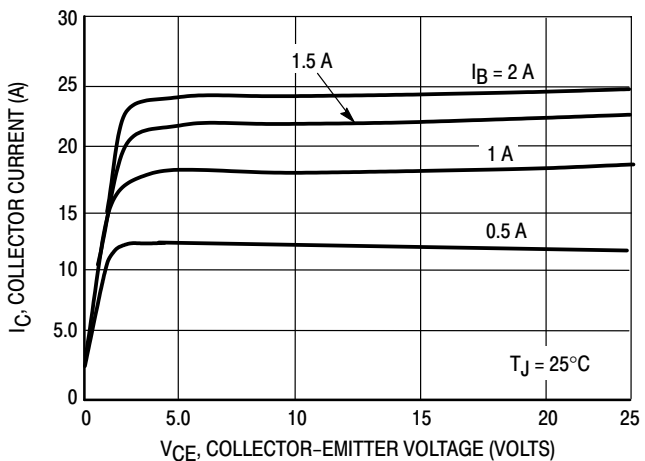
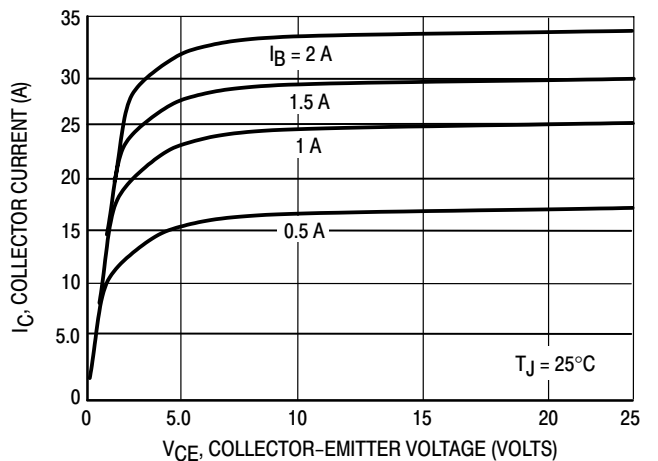


Figure 6. DC Current Gain, $V_{CE} = 5\text{ V}$

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TYPICAL CHARACTERISTICS

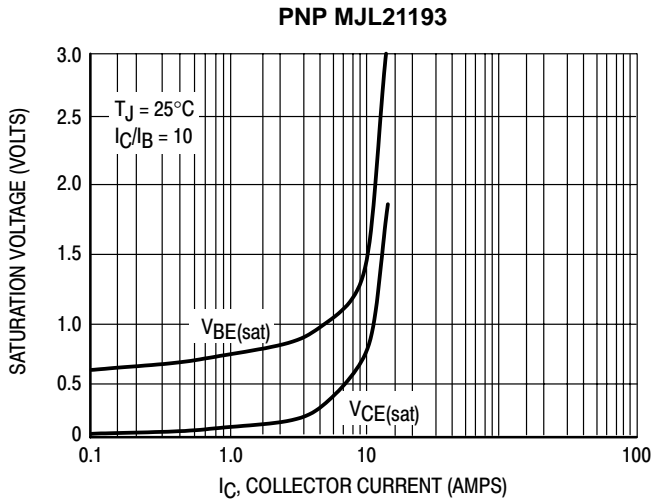


Figure 9. Typical Saturation Voltages

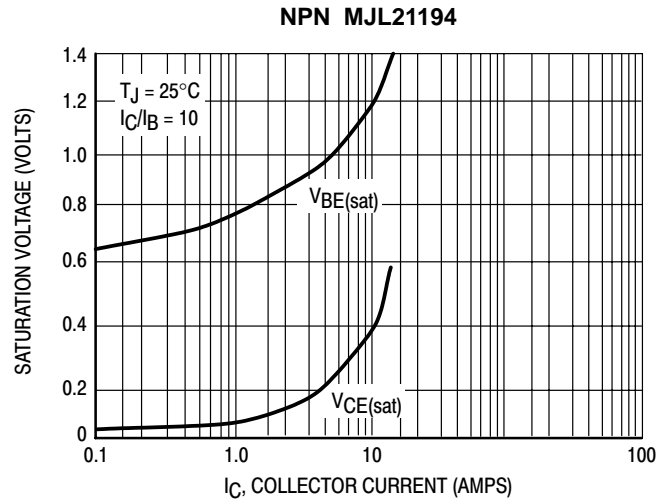


Figure 10. Typical Saturation Voltages

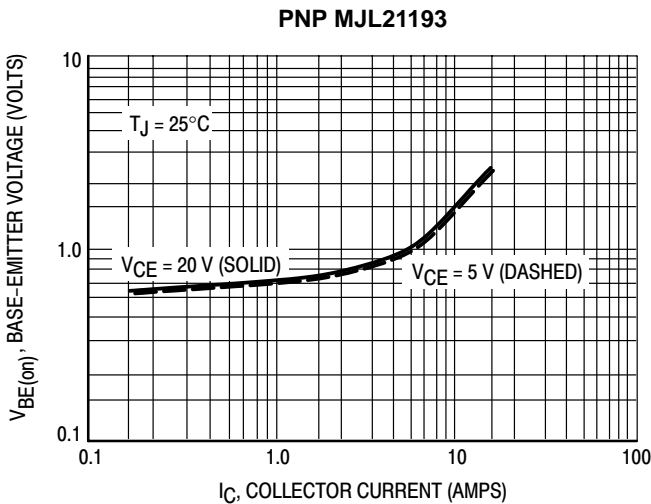


Figure 11. Typical Base-Emitter Voltage

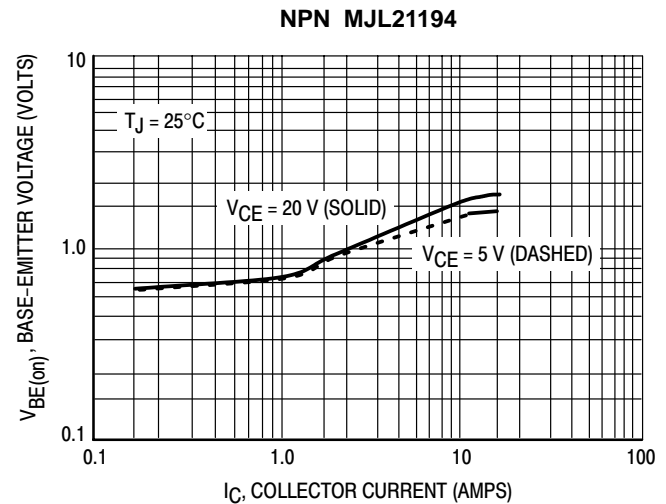


Figure 12. Typical Base-Emitter Voltage

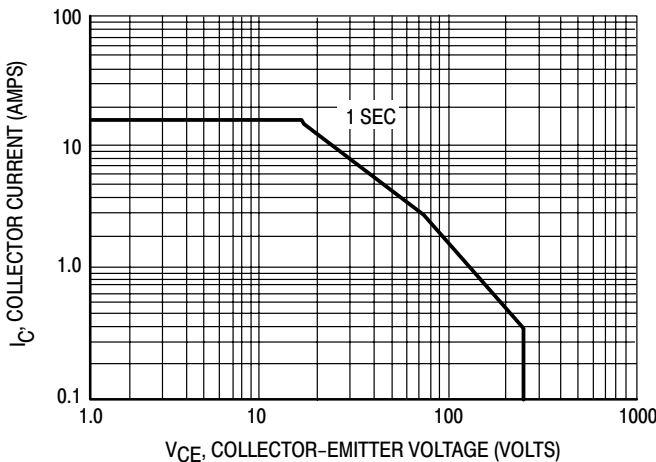


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

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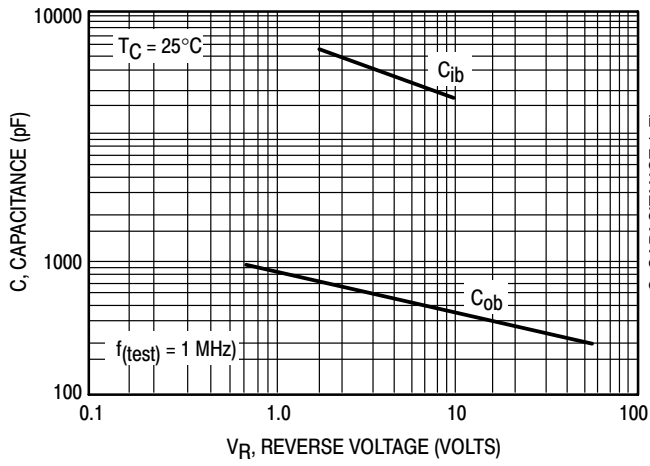


Figure 14. MJL21193 Typical Capacitance

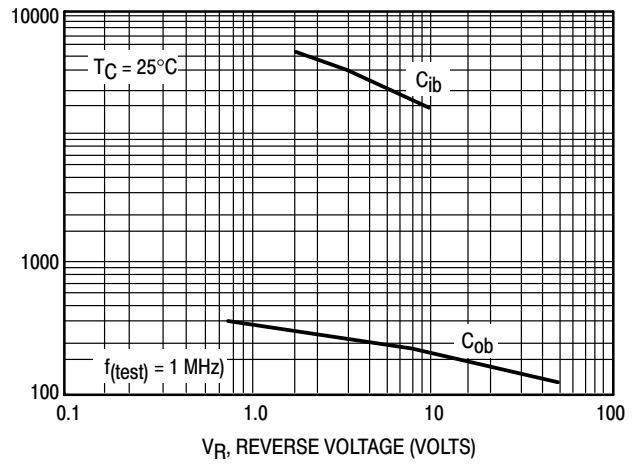


Figure 15. MJL21194 Typical Capacitance

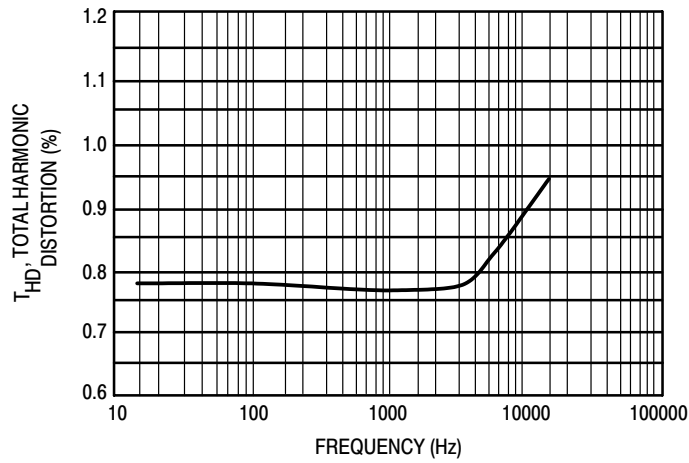


Figure 16. Typical Total Harmonic Distortion

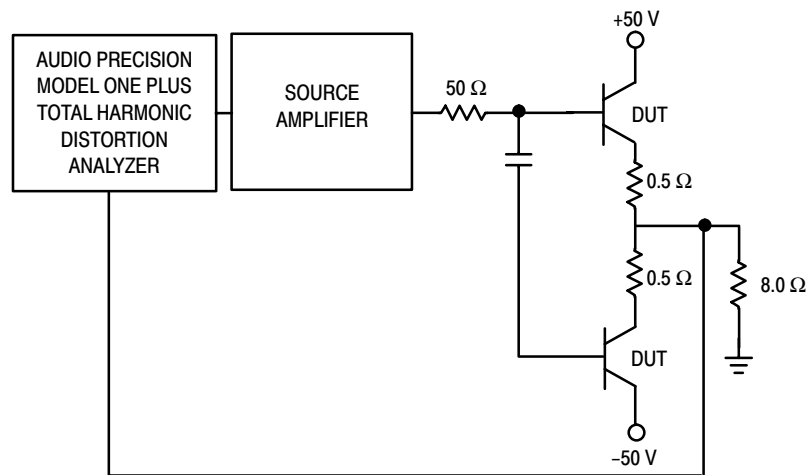


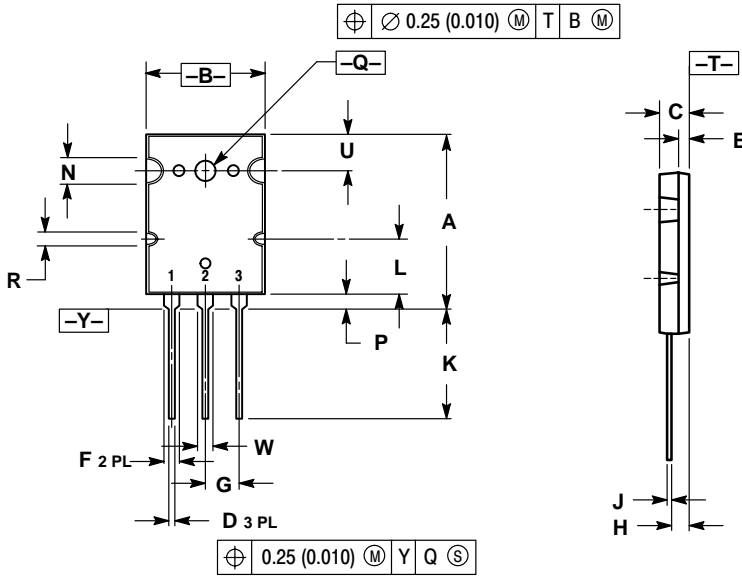
Figure 17. Total Harmonic Distortion Test Circuit

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PACKAGE DIMENSIONS

TO-3PBL (TO-264)
CASE 340G-02
ISSUE H

SCALE 1:2



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	28.0	29.0	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
F	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
J	0.43	0.78	0.017	0.031
K	17.6	18.8	0.693	0.740
L	11.0	11.4	0.433	0.449
N	3.95	4.75	0.156	0.187
P	2.2	2.6	0.087	0.102
Q	3.1	3.5	0.122	0.137
R	2.15	2.35	0.085	0.093
U	6.1	6.5	0.240	0.256
W	2.8	3.2	0.110	0.125

Notes

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