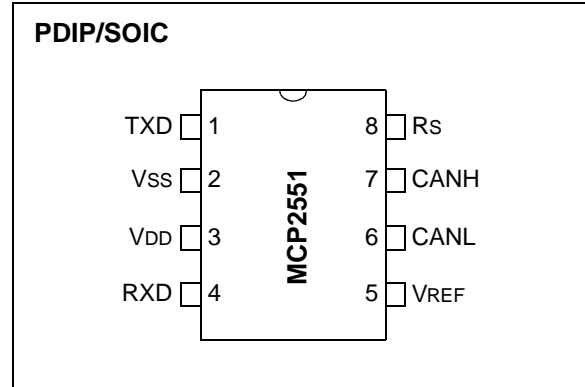


High-Speed CAN Transceiver

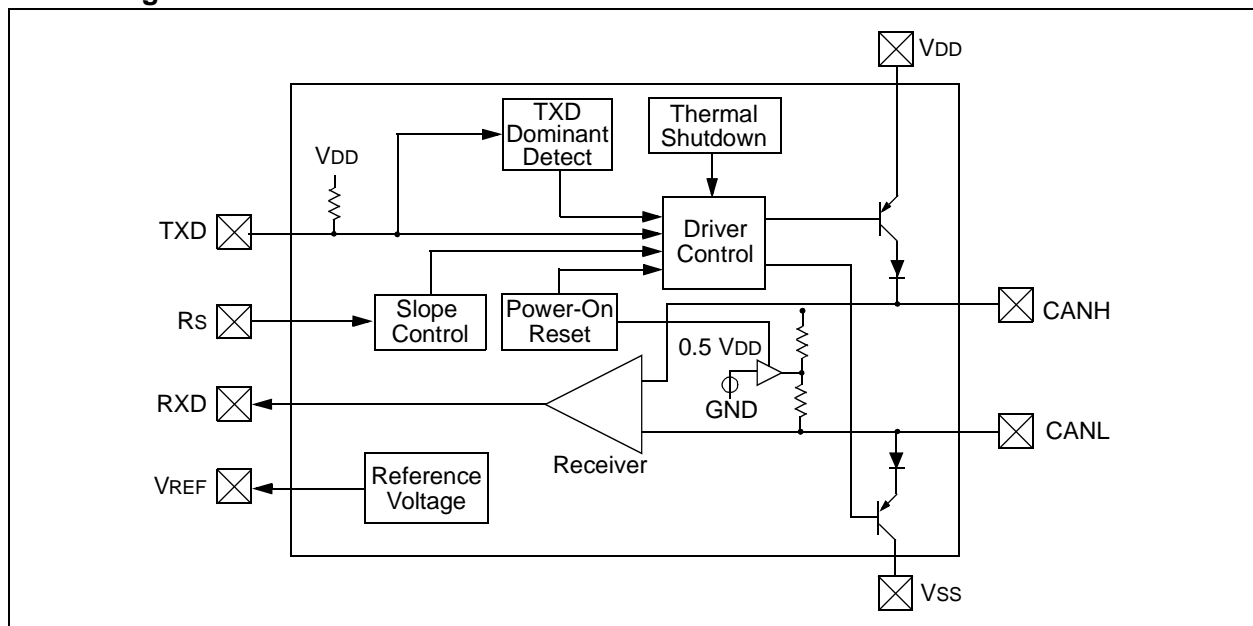
Features

- Supports 1 Mb/s operation
- Implements ISO-11898 standard physical layer requirements
- Suitable for 12V and 24V systems
- Externally-controlled slope for reduced RFI emissions
- Detection of ground fault (permanent dominant) on TXD input
- Power-on reset and voltage brown-out protection
- An unpowered node or brown-out event will not disturb the CAN bus
- Low current standby operation
- Protection against damage due to short-circuit conditions (positive or negative battery voltage)
- Protection against high-voltage transients
- Automatic thermal shutdown protection
- Up to 112 nodes can be connected
- High noise immunity due to differential bus implementation
- Temperature ranges:
 - Industrial (I): -40°C to +85°C
 - Extended (E): -40°C to +125°C

Package Types



Block Diagram



MCP2551

NOTES:

1.0 DEVICE OVERVIEW

The MCP2551 is a high-speed CAN, fault-tolerant device that serves as the interface between a CAN protocol controller and the physical bus. The MCP2551 provides differential transmit and receive capability for the CAN protocol controller and is fully compatible with the ISO-11898 standard, including 24V requirements. It will operate at speeds of up to 1 Mb/s.

Typically, each node in a CAN system must have a device to convert the digital signals generated by a CAN controller to signals suitable for transmission over the bus cabling (differential output). It also provides a buffer between the CAN controller and the high-voltage spikes that can be generated on the CAN bus by outside sources (EMI, ESD, electrical transients, etc.).

1.1 Transmitter Function

The CAN bus has two states: Dominant and Recessive. A dominant state occurs when the differential voltage between CANH and CANL is greater than a defined voltage (e.g., 1.2V). A recessive state occurs when the differential voltage is less than a defined voltage (typically 0V). The dominant and recessive states correspond to the low and high state of the TXD input pin, respectively. However, a dominant state initiated by another CAN node will override a recessive state on the CAN bus.

1.1.1 MAXIMUM NUMBER OF NODES

The MCP2551 CAN outputs will drive a minimum load of 45Ω, allowing a maximum of 112 nodes to be connected (given a minimum differential input resistance of 20 kΩ and a nominal termination resistor value of 120Ω).

1.2 Receiver Function

The RXD output pin reflects the differential bus voltage between CANH and CANL. The low and high states of the RXD output pin correspond to the dominant and recessive states of the CAN bus, respectively.

1.3 Internal Protection

CANH and CANL are protected against battery short-circuits and electrical transients that can occur on the CAN bus. This feature prevents destruction of the transmitter output stage during such a fault condition.

The device is further protected from excessive current loading by thermal shutdown circuitry that disables the output drivers when the junction temperature exceeds a nominal limit of 165°C. All other parts of the chip remain operational and the chip temperature is lowered due to the decreased power dissipation in the transmitter outputs. This protection is essential to protect against bus line short-circuit-induced damage.

1.4 Operating Modes

The Rs pin allows three modes of operation to be selected:

- High-Speed
- Slope-Control
- Standby

These modes are summarized in Table 1-1.

When in High-speed or Slope-control mode, the drivers for the CANH and CANL signals are internally regulated to provide controlled symmetry in order to minimize EMI emissions.

Additionally, the slope of the signal transitions on CANH and CANL can be controlled with a resistor connected from pin 8 (Rs) to ground, with the slope proportional to the current output at Rs, further reducing EMI emissions.

1.4.1 HIGH-SPEED

High-speed mode is selected by connecting the Rs pin to Vss. In this mode, the transmitter output drivers have fast output rise and fall times to support high-speed CAN bus rates.

1.4.2 SLOPE-CONTROL

Slope-control mode further reduces EMI by limiting the rise and fall times of CANH and CANL. The slope, or slew rate (SR), is controlled by connecting an external resistor (R_{EXT}) between Rs and VOL (usually ground). The slope is proportional to the current output at the Rs pin. Since the current is primarily determined by the slope-control resistance value R_{EXT}, a certain slew rate is achieved by applying a respective resistance. Figure 1-1 illustrates typical slew rate values as a function of the slope-control resistance value.

1.4.3 STANDBY MODE

The device may be placed in standby or "SLEEP" mode by applying a high-level to Rs. In SLEEP mode, the transmitter is switched off and the receiver operates at a lower current. The receive pin on the controller side (RXD) is still functional but will operate at a slower rate. The attached microcontroller can monitor RXD for CAN bus activity and place the transceiver into normal operation via the Rs pin (at higher bus rates, the first CAN message may be lost).

MCP2551

TABLE 1-1: MODES OF OPERATION

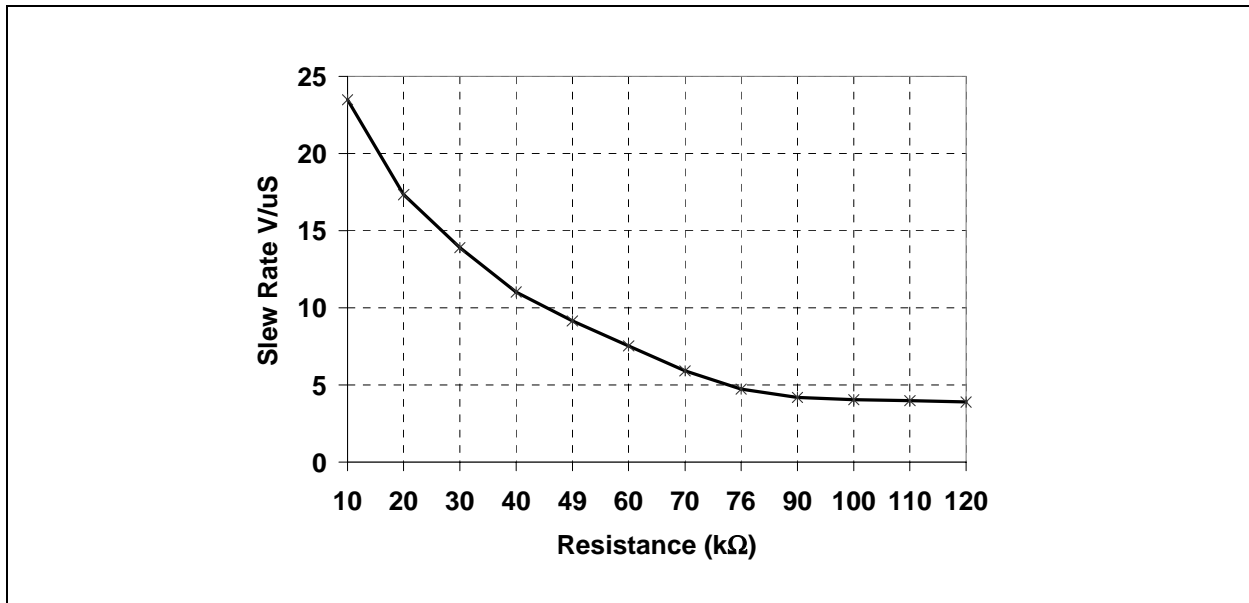
Mode	Current at R _S Pin	Resulting Voltage at R _S Pin
Standby	-I _{RS} < 10 μA	V _{RS} > 0.75 V _{DD}
Slope-control	10 μA < -I _{RS} < 200 μA	0.4 V _{DD} < V _{RS} < 0.6 V _{DD}
High-speed	-I _{RS} < 610 μA	0 < V _{RS} < 0.3V _{DD}

TABLE 1-2: TRANSCEIVER TRUTH TABLE

V _{DD}	V _{RS}	TXD	CANH	CANL	Bus State ⁽¹⁾	RxD ⁽¹⁾
4.5V ≤ V _{DD} ≤ 5.5V	V _{RS} < 0.75 V _{DD}	0	HIGH	LOW	Dominant	0
		1 or floating	Not Driven	Not Driven	Recessive	1
	V _{RS} > 0.75 V _{DD}	X	Not Driven	Not Driven	Recessive	1
V _{POR} < V _{DD} < 4.5V (See Note 3)	V _{RS} < 0.75 V _{DD}	0	HIGH	LOW	Dominant	0
		1 or floating	Not Driven	Not Driven	Recessive	1
	V _{RS} > 0.75 V _{DD}	X	Not Driven	Not Driven	Recessive	1
0 < V _{DD} < V _{POR}	X	X	Not Driven/ No Load	Not Driven/ No Load	High Impedance	X

- Note 1:** If another bus node is transmitting a dominant bit on the CAN bus, then RXD is a logic '0'.
2: X = "don't care".
3: Device drivers will function, although outputs are not ensured to meet the ISO-11898 specification.

FIGURE 1-1: SLEW RATE VS. SLOPE-CONTROL RESISTANCE VALUE



1.5 TXD Permanent Dominant Detection

If the MCP2551 detects an extended low state on the TXD input, it will disable the CANH and CANL output drivers in order to prevent the corruption of data on the CAN bus. The drivers are disabled if TXD is low for more than 1.25 ms (minimum). This implies a maximum bit time of 62.5 μ s (16 kb/s bus rate), allowing up to 20 consecutive transmitted dominant bits during a multiple bit error and error frame scenario. The drivers remain disabled as long as TXD remains low. A rising edge on TXD will reset the timer logic and enable the CANH and CANL output drivers.

1.6 Power-on Reset

When the device is powered on, CANH and CANL remain in a high-impedance state until VDD reaches the voltage-level VPORH. In addition, CANH and CANL will remain in a high-impedance state if TXD is low when VDD reaches VPORH. CANH and CANL will become active only after TXD is asserted high. Once powered on, CANH and CANL will enter a high-impedance state if the voltage level at VDD falls below VPORL, providing voltage brown-out protection during normal operation.

1.7 Pin Descriptions

The 8-pin pinout is listed in Table 1-3.

TABLE 1-3: MCP2551 PINOUT

Pin Number	Pin Name	Pin Function
1	TXD	Transmit Data Input
2	VSS	Ground
3	VDD	Supply Voltage
4	RXD	Receive Data Output
5	VREF	Reference Output Voltage
6	CANL	CAN Low-Level Voltage I/O
7	CANH	CAN High-Level Voltage I/O
8	Rs	Slope-Control Input

1.7.1 TRANSMITTER DATA INPUT (TXD)

TXD is a TTL-compatible input pin. The data on this pin is driven out on the CANH and CANL differential output pins. It is usually connected to the transmitter data output of the CAN controller device. When TXD is low, CANH and CANL are in the dominant state. When TXD is high, CANH and CANL are in the recessive state, provided that another CAN node is not driving the CAN bus with a dominant state. TXD has an internal pull-up resistor (nominal 25 k Ω to VDD).

1.7.2 GROUND SUPPLY (VSS)

Ground supply pin.

1.7.3 SUPPLY VOLTAGE (VDD)

Positive supply voltage pin.

1.7.4 RECEIVER DATA OUTPUT (RXD)

RXD is a CMOS-compatible output that drives high or low depending on the differential signals on the CANH and CANL pins and is usually connected to the receiver data input of the CAN controller device. RXD is high when the CAN bus is recessive and low in the dominant state.

1.7.5 REFERENCE VOLTAGE (VREF)

Reference Voltage Output (Defined as VDD/2).

1.7.6 CAN LOW (CANL)

The CANL output drives the low side of the CAN differential bus. This pin is also tied internally to the receive input comparator.

1.7.7 CAN HIGH (CANH)

The CANH output drives the high-side of the CAN differential bus. This pin is also tied internally to the receive input comparator.

1.7.8 SLOPE RESISTOR INPUT (Rs)

The Rs pin is used to select High-speed, Slope-control or Standby modes via an external biasing resistor.

MCP2551

NOTES:

2.0 ELECTRICAL CHARACTERISTICS

2.1 Terms and Definitions

A number of terms are defined in ISO-11898 that are used to describe the electrical characteristics of a CAN transceiver device. These terms and definitions are summarized in this section.

2.1.1 BUS VOLTAGE

V_{CANL} and V_{CANH} denote the voltages of the bus line wires CANL and CANH relative to ground of each individual CAN node.

2.1.2 COMMON MODE BUS VOLTAGE RANGE

Boundary voltage levels of V_{CANL} and V_{CANH} with respect to ground, for which proper operation will occur, if up to the maximum number of CAN nodes are connected to the bus.

2.1.3 DIFFERENTIAL INTERNAL CAPACITANCE, C_{DIFF} (OF A CAN NODE)

Capacitance seen between CANL and CANH during the recessive state when the CAN node is disconnected from the bus (see Figure 2-1).

2.1.4 DIFFERENTIAL INTERNAL RESISTANCE, R_{DIFF} (OF A CAN NODE)

Resistance seen between CANL and CANH during the recessive state when the CAN node is disconnected from the bus (see Figure 2-1).

2.1.5 DIFFERENTIAL VOLTAGE, V_{DIFF} (OF CAN BUS)

Differential voltage of the two-wire CAN bus, value $V_{DIFF} = V_{CANH} - V_{CANL}$.

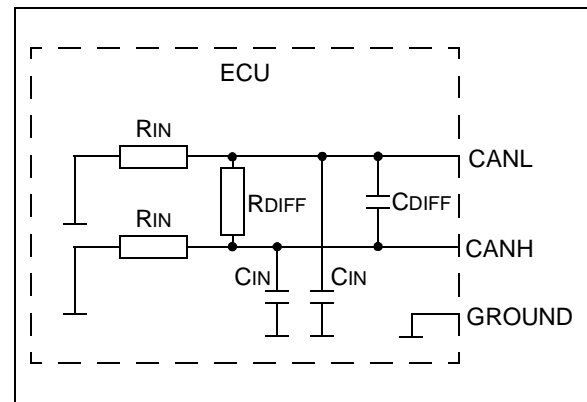
2.1.6 INTERNAL CAPACITANCE, C_{IN} (OF A CAN NODE)

Capacitance seen between CANL (or CANH) and ground during the recessive state when the CAN node is disconnected from the bus (see Figure 2-1).

2.1.7 INTERNAL RESISTANCE, R_{IN} (OF A CAN NODE)

Resistance seen between CANL (or CANH) and ground during the recessive state when the CAN node is disconnected from the bus (see Figure 2-1).

FIGURE 2-1: PHYSICAL LAYER DEFINITIONS



MCP2551

Absolute Maximum Ratings†

VDD.....	7.0V
DC Voltage at TXD, RXD, VREF and Vs.....	-0.3V to VDD + 0.3V
DC Voltage at CANH, CANL (Note 1).....	-42V to +42V
Transient Voltage on Pins 6 and 7 (Note 2).....	-250V to +250V
Storage temperature.....	-55°C to +150°C
Operating ambient temperature.....	-40°C to +125°C
Virtual Junction Temperature, TVJ (Note 3).....	-40°C to +150°C
Soldering temperature of leads (10 seconds).....	+300°C
ESD protection on CANH and CANL pins (Note 4).....	6 kV
ESD protection on all other pins (Note 4).....	4 kV

Note 1: Short-circuit applied when TXD is high and low.

2: In accordance with ISO-7637.

3: In accordance with IEC 60747-1.

4: Classification A: Human Body Model.

† **NOTICE:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2.2 DC Characteristics

DC Specifications			Electrical Characteristics:			
			Industrial (I): $T_{AMB} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ $V_{DD} = 4.5\text{V}$ to 5.5V			
			Extended (E): $T_{AMB} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ $V_{DD} = 4.5\text{V}$ to 5.5V			
Param No.	Sym	Characteristic	Min	Max	Units	Conditions
Supply						
D1	IDD	Supply Current	—	75	mA	Dominant; $V_{TXD} = 0.8\text{V}$; V_{DD}
D2			—	10	mA	Recessive; $V_{TXD} = +2\text{V}$; $R_s = 47\text{ k}\Omega$
D3			—	365	μA	$-40^{\circ}\text{C} \leq T_{AMB} \leq +85^{\circ}\text{C}$, Standby; (Note 2)
	—	465	μA	$-40^{\circ}\text{C} \leq T_{AMB} \leq +125^{\circ}\text{C}$, Standby; (Note 2)		
D4	VPORH	High-level of the power-on reset comparator	3.8	4.3	V	CANH, CANL outputs are active when $V_{DD} > V_{PORH}$
D5	VPORL	Low-level of the power-on reset comparator	3.4	4.0	V	CANH, CANL outputs are not active when $V_{DD} < V_{PORL}$
D6	VPORD	Hysteresis of power-on reset comparator	0.3	0.8	V	Note 1
Bus Line (CANH; CANL) Transmitter						
D7	$V_{CANH(r)}; V_{CANL(r)}$	CANH, CANL Recessive bus voltage	2.0	3.0	V	$V_{TXD} = V_{DD}$; no load.
D8	$I_{O(CANH)(reces)}$ $I_{O(CANL)(reces)}$	Recessive output current	-2	+2	mA	$-2\text{V} < V_{(CANL, CANH)} < +7\text{V}$, $0\text{V} < V_{DD} < 5.5\text{V}$
D9			-10	+10	mA	$-5\text{V} < V_{(CANL, CANH)} < +40\text{V}$, $0\text{V} < V_{DD} < 5.5\text{V}$
D10	$V_{O(CANH)}$	CANH dominant output voltage	2.75	4.5	V	$V_{TXD} = 0.8\text{V}$
D11	$V_{O(CANL)}$	CANL dominant output voltage	0.5	2.25	V	$V_{TXD} = 0.8\text{V}$
D12	$V_{DIFF(r)(o)}$	Recessive differential output voltage	-500	+50	mV	$V_{TXD} = 2\text{V}$; no load
D13	$V_{DIFF(d)(o)}$	Dominant differential output voltage	1.5	3.0	V	$V_{TXD} = 0.8\text{V}$; $V_{DD} = 5\text{V}$ $40\Omega < R_L < 60\Omega$ (Note 2)
D14	$I_{O(SC)(CANH)}$	CANH short-circuit output current	—	-200	mA	$V_{CANH} = -5\text{V}$
D15			—	-100 (typical)	mA	$V_{CANH} = -40\text{V}, +40\text{V}$. (Note 1)
D16	$I_{O(SC)(CANL)}$	CANL short-circuit output current	—	200	mA	$V_{CANL} = -40\text{V}, +40\text{V}$. (Note 1)
Bus Line (CANH; CANL) Receiver: [TXD = 2V; pins 6 and 7 externally driven]						
D17	$V_{DIFF(r)(i)}$	Recessive differential input voltage	-1.0	+0.5	V	$-2\text{V} < V_{(CANL, CANH)} < +7\text{V}$ (Note 3)
			-1.0	+0.4	V	$-12\text{V} < V_{(CANL, CANH)} < +12\text{V}$ (Note 3)
D18	$V_{DIFF(d)(i)}$	Dominant differential input voltage	0.9	5.0	V	$-2\text{V} < V_{(CANL, CANH)} < +7\text{V}$ (Note 3)
			1.0	5.0	V	$-12\text{V} < V_{(CANL, CANH)} < +12\text{V}$ (Note 3)
D19	$V_{DIFF(h)(i)}$	Differential input hysteresis	100	200	mV	see Figure 2-3. (Note 1)
D20	RIN	CANH, CANL common-mode input resistance	5	50	$\text{k}\Omega$	
D21	$R_{IN(d)}$	Deviation between CANH and CANL common-mode input resistance	-3	+3	%	$V_{CANH} = V_{CANL}$

- Note 1:** This parameter is periodically sampled and not 100% tested.
Note 2: $I_{TXD} = I_{RXD} = I_{VREF} = 0\text{ mA}$; $0\text{V} < V_{CANL} < V_{DD}$; $0\text{V} < V_{CANH} < V_{DD}$; $V_{RS} = V_{DD}$.
Note 3: This is valid for the receiver in all modes; High-speed, Slope-control and Standby.

MCP2551

2.2 DC Characteristics (Continued)

DC Specifications (Continued)			Electrical Characteristics:			
			Industrial (I): $T_{AMB} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ $V_{DD} = 4.5\text{V}$ to 5.5V			
			Extended (E): $T_{AMB} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ $V_{DD} = 4.5\text{V}$ to 5.5V			
Param No.	Sym	Characteristic	Min	Max	Units	Conditions
Bus Line (CANH; CANL) Receiver: [TXD = 2V; pins 6 and 7 externally driven]						
D22	RDIFF	Differential input resistance	20	100	k Ω	
D24	ILI	CANH, CANL input leakage current	—	150	μA	$V_{DD} < V_{POR}$; $V_{CANH} = V_{CANL} = +5\text{V}$
Transmitter Data Input (TXD)						
D25	V _{IH}	High-level input voltage	2.0	V _{DD}	V	Output recessive
D26	V _{IL}	Low-level input voltage	V _{SS}	+0.8	V	Output dominant
D27	I _{IH}	High-level input current	-1	+1	μA	V _{TXD} = V _{DD}
D28	I _{IL}	Low-level input current	-100	-400	μA	V _{TXD} = 0V
Receiver Data Output (RXD)						
D31	V _{OH}	High-level output voltage	0.7 V _{DD}	—	V	I _{OH} = 8 mA
D32	V _{OL}	Low-level output voltage	—	0.8	V	I _{OL} = 8 mA
Voltage Reference Output (VREF)						
D33	V _{REF}	Reference output voltage	0.45 V _{DD}	0.55 V _{DD}	V	$-50 \mu\text{A} < I_{VREF} < 50 \mu\text{A}$
Standby/Slope-Control (Rs pin)						
D34	V _{STB}	Input voltage for standby mode	0.75 V _{DD}	—	V	
D35	I _{SLOPE}	Slope-control mode current	-10	-200	μA	
D36	V _{SLOPE}	Slope-control mode voltage	0.4 V _{DD}	0.6 V _{DD}	V	
Thermal Shutdown						
D37	T _{J(sd)}	Shutdown junction temperature	155	180	$^{\circ}\text{C}$	Note 1
D38	T _{J(h)}	Shutdown temperature hysteresis	20	30	$^{\circ}\text{C}$	$-12\text{V} < V(\text{CANL}, \text{CANH}) < +12\text{V}$ (Note 3)

- Note 1:** This parameter is periodically sampled and not 100% tested.
Note 2: I_{TXD} = I_{RXD} = I_{VREF} = 0 mA; 0V < V_{CANL} < V_{DD}; 0V < V_{CANH} < V_{DD}; V_{RS} = V_{DD}.
Note 3: This is valid for the receiver in all modes; High-speed, Slope-control and Standby.

FIGURE 2-1: TEST CIRCUIT FOR ELECTRICAL CHARACTERISTICS

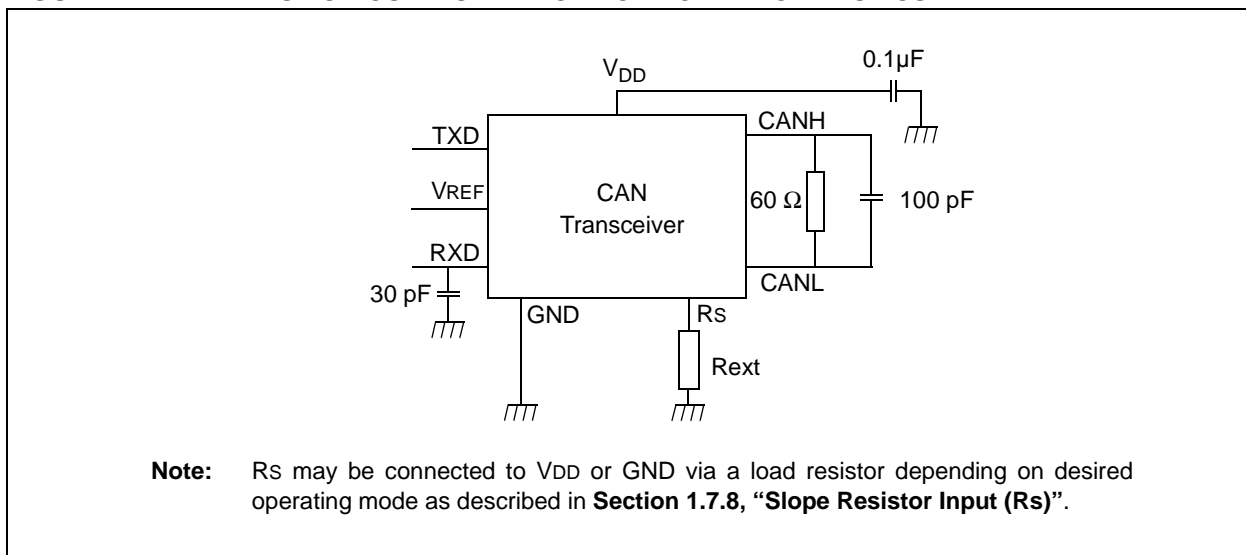


FIGURE 2-2: TEST CIRCUIT FOR AUTOMOTIVE TRANSIENTS

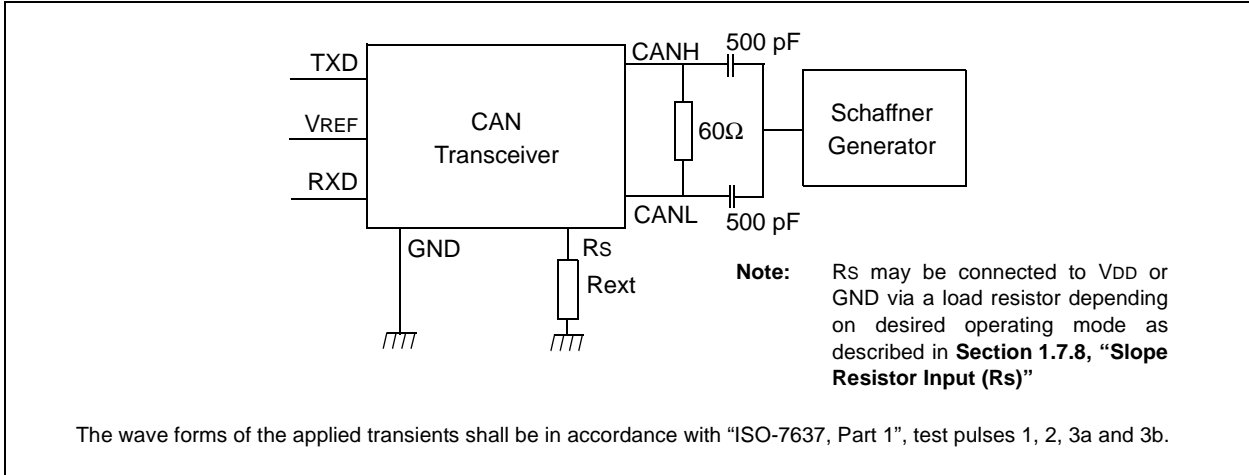
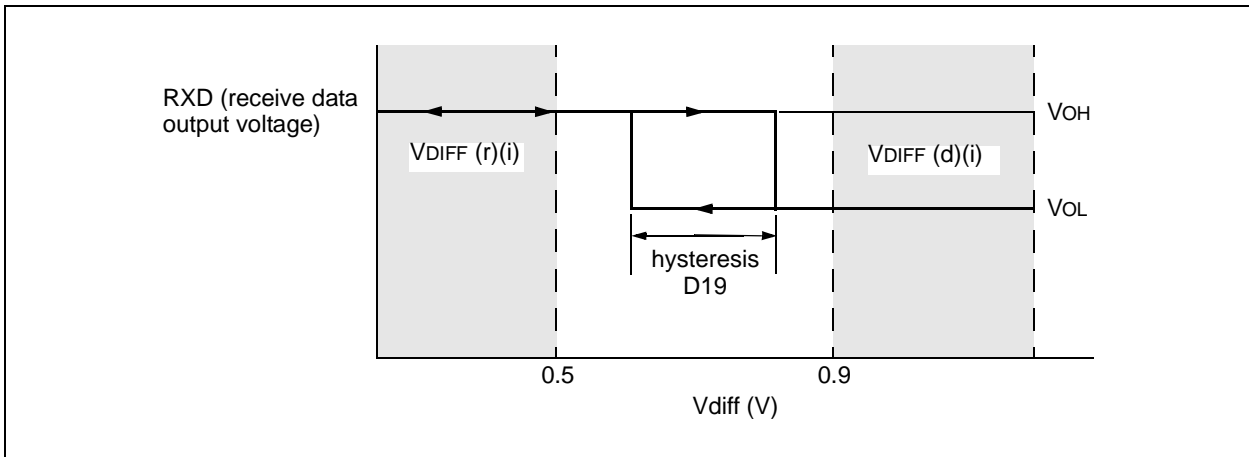


FIGURE 2-3: HYSTERESIS OF THE RECEIVER



MCP2551

2.3 AC Characteristics

AC Specifications			Electrical Characteristics: Industrial (I): T _{AMB} = -40°C to +85°C V _{DD} = 4.5V to 5.5V Extended (E): T _{AMB} = -40°C to +125°C V _{DD} = 4.5V to 5.5V			
Param No.	Sym	Characteristic	Min	Max	Units	Conditions
1	tBIT	Bit time	1	62.5	μs	V _{RS} = 0V
2	fBIT	Bit frequency	16	1000	kHz	V _{RS} = 0V
3	TtxL2bus(d)	Delay TXD to bus active	—	70	ns	-40°C ≤ T _{AMB} ≤ +125°C, V _{RS} = 0V
4	TtxH2bus(r)	Delay TXD to bus inactive	—	125	ns	-40°C ≤ T _{AMB} ≤ +85°C, V _{RS} = 0V
			—	170	ns	-40°C ≤ T _{AMB} ≤ +125°C, V _{RS} = 0V
5	TtxL2rx(d)	Delay TXD to receive active	—	130	ns	-40°C ≤ T _{AMB} ≤ +125°C, V _{RS} = 0V
			—	250	ns	-40°C ≤ T _{AMB} ≤ +125°C, R _S = 47 kΩ
6	TtxH2rx(r)	Delay TXD to receiver inactive	—	175	ns	-40°C ≤ T _{AMB} ≤ +85°C, V _{RS} = 0V
			—	225	ns	-40°C ≤ T _{AMB} ≤ +85°C, R _S = 47 kΩ
			—	235	ns	-40°C ≤ T _{AMB} ≤ +125°C, V _{RS} = 0V
			—	400	ns	-40°C ≤ T _{AMB} ≤ +125°C, R _S = 47 kΩ
7	SR	CANH, CANL slew rate	5.5	8.5	V/μs	Refer to Figure 1-1; R _S = 47 kΩ, (Note 1)
10	twAKE	Wake-up time from standby (R _S pin)	—	5	μs	see Figure 2-5
11	TbusD2rx(s)	Bus dominant to RXD Low (Standby mode)	—	550	ns	V _{RS} = +4V; (see Figure 2-2)
12	C _{IN} (CANH) C _{IN} (CANL)	CANH; CANL input capacitance	—	20 (typical)	pF	1 Mbit/s data rate; V _{TXD} = V _{DD} , (Note 1)
13	CDIFF	Differential input capacitance	—	10 (typical)	pF	1 Mbit/s data rate (Note 1)
14	TtxL2busZ	TX Permanent Dominant Timer Disable Time	1.25	4	ms	
15	TtxR2pdt(res)	TX Permanent Dominant Timer Reset Time	—	1	μs	Rising edge on TXD while device is in permanent dominant state

Note 1: This parameter is periodically sampled and not 100% tested.

2.4 Timing Diagrams and Specifications

FIGURE 2-4: TIMING DIAGRAM FOR AC CHARACTERISTICS

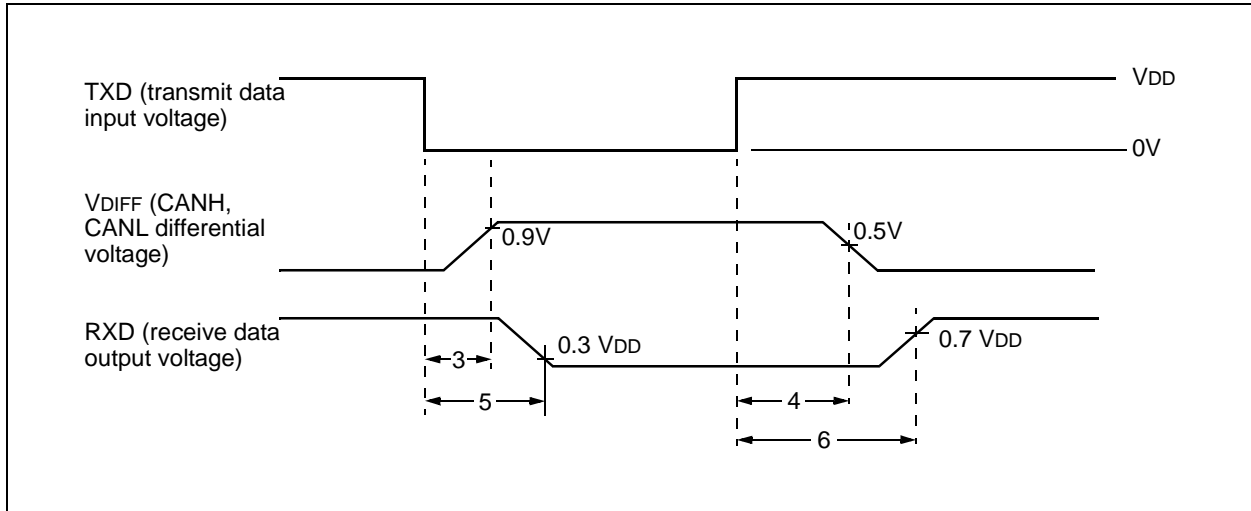


FIGURE 2-5: TIMING DIAGRAM FOR WAKE-UP FROM STANDBY

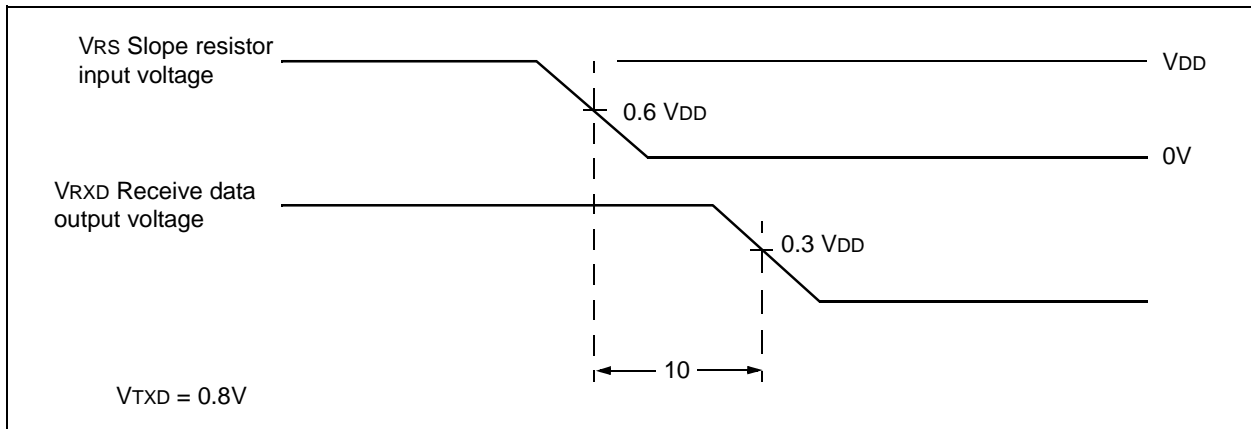
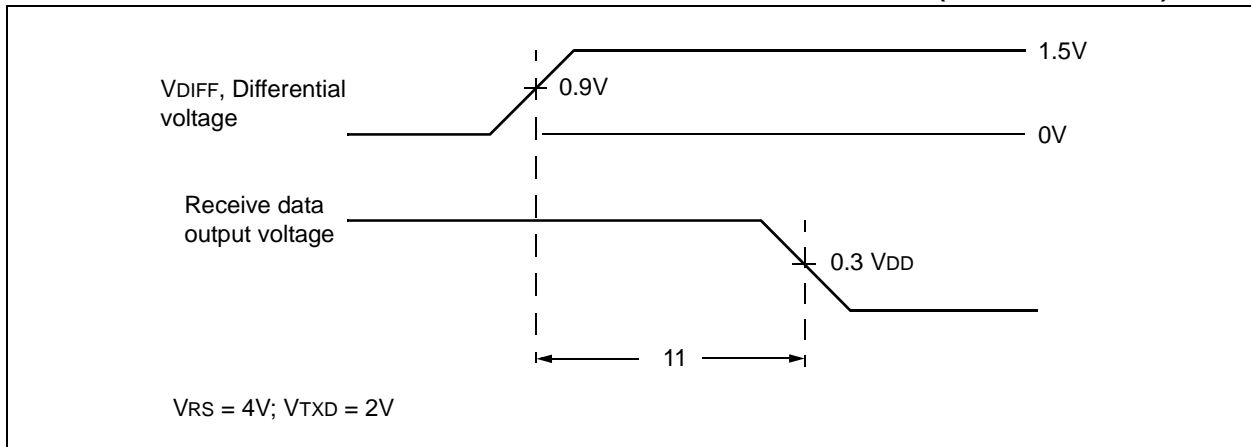


FIGURE 2-2: TIMING DIAGRAM FOR BUS DOMINANT TO RXD LOW (STANDBY MODE)



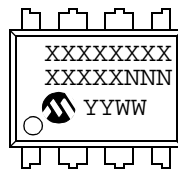
MCP2551

NOTES:

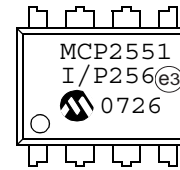
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

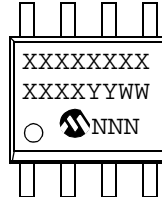
8-Lead PDIP (300 mil)



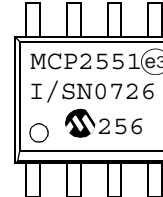
Example:



8-Lead SOIC (150 mil)



Example:

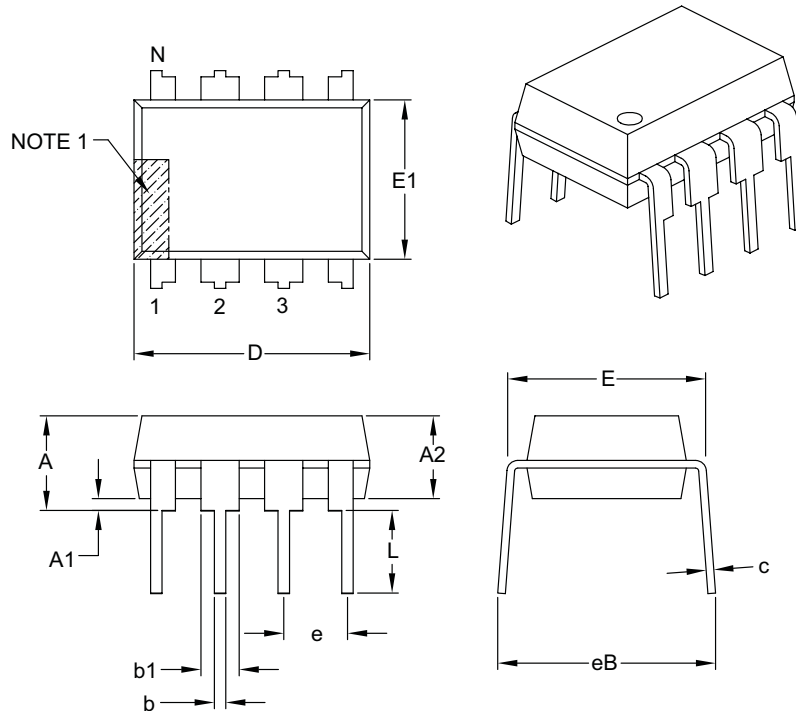


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

MCP2551

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

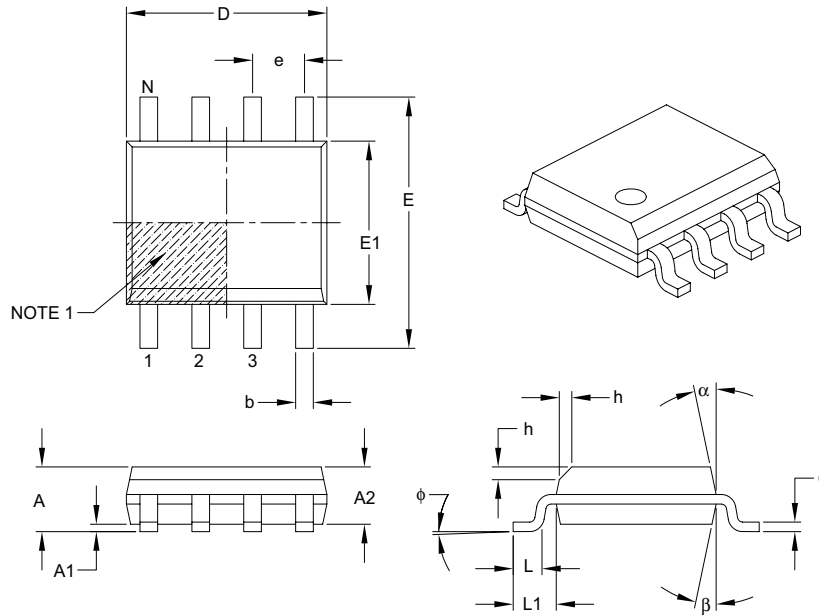
- Pin 1 visual index feature may vary, but must be located with the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

MCP2551

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>
Device	Temperature Range	Package
Device:	MCP2551= High-Speed CAN Transceiver	
Temperature Range:	I = -40°C to +85°C	E = -40°C to +125°C
Package:	P = Plastic DIP (300 mil Body) 8-lead	SN = Plastic SOIC (150 mil Body) 8-lead

Examples:

- a) MCP2551-I/P: Industrial temperature, PDIP package.
- b) MCP2551-E/P: Extended temperature, PDIP package.
- c) MCP2551-I/SN: Industrial temperature, SOIC package.
- d) MCP2551T-I/SN: Tape and Reel, Industrial Temperature, SOIC package.
- e) MCP2551T-E/SN: Tape and Reel, Extended Temperature, SOIC package.

MCP2551

NOTES:

APPENDIX A: REVISION HISTORY

Revision E (January 2007)

This revision includes updates to the packaging diagrams.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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