

Figure 1. MC145026 Encoder Block Diagram

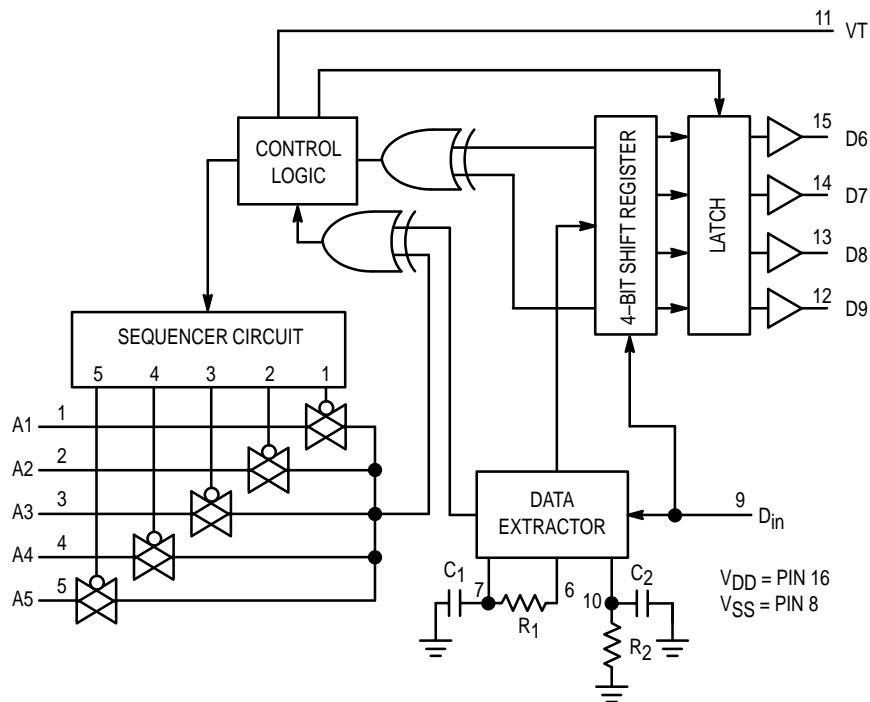


Figure 2. MC145027 Decoder Block Diagram

ELECTRICAL CHARACTERISTICS — MC145026*, MC145027, and MC145028 (Voltage Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	Guaranteed Limit						Unit
			- 40°C		25°C		85°C		
			Min	Max	Min	Max	Min	Max	
V _{OL}	Low-Level Output Voltage ($V_{in} = V_{DD}$ or 0)	5.0	—	0.05	—	0.05	—	0.05	V
		10	—	0.05	—	0.05	—	0.05	
		15	—	0.05	—	0.05	—	0.05	
V _{OH}	High-Level Output Voltage ($V_{in} = 0$ or V_{DD})	5.0	4.95	—	4.95	—	4.95	—	V
		10	9.95	—	9.95	—	9.95	—	
		15	14.95	—	14.95	—	14.95	—	
V _{IL}	Low-Level Input Voltage ($V_{out} = 4.5$ or 0.5 V) ($V_{out} = 9.0$ or 1.0 V) ($V_{out} = 13.5$ or 1.5 V)	5.0	—	1.5	—	1.5	—	1.5	V
		10	—	3.0	—	3.0	—	3.0	
		15	—	4.0	—	4.0	—	4.0	
V _{IH}	High-Level Input Voltage ($V_{out} = 0.5$ or 4.5 V) ($V_{out} = 1.0$ or 9.0 V) ($V_{out} = 1.5$ or 13.5 V)	5.0	3.5	—	3.5	—	3.5	—	V
		10	7.0	—	7.0	—	7.0	—	
		15	11	—	11	—	11	—	
I _{OH}	High-Level Output Current ($V_{out} = 2.5$ V) ($V_{out} = 4.6$ V) ($V_{out} = 9.5$ V) ($V_{out} = 13.5$ V)	5.0	-2.5	—	-2.1	—	-1.7	—	mA
		5.0	-0.52	—	-0.44	—	-0.36	—	
		10	-1.3	—	-1.1	—	-0.9	—	
		15	-3.6	—	-3.0	—	-2.4	—	
I _{OL}	Low-Level Output Current ($V_{out} = 0.4$ V) ($V_{out} = 0.5$ V) ($V_{out} = 1.5$ V)	5.0	0.52	—	0.44	—	0.36	—	mA
		10	1.3	—	1.1	—	0.9	—	
		15	3.6	—	3.0	—	2.4	—	
I _{in}	Input Current — $\bar{T}\bar{E}$ (MC145026, Pull-Up Device)	5.0	—	—	3.0	11	—	—	μ A
		10	—	—	16	60	—	—	
		15	—	—	35	120	—	—	
I _{in}	Input Current R_S (MC145026), D_{in} (MC145027, MC145028)	15	—	± 0.3	—	± 0.3	—	± 1.0	μ A
I _{in}	Input Current A1 – A5, A6/D6 – A9/D9 (MC145026), A1 – A5 (MC145027), A1 – A9 (MC145028)	5.0	—	—	—	± 110	—	—	μ A
		10	—	—	—	± 500	—	—	
		15	—	—	—	± 1000	—	—	
C _{in}	Input Capacitance ($V_{in} = 0$)	—	—	—	—	7.5	—	—	pF
I _{DD}	Quiescent Current — MC145026	5.0	—	—	—	0.1	—	—	μ A
		10	—	—	—	0.2	—	—	
		15	—	—	—	0.3	—	—	
I _{DD}	Quiescent Current — MC145027, MC145028	5.0	—	—	—	50	—	—	μ A
		10	—	—	—	100	—	—	
		15	—	—	—	150	—	—	
I _{dd}	Dynamic Supply Current — MC145026 ($f_C = 20$ kHz)	5.0	—	—	—	200	—	—	μ A
		10	—	—	—	400	—	—	
		15	—	—	—	600	—	—	
I _{dd}	Dynamic Supply Current — MC145027, MC145028 ($f_C = 20$ kHz)	5.0	—	—	—	400	—	—	μ A
		10	—	—	—	800	—	—	
		15	—	—	—	1200	—	—	

* Also see next Electrical Characteristics table for 2.5 V specifications.

ELECTRICAL CHARACTERISTICS — MC145026 (Voltage Referenced to V_{SS})

Symbol	Characteristic	V _{DD} V	Guaranteed Limit						Unit
			- 40°C		25°C		85°C		
			Min	Max	Min	Max	Min	Max	
V _{OL}	Low-Level Output Voltage (V _{in} = 0 V or V _{DD})	2.5	—	0.05	—	0.05	—	0.05	V
V _{OH}	High-Level Output Voltage (V _{in} = 0 V or V _{DD})	2.5	2.45	—	2.45	—	2.45	—	V
V _{IL}	Low-Level Input Voltage (V _{out} = 0.5 V or 2.0 V)	2.5	—	0.3	—	0.3	—	0.3	V
V _{IH}	High-Level Input Voltage (V _{out} = 0.5 V or 2.0 V)	2.5	2.2	—	2.2	—	2.2	—	V
I _{OH}	High-Level Output Current (V _{out} = 1.25 V)	2.5	0.28	—	0.25	—	0.2	—	mA
I _{OL}	Low-Level Output Current (V _{out} = 0.4 V)	2.5	0.22	—	0.2	—	0.16	—	mA
I _{in}	Input Current (\overline{TE} — Pull-Up Device)	2.5	—	—	0.09	1.8	—	—	μA
I _{in}	Input Current (A1–A5, A6/D6–A9/D9)	2.5	—	—	—	± 25	—	—	μA
I _{DD}	Quiescent Current	2.5	—	—	—	0.05	—	—	μA
I _{dd}	Dynamic Supply Current (f _C = 20 kHz)	2.5	—	—	—	40	—	—	μA

SWITCHING CHARACTERISTICS — MC145026*, MC145027, and MC145028 (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	Figure No.	V _{DD}	Guaranteed Limit		Unit
				Min	Max	
t _{TLH} , t _{THL}	Output Transition Time	4, 8	5.0 10 15	— — —	200 100 80	ns
t _r	D _{in} Rise Time — Decoders	5	5.0 10 15	— — —	15 15 15	μs
t _f	D _{in} Fall Time — Decoders	5	5.0 10 15	— — —	15 5.0 4.0	μs
f _{osc}	Encoder Clock Frequency	6	5.0 10 15	0.001 0.001 0.001	2.0 5.0 10	MHz
f	Decoder Frequency — Referenced to Encoder Clock	12	5.0 10 15	1.0 1.0 1.0	240 410 450	kHz
t _w	\overline{TE} Pulse Width — Encoders	7	5.0 10 15	65 30 20	— — —	ns

* Also see next Switching Characteristics table for 2.5 V specifications.

SWITCHING CHARACTERISTICS — MC145026 (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	Figure No.	V _{DD}	Guaranteed Limit		Unit
				Min	Max	
t _{TLH} , t _{THL}	Output Transition Time	4, 8	2.5	—	450	ns
f _{osc}	Encoder Clock Frequency	6	2.5	1.0	250	kHz
t _w	\overline{TE} Pulse Width	7	2.5	1.5	—	μs

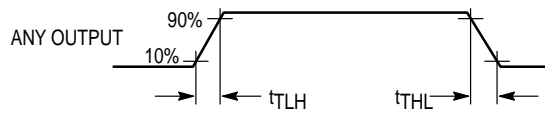


Figure 4.

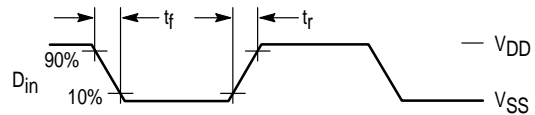


Figure 5.

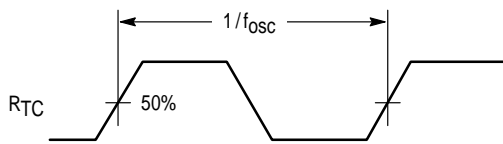


Figure 6.

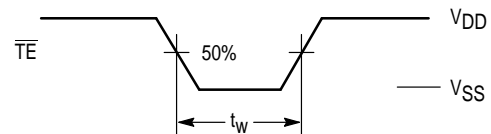
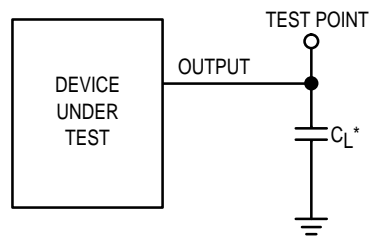


Figure 7.



* Includes all probe and fixture capacitance.

Figure 8. Test Circuit

OPERATING CHARACTERISTICS

MC145026

The encoder serially transmits trinary data as defined by the state of the A1 – A5 and A6/D6 – A9/D9 input pins. These pins may be in either of three states (low, high, or open) allowing 19,683 possible codes. The transmit sequence is initiated by a low level on the \overline{TE} input pin. Upon power-up, the MC145026 can continuously transmit as long as \overline{TE} remains low (also, the device can transmit two-word sequences by pulsing \overline{TE} low). However, no MC145026 application should be designed to rely upon the first data word transmitted immediately after power-up because this word may be invalid. Between the two data words, no signal is sent for three data periods (see Figure 10).

Each transmitted trinary digit is encoded into pulses (see Figure 11). A logic 0 (low) is encoded as two consecutive short pulses, a logic 1 (high) as two consecutive long pulses, and an open (high impedance) as a long pulse followed by a short pulse. The input state is determined by using a weak “output” device to try to force each input high then low. If only a high state results from the two tests, the input is assumed to be hardwired to V_{DD} . If only a low state is obtained, the input is assumed to be hardwired to V_{SS} . If both a high and a low can be forced at an input, an open is assumed and is encoded as such. The “high” and “low” levels are 70% and 30% of the supply voltage as shown in the Electrical Characteristics table. The weak “output” device sinks/sources up to 110 μ A at a 5 V supply level, 500 μ A at 10 V, and 1 mA at 15 V.

The \overline{TE} input has an internal pull-up device so that a simple switch may be used to force the input low. While \overline{TE} is high and the second-word transmission has timed out, the encoder is completely disabled, the oscillator is inhibited, and the current drain is reduced to quiescent current. When \overline{TE} is brought low, the oscillator is started and the transmit sequence begins. The inputs are then sequentially selected, and determinations are made as to the input logic states. This information is serially transmitted via the D_{out} pin.

MC145027

This decoder receives the serial data from the encoder and outputs the data, if it is valid. The transmitted data, consisting of two identical words, is examined bit by bit during reception. The first five trinary digits are assumed to be the address. If the received address matches the local address, the next four (data) bits are internally stored, but are not transferred to the output data latch. As the second encoded word is received, the address must again match. If a match occurs, the new data bits are checked against the previously stored data bits. If the two nibbles of data (four bits each) match, the data is transferred to the output data latch by VT and remains until new data replaces it. At the same time, the VT output pin is brought high and remains high until an error is received or until no input signal is received for four data periods (see Figure 10).

Although the address information may be encoded in trinary, the data information must be either a 1 or 0. A trinary (open) data line is decoded as a logic 1.

MC145028

This decoder operates in the same manner as the MC145027 except that nine address lines are used and no data output is available. The VT output is used to indicate that a valid address has been received. For transmission security, two identical transmitted words must be consecutively received before a VT output signal is issued.

The MC145028 allows 19,683 addresses when trinary levels are used. 512 addresses are possible when binary levels are used.

PIN DESCRIPTIONS

MC145026 ENCODER

A1 – A5, A6/D6 – A9/D9

Address, Address/Data Inputs (Pins 1 – 7, 9, and 10)

These address/data inputs are encoded and the data is sent serially from the encoder via the D_{out} pin.

RS, CTC, RTC

(Pins 11, 12, and 13)

These pins are part of the oscillator section of the encoder (see Figure 9).

If an external signal source is used instead of the internal oscillator, it should be connected to the R_S input and the R_{TC} and C_{TC} pins should be left open.

\overline{TE}

Transmit Enable (Pin 14)

This active-low transmit enable input initiates transmission when forced low. An internal pull-up device keeps this input normally high. The pull-up current is specified in the Electrical Characteristics table.

D_{out}

Data Out (Pin 15)

This is the output of the encoder that serially presents the encoded data word.

V_{SS}

Negative Power Supply (Pin 8)

The most-negative supply potential. This pin is usually ground.

V_{DD}

Positive Power Supply (Pin 16)

The most-positive power supply pin.

MC145027 AND MC145028 DECODERS

A1 – A5, A1 – A9

Address Inputs (Pins 1 – 5) — MC145027,

Address Inputs (Pins 1 – 5, 15, 14, 13, 12) — MC145028

These are the local address inputs. The states of these pins must match the appropriate encoder inputs for the VT pin to go high. The local address may be encoded with trinary or binary data.

D6 – D9

Data Outputs (Pins 15, 14, 13, 12) — MC145027 Only

These outputs present the binary information that is on encoder inputs A6/D6 through A9/D9. Only binary data is

acknowledged; a trinary open at the MC145026 encoder is decoded as a high level (logic 1).

D_{in}
Data In (Pin 9)

This pin is the serial data input to the decoder. The input voltage must be at CMOS logic levels. The signal source driving this pin must be dc coupled.

R₁, C₁
Resistor 1, Capacitor 1 (Pins 6, 7)

As shown in Figures 2 and 3, these pins accept a resistor and capacitor that are used to determine whether a narrow pulse or wide pulse has been received. The time constant $R_1 \times C_1$ should be set to 1.72 encoder clock periods:

$$R_1 C_1 = 3.95 R_{TC} C_{TC}$$

R₂/C₂
Resistor 2/Capacitor 2 (Pin 10)

As shown in Figures 2 and 3, this pin accepts a resistor and capacitor that are used to detect both the end of a received word and the end of a transmission. The time constant $R_2 \times C_2$ should be 33.5 encoder clock periods (four data periods per Figure 11): $R_2 C_2 = 77 R_{TC} C_{TC}$. This time

constant is used to determine whether the D_{in} pin has remained low for four data periods (end of transmission). A separate on-chip comparator looks at the voltage-equivalent two data periods ($0.4 R_2 C_2$) to detect the dead time between received words within a transmission.

VT
Valid Transmission Output (Pin 11)

This valid transmission output goes high after the second word of an encoding sequence when the following conditions are satisfied:

1. the received addresses of both words match the local decoder address, and
2. the received data bits of both words match.

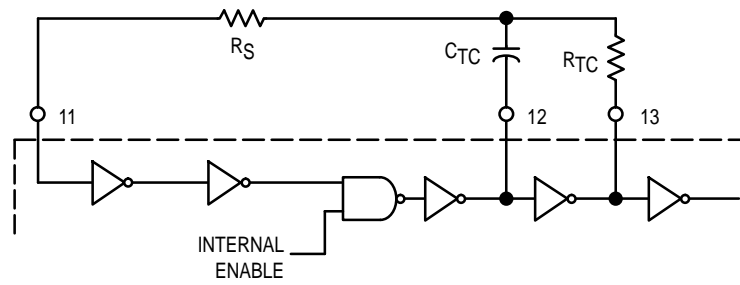
VT remains high until either a mismatch is received or no input signal is received for four data periods.

V_{SS}
Negative Power Supply (Pin 8)

The most-negative supply potential. This pin is usually ground.

V_{DD}
Positive Power Supply (Pin 16)

The most-positive power supply pin.



This oscillator operates at a frequency determined by the external RC network; i.e.,

$$f \approx \frac{1}{2.3 R_{TC} C_{TC'}} \text{ (Hz)}$$

for $1 \text{ kHz} \leq f \leq 400 \text{ kHz}$

where: $C_{TC'} = C_{TC} + C_{\text{layout}} + 12 \text{ pF}$

$R_S \approx 2 R_{TC}$

$R_S \geq 20 \text{ k}$

$R_{TC} \geq 10 \text{ k}$

$400 \text{ pF} < C_{TC} < 15 \text{ }\mu\text{F}$

The value for R_S should be chosen to be ≥ 2 times R_{TC} . This range ensures that current through R_S is insignificant compared to current through R_{TC} . The upper limit for R_S must ensure that $R_S \times 5 \text{ pF}$ (input capacitance) is small compared to $R_{TC} \times C_{TC}$.

For frequencies outside the indicated range, the formula is less accurate. The minimum recommended oscillation frequency of this circuit is 1 kHz. Susceptibility to externally induced noise signals may occur for frequencies below 1 kHz and/or when resistors utilized are greater than 1 M Ω .

Figure 9. Encoder Oscillator Information

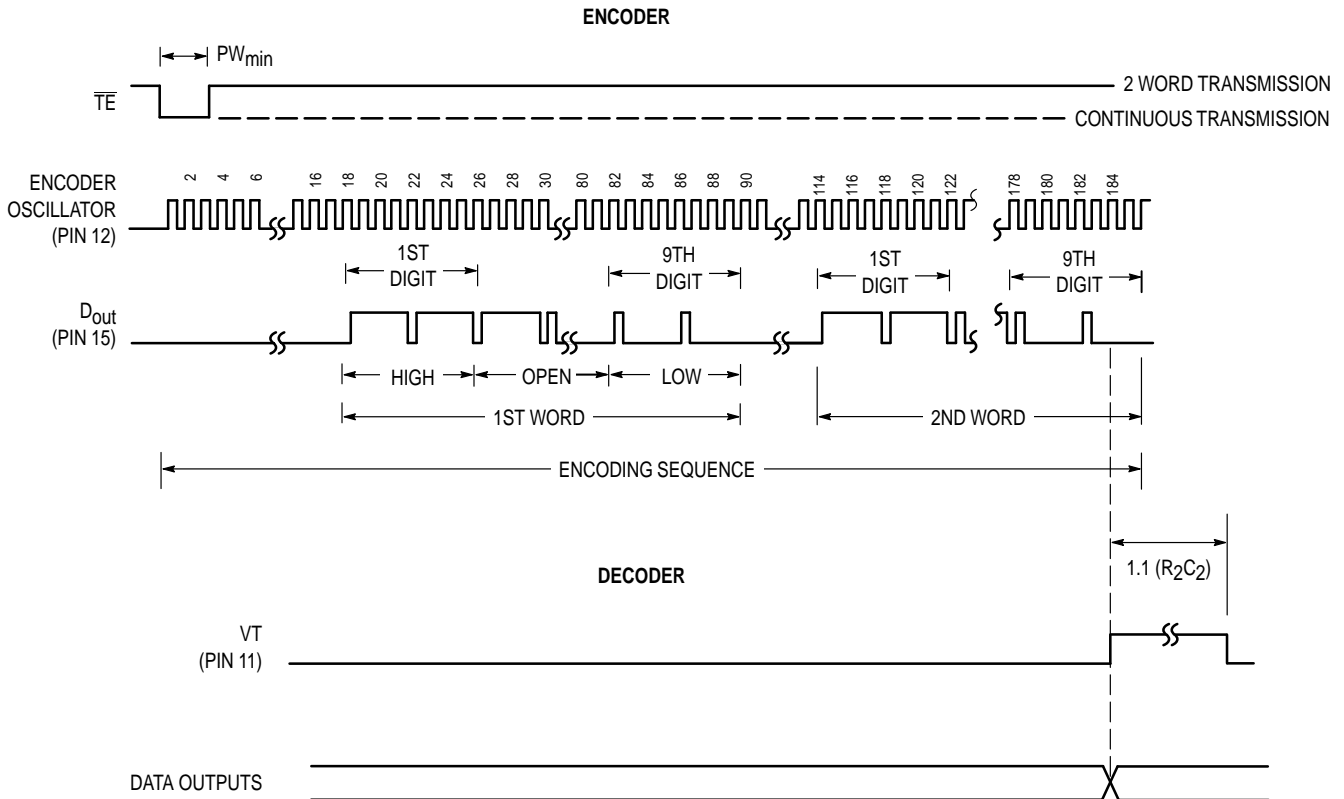


Figure 10. Timing Diagram

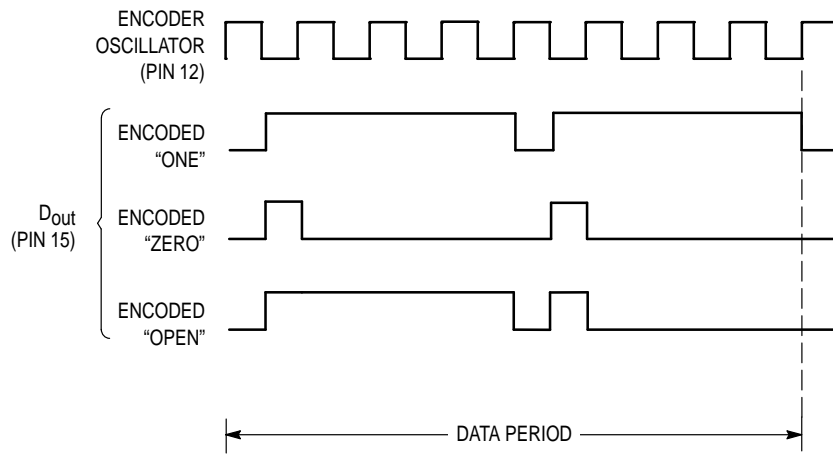


Figure 11. Encoder Data Waveforms

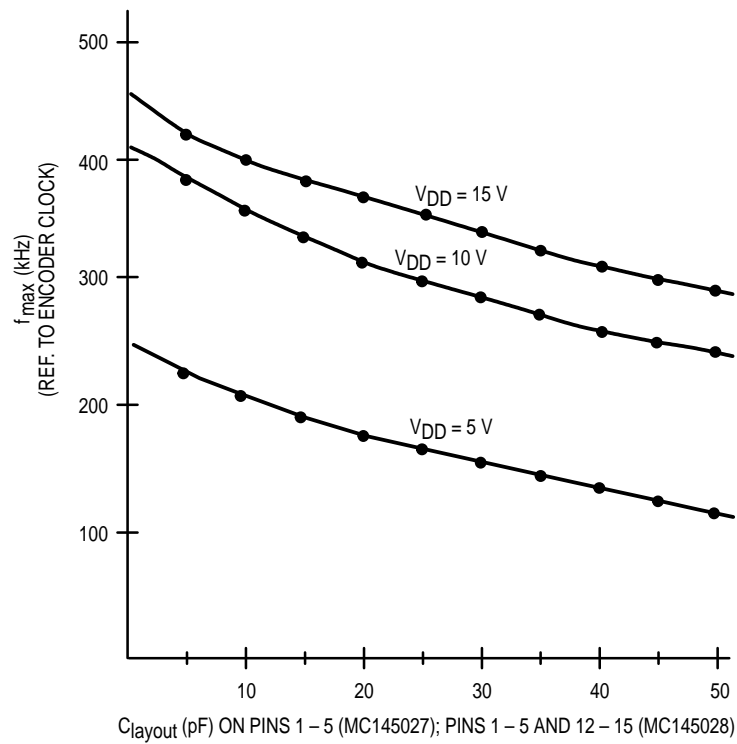


Figure 12. f_{max} vs C_{layout} — Decoders Only

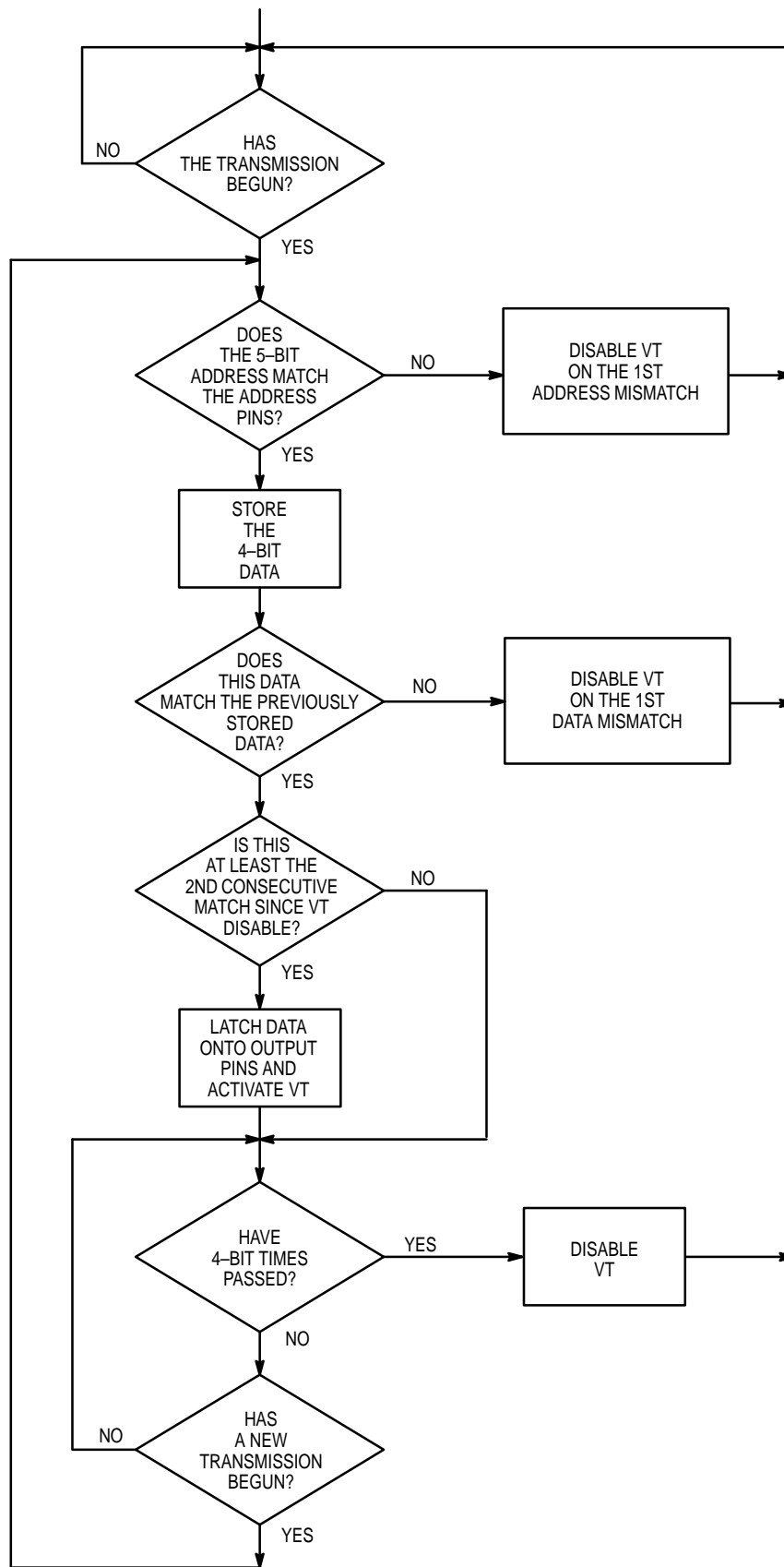


Figure 13. MC145027 Flowchart

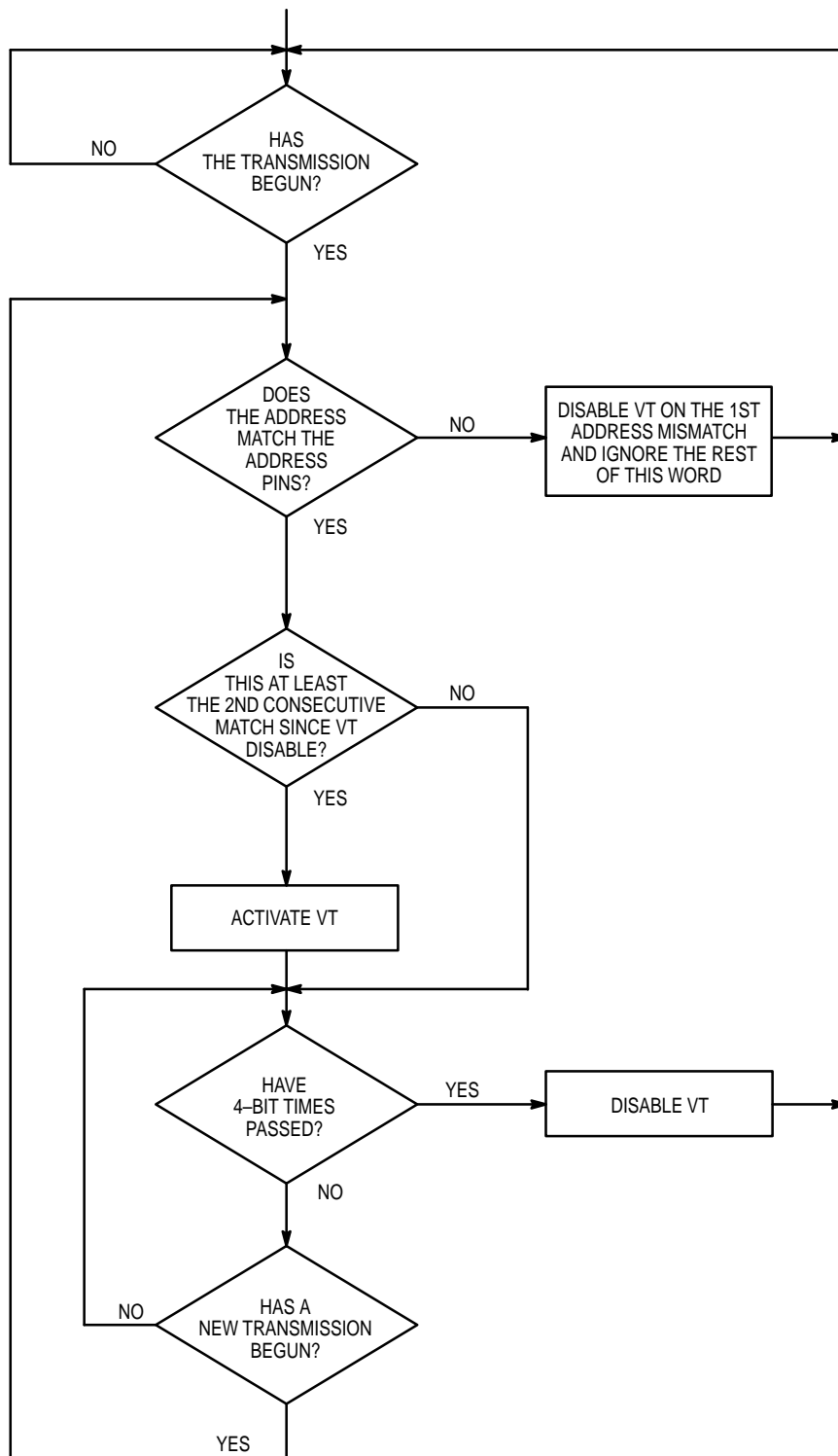


Figure 14. MC145028 Flowchart

MC145027 AND MC145028 TIMING

To verify the MC145027 or MC145028 timing, check the waveforms on C1 (Pin 7) and R2/C2 (Pin 10) as compared to the incoming data waveform on D_{in} (Pin 9).

The R–C decay seen on C1 discharges down to $1/3 V_{DD}$ before being reset to V_{DD} . This point of reset (labelled “DOS” in Figure 15) is the point in time where the decision is made whether the data seen on D_{in} is a 1 or 0. DOS should not be too close to the D_{in} data edges or intermittent operation may occur.

The other timing to be checked on the MC145027 and MC145028 is on R2/C2 (see Figure 16). The R–C decay is continually reset to V_{DD} as data is being transmitted. Only between words and after the end-of-transmission (EOT) does R2/C2 decay significantly from V_{DD} . R2/C2 can be used to identify the internal end-of-word (EOW) timing edge which is generated when R2/C2 decays to $2/3 V_{DD}$. The internal EOT timing edge occurs when R2/C2 decays to $1/3 V_{DD}$. When the waveform is being observed, the R–C decay should go down between the $2/3$ and $1/3 V_{DD}$ levels, but not too close to either level before data transmission on D_{in} resumes.

Verification of the timing described above should ensure a good match between the MC145026 transmitter and the MC145027 and MC145028 receivers.

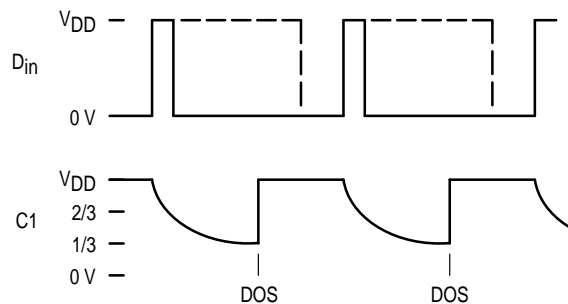


Figure 15. R–C Decay on Pin 7 (C1)

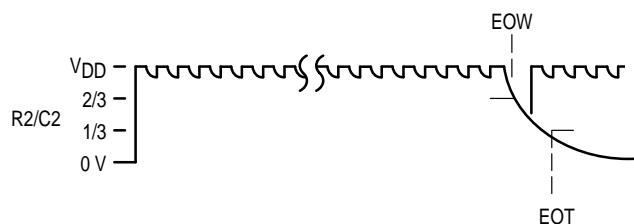
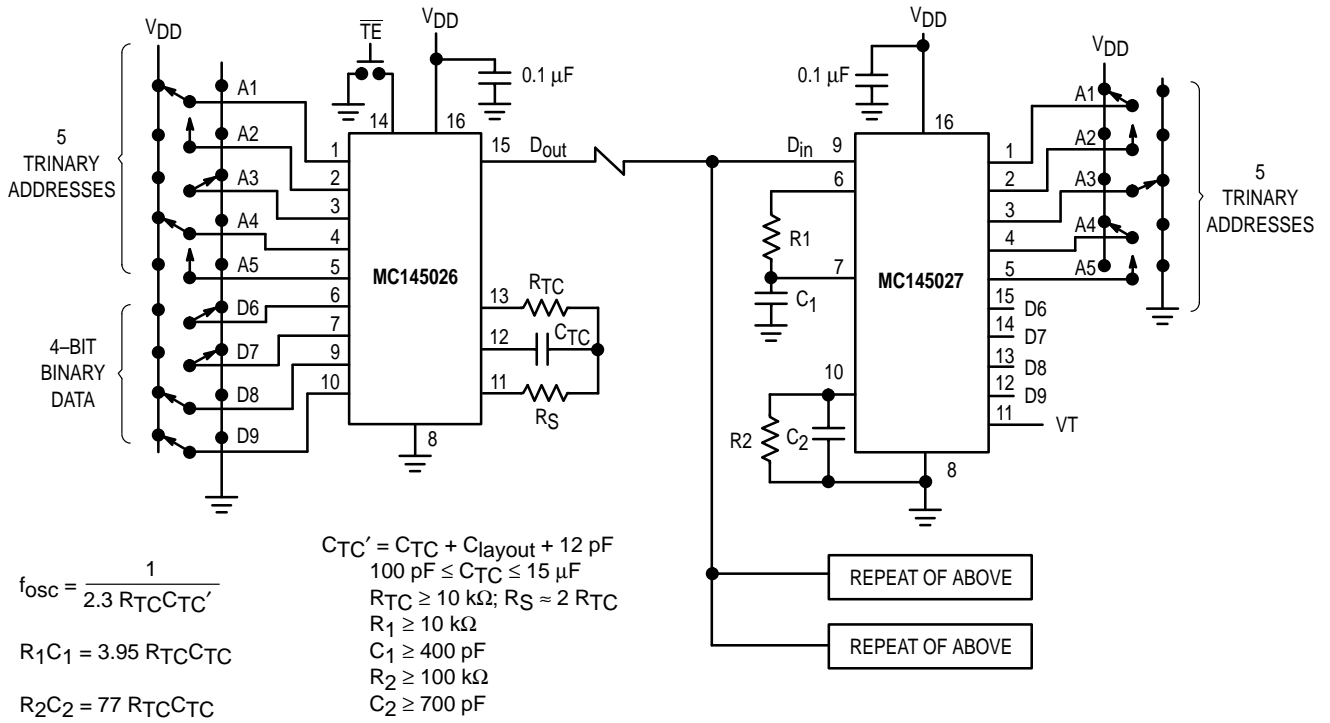


Figure 16. R–C Decay on Pin 10 (R2/C2)



Example R/C Values (All Resistors and Capacitors are $\pm 5\%$)

($C_{TC}' = C_{TC} + 20 \text{ pF}$)

f _{osc} (kHz)	R _{TC}	C _{TC} '	R _S	R ₁	C ₁	R ₂	C ₂
362	10 k	120 pF	20 k	10 k	470 pF	100 k	910 pF
181	10 k	240 pF	20 k	10 k	910 pF	100 k	1800 pF
88.7	10 k	490 pF	20 k	10 k	2000 pF	100 k	3900 pF
42.6	10 k	1020 pF	20 k	10 k	3900 pF	100 k	7500 pF
21.5	10 k	2020 pF	20 k	10 k	8200 pF	100 k	0.015 μF
8.53	10 k	5100 pF	20 k	10 k	0.02 μF	200 k	0.02 μF
1.71	50 k	5100 pF	100 k	50 k	0.02 μF	200 k	0.1 μF

Figure 17. Typical Application

APPLICATIONS INFORMATION

INFRARED TRANSMITTER

In Figure 18, the MC145026 encoder is set to run at an oscillator frequency of about 4 to 9 kHz. Thus, the time required for a complete two-word encoding sequence is about 20 to 40 ms. The data output from the encoder gates an RC oscillator running at 50 kHz; the oscillator shown starts rapidly enough to be used in this application. When the "send" button is not depressed, both the MC145026 and oscillator are in a low-power standby state. The RC oscillator has to be trimmed for 50 kHz and has some drawbacks for frequency stability. A superior system uses a ceramic resonator oscillator running at 400 kHz. This oscillator feeds a divider as shown in Figure 19. The unused inputs of the MC14011UB must be grounded.

The MLED81 IRED is driven with the 50 kHz square wave at about 200 to 300 mA to generate the carrier. If desired, two IREDs wired in series can be used (see Application Note AN1016 for more information). The bipolar IRED switch, shown in Figure 18, offers two advantages over a FET. First, a logic FET has too much gate capacitance for the MC14011UB to drive without waveform distortion. Second, the bipolar drive permits lower supply voltages, which are an advantage in portable battery-powered applications.

The configuration shown in Figure 18 operates over a supply range of 4.5 to 18 V. A low-voltage system which operates down to 2.5 V could be realized if the oscillator section of a MC74HC4060 is used in place of the MC14011UB. The data output of the MC145026 is inverted and fed to the RESET pin of the MC74HC4060. Alternately, the MC74HCU04 could be used for the oscillator.

Information on the MC14011UB is in book number DL131/D. The MC74HCU04 and MC74HC4060 are found in book number DL129/D.

INFRARED RECEIVER

The receiver in Figure 20 couples an IR-sensitive diode to input preamp A1, followed by band-pass amplifier A2 with a gain of about 10. Limiting stage A3 follows, with an output of about 800 mV p-p. The limited 50 kHz burst is detected by comparator A4 that passes only positive pulses, and peak-

detected and filtered by a diode/RC network to extract the data envelope from the burst. Comparator A5 boosts the signal to logic levels compatible with the MC145027/28 data input. The D_{in} pin of these decoders is a standard CMOS high-impedance input which must **not** be allowed to float. Therefore, direct coupling from A5 to the decoder input is utilized.

Shielding should be used on at least A1 and A2, with good ground and high-sensitivity circuit layout techniques applied.

For operation with supplies higher than +5 V, limiter A4's positive output swing needs to be limited to 3 to 5 V. This is accomplished via adding a zener diode in the negative feedback path, thus avoiding excessive system noise. The biasing resistor stack should be adjusted such that V3 is 1.25 to 1.5 V.

This system works up to a range of about 10 meters. The gains of the system may be adjusted to suit the individual design needs. The 100 Ω resistor in the emitter of the first 2N5088 and the 1 k Ω resistor feeding A2 may be altered if different gain is required. In general, more gain does not necessarily result in increased range. This is due to noise floor limitations. The designer should increase transmitter power and/or increase receiver aperture with Fresnel lensing to greatly improve range. See Application Note AN1016 for additional information.

Information on the MC34074 is in data book DL128/D.

TRINARY SWITCH MANUFACTURERS

Midland Ross—Electronic Connector Div.
Greyhill
Augat/Alcoswitch
Aries Electronics

The above companies may not have the switches in a DIP. For more information, call them or consult *eem Electronic Engineers Master Catalog* or the *Gold Book*. **Ask for SPDT with center OFF.**

Alternative: An SPST can be placed in series between a SPDT and the Encoder or Decoder to achieve trinary action.

Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of trinary switch manufacturers.

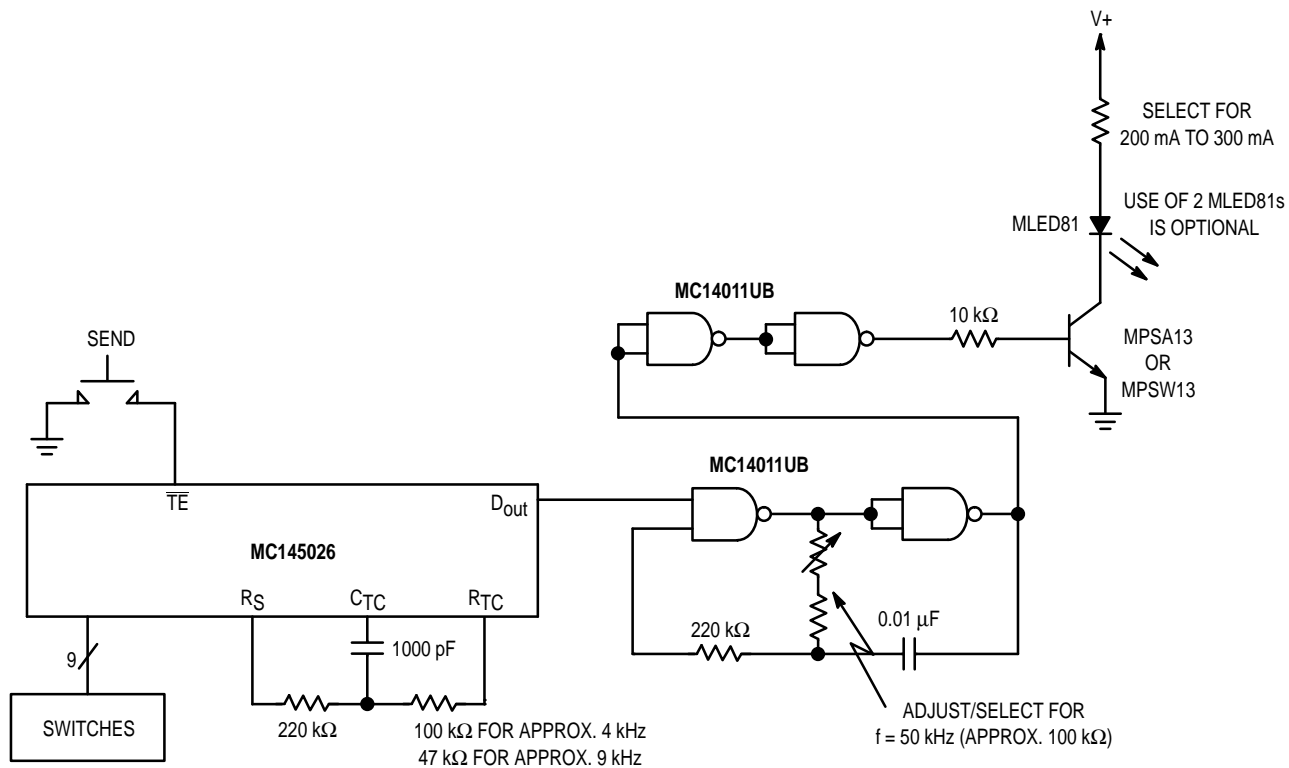


Figure 18. IRED Transmitter Using RC Oscillator to Generate Carrier Frequency

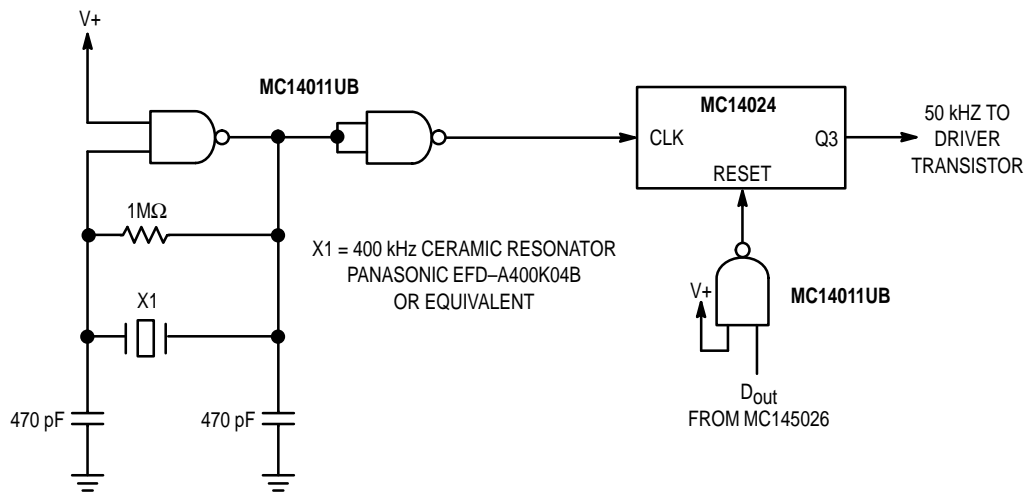


Figure 19. Using a Ceramic Resonator to Generate Carrier Frequency

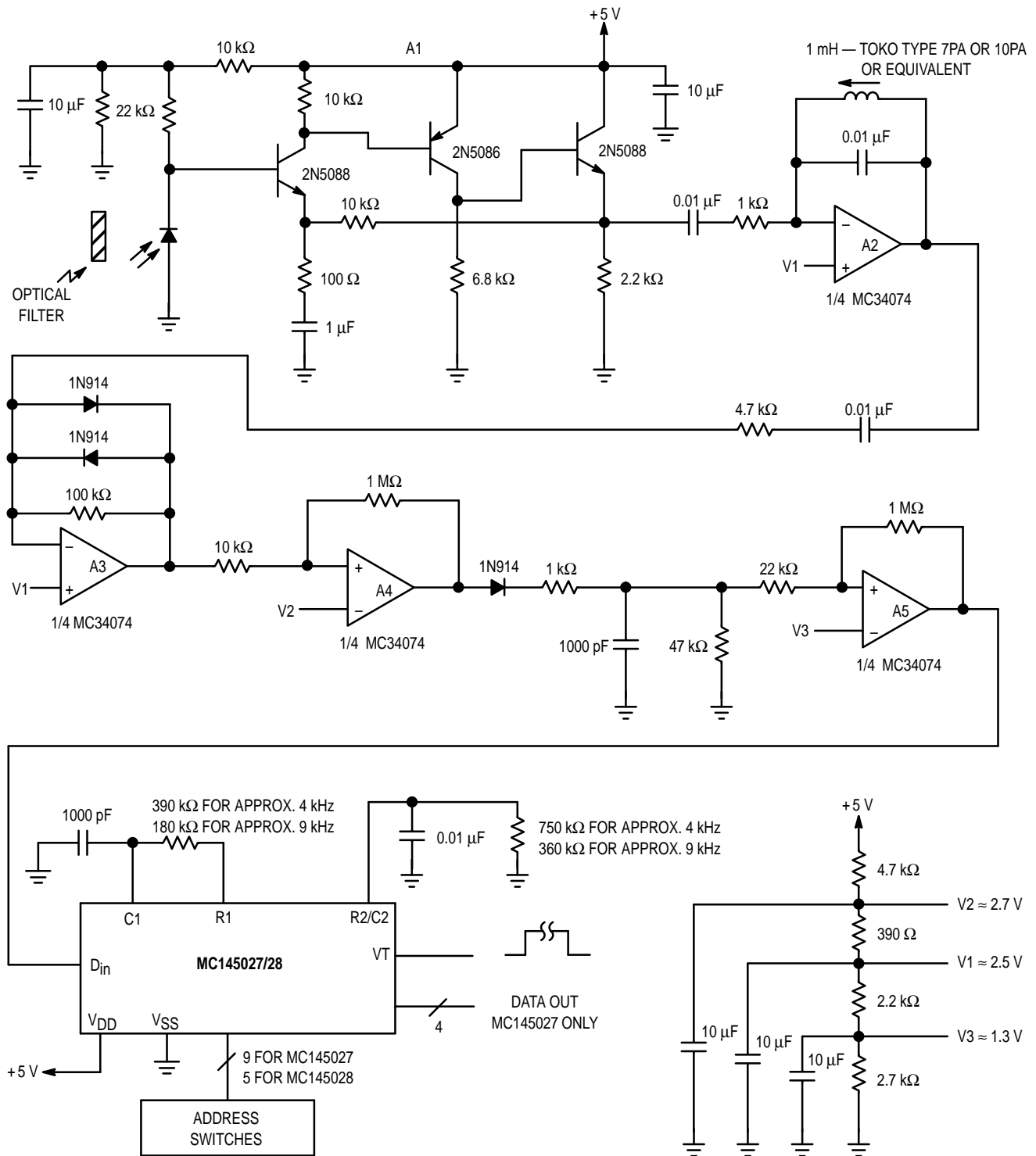
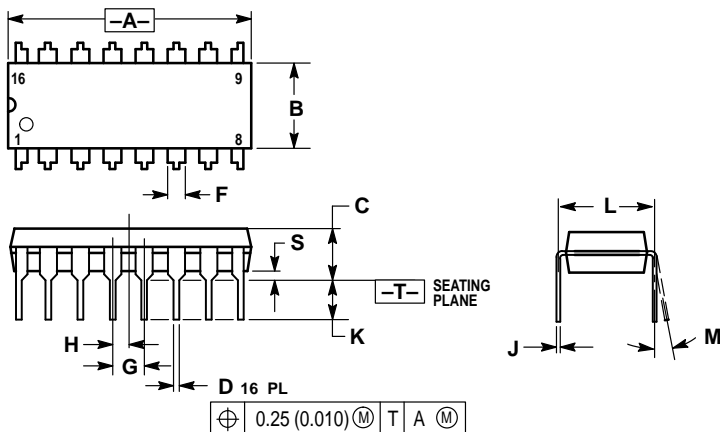


Figure 20. Infrared Receiver

PACKAGE DIMENSIONS

P SUFFIX PLASTIC DIP (DUAL IN-LINE PACKAGE) CASE 648-08

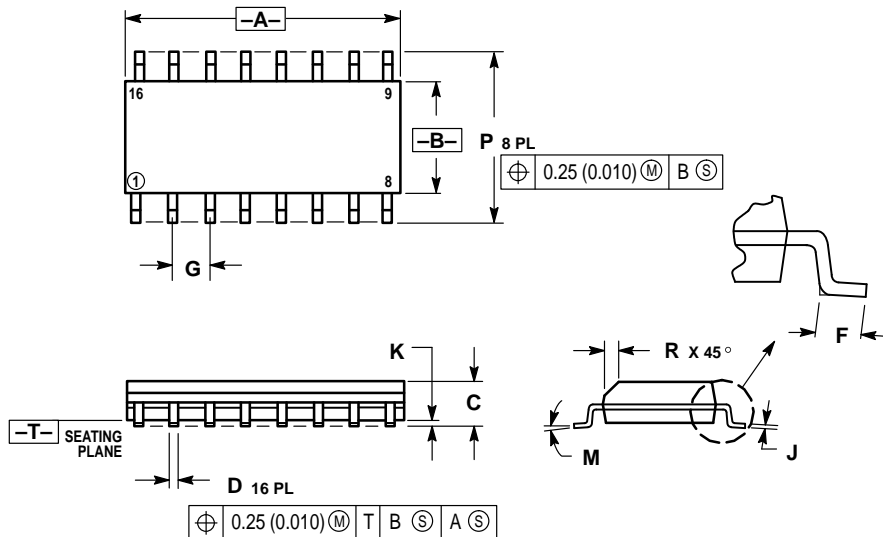


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0° 10°		0° 10°	
S	0.020	0.040	0.51	1.01

D SUFFIX SOG (SMALL OUTLINE GULL-WING) PACKAGE CASE 751B-05

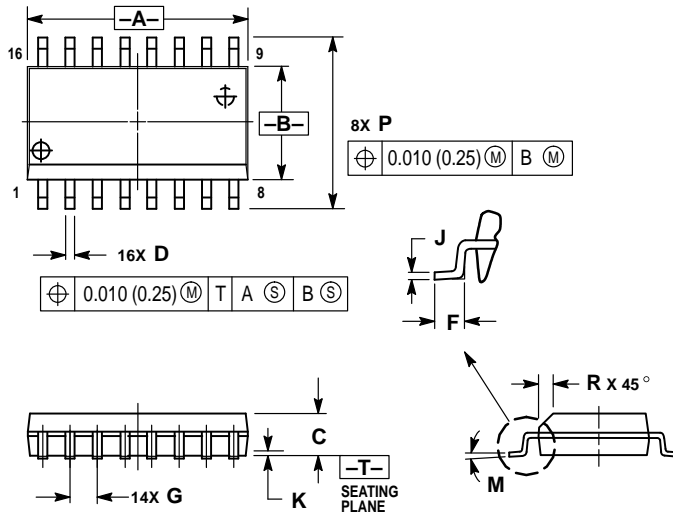


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0° 7°		0° 7°	
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

**DW SUFFIX
SOG (SMALL OUTLINE GULL-WING) PACKAGE
CASE 751G-02**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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