

# MC14029B

## Binary/Decade Up/Down Counter

The MC14029B Binary/Decade up/down counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide toggle flip-flop capability. The counter can be used in either Binary or BCD operation. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design — Count Occurs on Positive Going Edge of Clock
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin for Pin Replacement for CD4029B

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ ) (Note 2.)

| Symbol            | Parameter   | Value                  | Unit               |
|-------------------|---|------------------------|--------------------|
| $V_{DD}$          | DC Supply Voltage Range                           | -0.5 to +18.0          | V                  |
| $V_{in}, V_{out}$ | Input or Output Voltage Range (DC or Transient)   | -0.5 to $V_{DD} + 0.5$ | V                  |
| $I_{in}, I_{out}$ | Input or Output Current (DC or Transient) per Pin | $\pm 10$               | mA                 |
| $P_D$             | Power Dissipation, per Package (Note 3.)          | 500                    | mW                 |
| $T_A$             | Ambient Temperature Range                         | -55 to +125            | $^{\circ}\text{C}$ |
| $T_{stg}$         | Storage Temperature Range                         | -65 to +150            | $^{\circ}\text{C}$ |
| $T_L$             | Lead Temperature (8-Second Soldering)             | 260                    | $^{\circ}\text{C}$ |

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

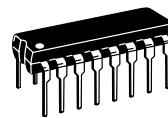
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



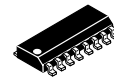
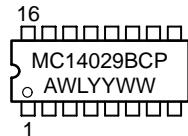
ON Semiconductor

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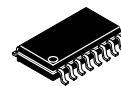
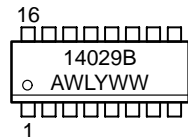
### MARKING DIAGRAMS



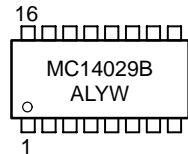
PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



SOEIAJ-16  
F SUFFIX  
CASE 966



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week

### ORDERING INFORMATION

| Device      | Package   | Shipping         |
|-------------|-----------|------------------|
| MC14029BCP  | PDIP-16   | 2000/Box         |
| MC14029BD   | SOIC-16   | 2400/Box         |
| MC14029BDR2 | SOIC-16   | 2500/Tape & Reel |
| MC14029BF   | SOEIAJ-16 | See Note 1.      |
| MC14029BFEL | SOEIAJ-16 | See Note 1.      |

1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

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## PIN ASSIGNMENT

|                  |     |    |                 |
|------------------|-----|----|-----------------|
| PE               | 1 ● | 16 | V <sub>DD</sub> |
| Q3               | 2   | 15 | CLK             |
| P3               | 3   | 14 | Q2              |
| P0               | 4   | 13 | P2              |
| C <sub>in</sub>  | 5   | 12 | P1              |
| Q0               | 6   | 11 | Q1              |
| C <sub>out</sub> | 7   | 10 | U/D             |
| V <sub>SS</sub>  | 8   | 9  | B/D             |

## TRUTH TABLE

| Carry In | Up/Down | Preset Enable | Action     |
|----------|---------|---------------|------------|
| 1        | X       | 0             | No Count   |
| 0        | 1       | 0             | Count Up   |
| 0        | 0       | 0             | Count Down |
| X        | X       | 1             | Preset     |

X = Don't Care

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

| Characteristic  | Symbol                       | V <sub>DD</sub><br>Vdc | - 55°C   |       | 25°C  |                    |       | 125°C |       | Unit |
|---|------------------------------|------------------------|--|-------|-------|--------------------|-------|-------|-------|------|
|   |                              |                        | Min  | Max   | Min   | Typ <sup>(4)</sup> | Max   | Min   | Max   |      |
| Output Voltage<br>V <sub>in</sub> = V <sub>DD</sub> or 0  | "0" Level<br>V <sub>OL</sub> | 5.0                    | —  | 0.05  | —     | 0                  | 0.05  | —     | 0.05  | Vdc  |
|   |                              | 10                     | —  | 0.05  | —     | 0                  | 0.05  | —     | 0.05  |      |
| V <sub>in</sub> = 0 or V <sub>DD</sub>  | "1" Level<br>V <sub>OH</sub> | 5.0                    | 4.95   | —     | 4.95  | 5.0                | —     | 4.95  | —     | Vdc  |
|   |                              | 10                     | 9.95   | —     | 9.95  | 10                 | —     | 9.95  | —     |      |
| Input Voltage<br>(V <sub>O</sub> = 4.5 or 0.5 Vdc)<br>(V <sub>O</sub> = 9.0 or 1.0 Vdc)<br>(V <sub>O</sub> = 13.5 or 1.5 Vdc)   | "0" Level<br>V <sub>IL</sub> | 5.0                    | —  | 1.5   | —     | 2.25               | 1.5   | —     | 1.5   | Vdc  |
|   |                              | 10                     | —  | 3.0   | —     | 4.50               | 3.0   | —     | 3.0   |      |
| (V <sub>O</sub> = 0.5 or 4.5 Vdc)<br>(V <sub>O</sub> = 1.0 or 9.0 Vdc)<br>(V <sub>O</sub> = 1.5 or 13.5 Vdc)  | "1" Level<br>V <sub>IH</sub> | 5.0                    | 3.5  | —     | 3.5   | 2.75               | —     | 3.5   | —     | Vdc  |
|   |                              | 10                     | 7.0  | —     | 7.0   | 5.50               | —     | 7.0   | —     |      |
| Output Drive Current<br>(V <sub>OH</sub> = 2.5 Vdc)<br>(V <sub>OH</sub> = 4.6 Vdc)<br>(V <sub>OH</sub> = 9.5 Vdc)<br>(V <sub>OH</sub> = 13.5 Vdc)                     | Source<br>I <sub>OH</sub>    | 5.0                    | -3.0   | —     | -2.4  | -4.2               | —     | -1.7  | —     | mAdc |
|   |                              | 5.0                    | -0.64  | —     | -0.51 | -0.88              | —     | -0.36 | —     |      |
| (V <sub>OL</sub> = 0.4 Vdc)<br>(V <sub>OL</sub> = 0.5 Vdc)<br>(V <sub>OL</sub> = 1.5 Vdc)   | Sink<br>I <sub>OL</sub>      | 5.0                    | 0.64   | —     | 0.51  | 0.88               | —     | 0.36  | —     | mAdc |
|   |                              | 10                     | 1.6  | —     | 1.3   | 2.25               | —     | 0.9   | —     |      |
|   |                              | 15                     | 4.2  | —     | 3.4   | 8.8                | —     | 2.4   | —     |      |
| Input Current   | I <sub>in</sub>              | 15                     | —  | ± 0.1 | —     | ± 0.00001          | ± 0.1 | —     | ± 1.0 | μAdc |
| Input Capacitance<br>(V <sub>in</sub> = 0)  | C <sub>in</sub>              | —                      | —  | —     | —     | 5.0                | 7.5   | —     | —     | pF   |
| Quiescent Current<br>(Per Package)  | I <sub>DD</sub>              | 5.0                    | —  | 5.0   | —     | 0.005              | 5.0   | —     | 150   | μAdc |
|   |                              | 10                     | —  | 10    | —     | 0.010              | 10    | —     | 300   |      |
|   |                              | 15                     | —  | 20    | —     | 0.015              | 20    | —     | 600   |      |
| Total Supply Current <sup>(5.)</sup> <sup>(6.)</sup><br>(Dynamic plus Quiescent,<br>Per Package)<br>(C <sub>L</sub> = 50 pF on all outputs, all<br>buffers switching) | I <sub>T</sub>               | 5.0                    | I <sub>T</sub> = (0.58 μA/kHz) f + I <sub>DD</sub><br>I <sub>T</sub> = (1.20 μA/kHz) f + I <sub>DD</sub><br>I <sub>T</sub> = (1.70 μA/kHz) f + I <sub>DD</sub> |       |       |                    |       |       |       | μAdc |
|   |                              | 10                     |  |       |       |                    |       |       |       |      |
|   |                              | 15                     |  |       |       |                    |       |       |       |      |

4. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V/fk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.001.

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## SWITCHING CHARACTERISTICS (7.) ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

| Characteristic   | Symbol                     | $V_{DD}$        | All Types         |                   |                   | Unit          |
|--|----------------------------|-----------------|-------------------|-------------------|-------------------|---------------|
|  |                            |                 | Min               | Typ (8.)          | Max               |               |
| Output Rise and Fall Time<br>$t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$<br>$t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$<br>$t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$   | $t_{TLH},$<br>$t_{THL}$    | 5.0<br>10<br>15 | —<br>—<br>—       | 100<br>50<br>40   | 200<br>100<br>80  | ns            |
| Propagation Delay Time<br>Clk to Q<br>$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 230 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$<br><br>Clk to $\overline{C_{out}}$<br>$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 230 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$<br><br>$\overline{C_{in}}$ to $\overline{C_{out}}$<br>$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 95 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 47 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 35 \text{ ns}$<br><br>PE to Q<br>$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 230 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$<br><br>PE to $\overline{C_{out}}$<br>$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 465 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 192 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 125 \text{ ns}$ | $t_{PLH},$<br>$t_{PHL}$    | 5.0<br>10<br>15 | —<br>—<br>—       | 200<br>100<br>90  | 400<br>200<br>180 | ns            |
|  | $t_{PLH},$<br>$t_{PHL}$    | 5.0<br>10<br>15 | —<br>—<br>—       | 250<br>130<br>85  | 500<br>260<br>190 | ns            |
|  | $t_{PLH},$<br>$t_{PHL}$    | 5.0<br>10<br>15 | —<br>—<br>—       | 175<br>50<br>50   | 360<br>120<br>100 | ns            |
|  | $t_{PLH},$<br>$t_{PHL}$    | 5.0<br>10<br>15 | —<br>—<br>—       | 235<br>100<br>80  | 470<br>200<br>160 | ns            |
|  | $t_{PLH},$<br>$t_{PHL}$    | 5.0<br>10<br>15 | —<br>—<br>—       | 320<br>145<br>105 | 640<br>290<br>210 | ns            |
| Clock Pulse Width  | $t_{W(cl)}$                | 5.0<br>10<br>15 | 180<br>80<br>60   | 90<br>40<br>30    | —<br>—<br>—       | ns            |
| Clock Pulse Frequency  | $f_{cl}$                   | 5.0<br>10<br>15 | —<br>—<br>—       | 4.0<br>8.0<br>10  | 2.0<br>4.0<br>5.0 | MHz           |
| Preset Removal Time<br>The Preset Signal must be low prior to a positive-going transition of the clock.  | $t_{rem}$                  | 5.0<br>10<br>15 | 160<br>80<br>60   | 80<br>40<br>30    | —<br>—<br>—       | ns            |
| Clock Rise and Fall Time   | $t_{r(cl)}$<br>$t_{f(cl)}$ | 5.0<br>10<br>15 | —<br>—<br>—       | —<br>—<br>—       | 15<br>5<br>4      | $\mu\text{s}$ |
| Carry In Setup Time  | $t_{su}$                   | 5.0<br>10<br>15 | 150<br>60<br>40   | 75<br>30<br>20    | —<br>—<br>—       | ns            |
| Up/Down Setup Time   |                            | 5.0<br>10<br>15 | 340<br>140<br>100 | 170<br>70<br>50   | —<br>—<br>—       | ns            |
| Binary/Decade Setup Time   |                            | 5.0<br>10<br>15 | 320<br>140<br>100 | 160<br>70<br>50   | —<br>—<br>—       | ns            |
| Preset Enable Pulse Width  | $t_w$                      | 5.0<br>10<br>15 | 130<br>70<br>50   | 65<br>35<br>25    | —<br>—<br>—       | ns            |

7. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

8. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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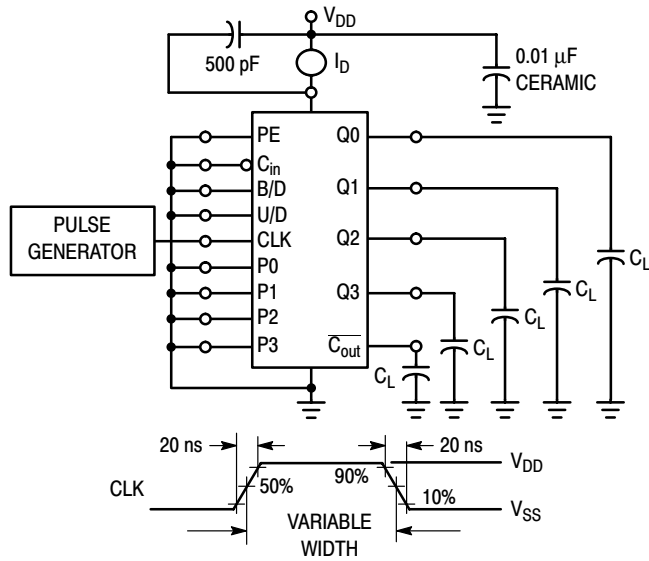


Figure 1. Power Dissipation Test Circuit and Waveform

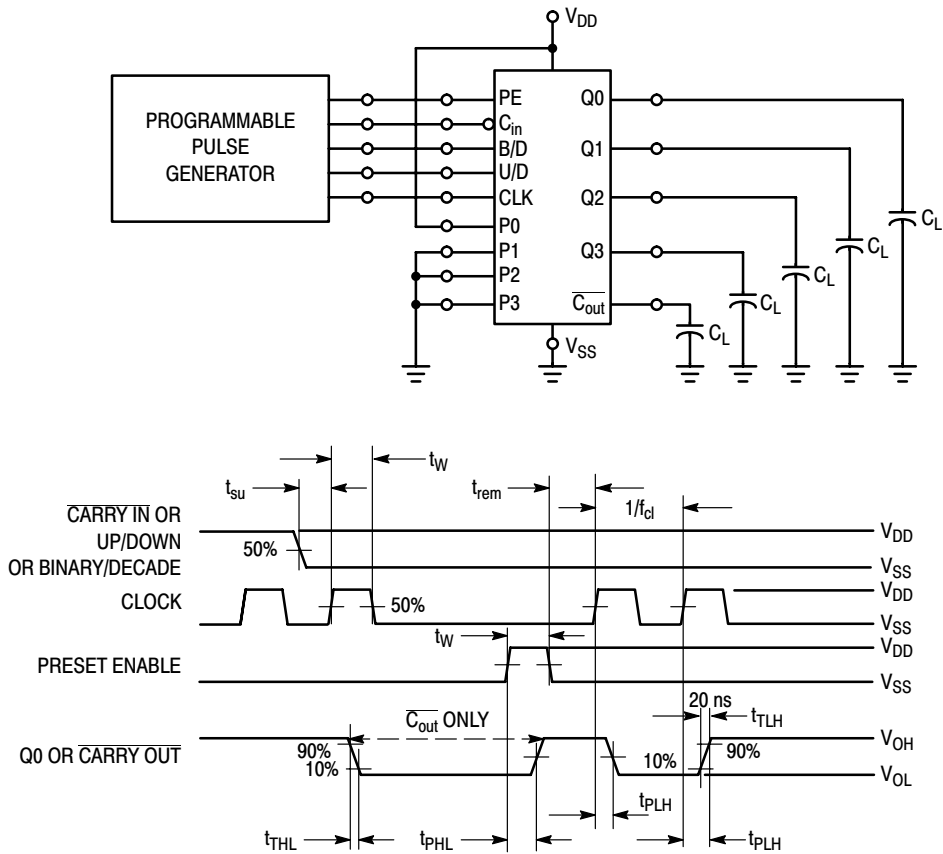
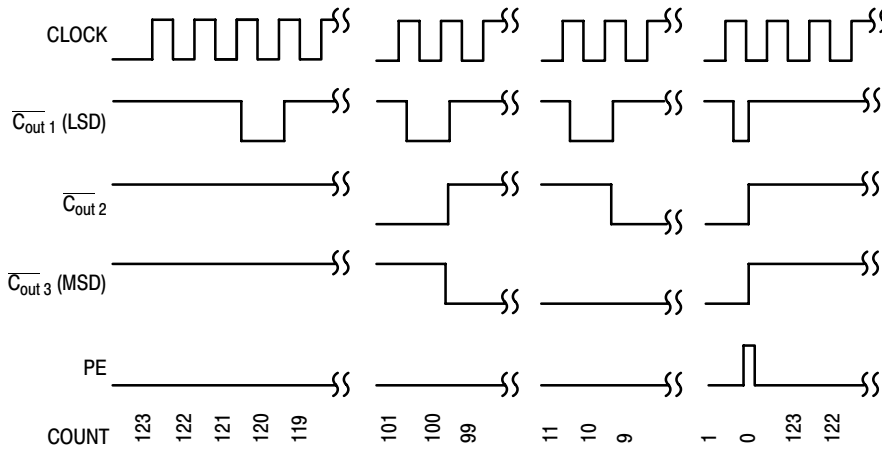
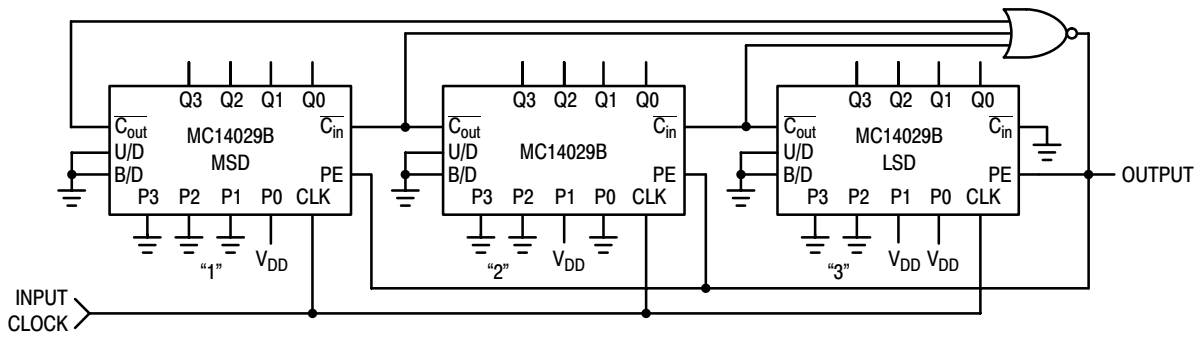
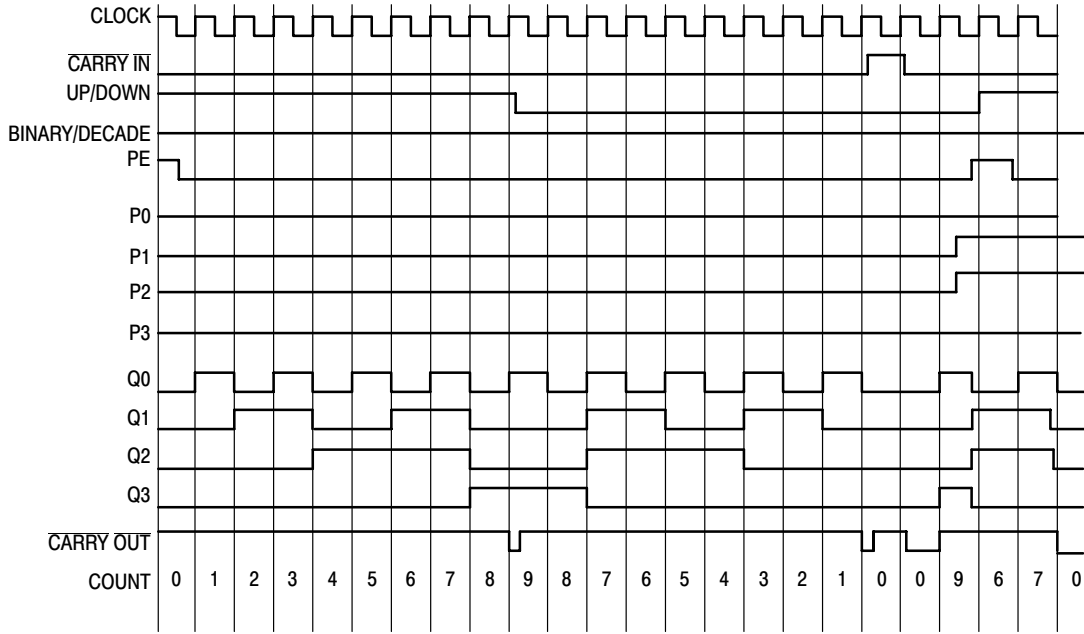


Figure 2. Switching Time Test Circuit and Waveforms

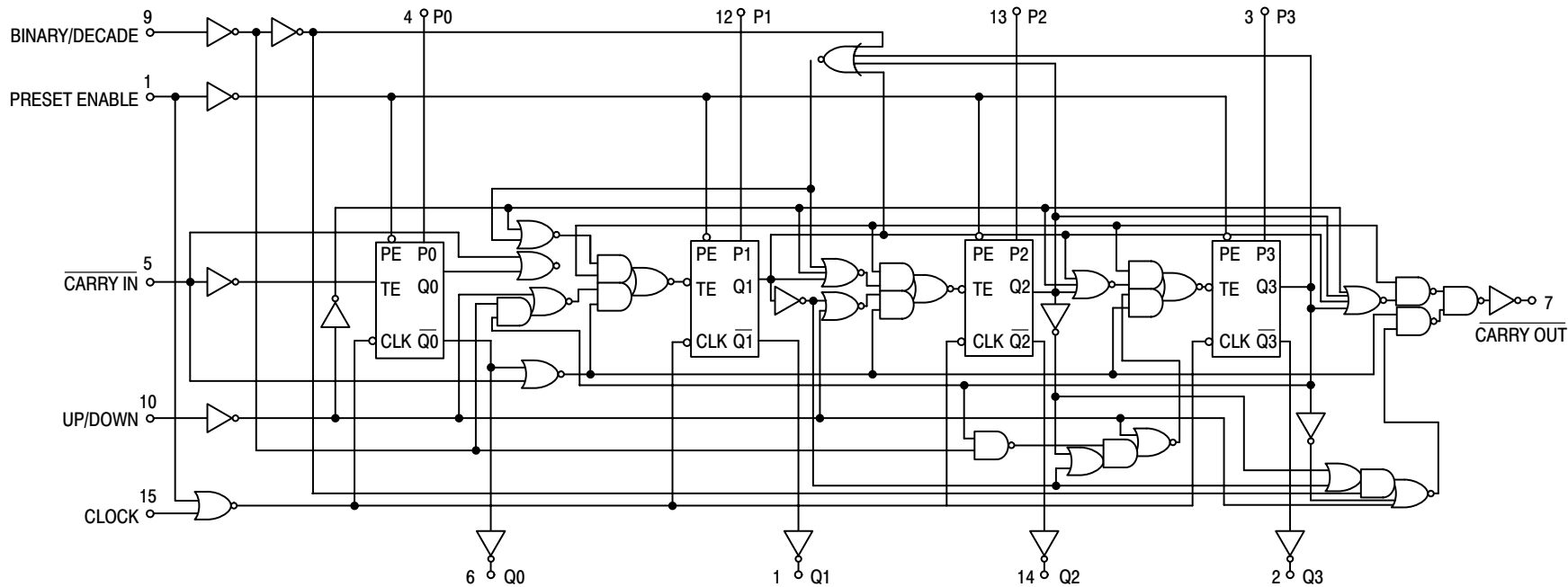
# MC14029B

## TIMING DIAGRAM



\* $t_{W} \cong 900 \text{ ns} @ V_{DD} = 5 \text{ V}$

Figure 3. Divide by N BCD Down Counter and Timing Diagram  
(Shown for N = 123)



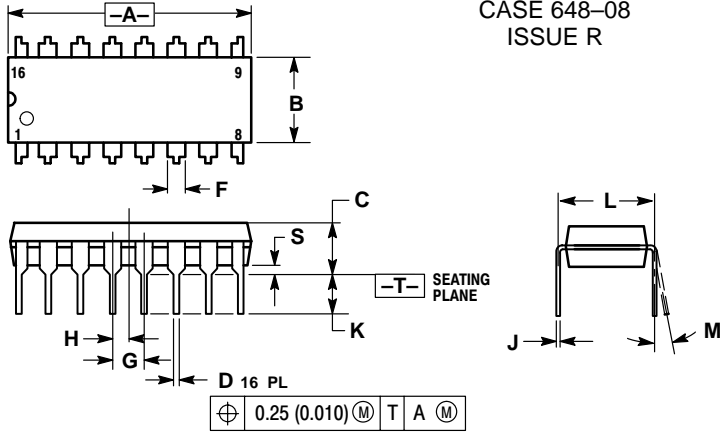
LOGIC DIAGRAM

MC14029B

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## PACKAGE DIMENSIONS

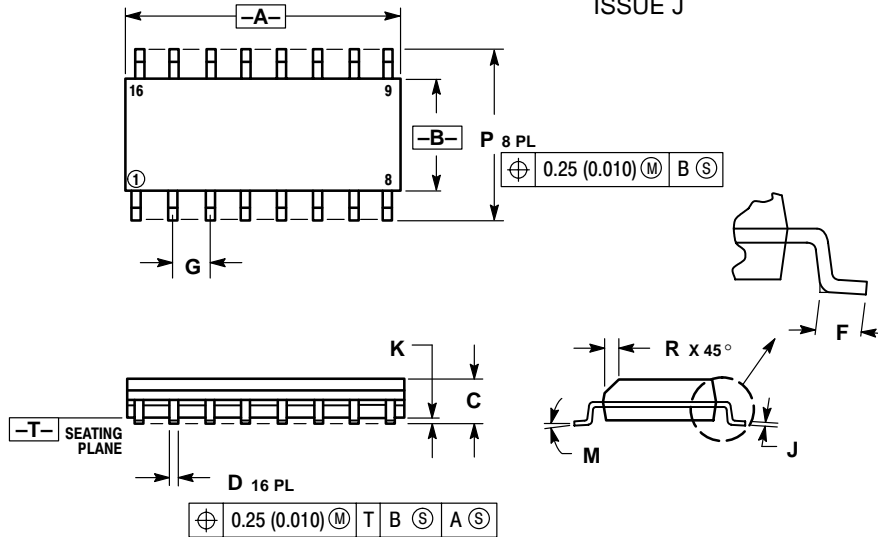
### PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.740     | 0.770 | 18.80       | 19.55 |
| B   | 0.250     | 0.270 | 6.35        | 6.85  |
| C   | 0.145     | 0.175 | 3.69        | 4.44  |
| D   | 0.015     | 0.021 | 0.39        | 0.53  |
| F   | 0.040     | 0.70  | 1.02        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.050 BSC |       | 1.27 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.130 | 2.80        | 3.30  |
| L   | 0.295     | 0.305 | 7.50        | 7.74  |
| M   | 0°        | 10°   | 0°          | 10°   |
| S   | 0.020     | 0.040 | 0.51        | 1.01  |

### SOIC-16 D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



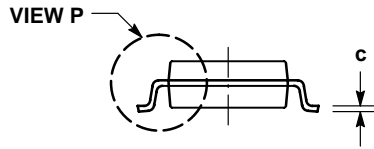
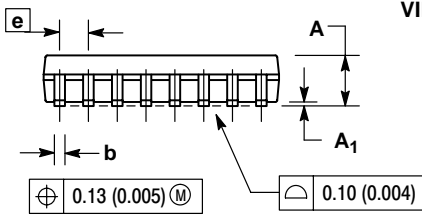
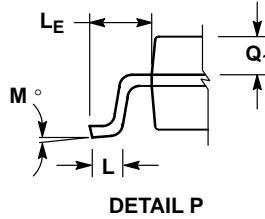
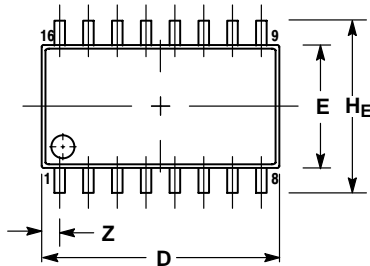
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

# MC14029B

## PACKAGE DIMENSIONS


### SOEIAJ-16 F SUFFIX PLASTIC EIAJ SOIC PACKAGE CASE 966-01 ISSUE O



#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM            | MILLIMETERS |       | INCHES    |       |
|----------------|-------------|-------|-----------|-------|
|                | MIN         | MAX   | MIN       | MAX   |
| A              | ---         | 2.05  | ---       | 0.081 |
| A <sub>1</sub> | 0.05        | 0.20  | 0.002     | 0.008 |
| b              | 0.35        | 0.50  | 0.014     | 0.020 |
| c              | 0.18        | 0.27  | 0.007     | 0.011 |
| D              | 9.90        | 10.50 | 0.390     | 0.413 |
| E              | 5.10        | 5.45  | 0.201     | 0.215 |
| e              | 1.27 BSC    |       | 0.050 BSC |       |
| HE             | 7.40        | 8.20  | 0.291     | 0.323 |
| L              | 0.50        | 0.85  | 0.020     | 0.033 |
| LE             | 1.10        | 1.50  | 0.043     | 0.059 |
| M              | 0°          | 10°   | 0°        | 10°   |
| Q <sub>1</sub> | 0.70        | 0.90  | 0.028     | 0.035 |
| Z              | ---         | 0.78  | ---       | 0.031 |

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