DS04-27248-1E

ASSP for Power Supply Applications (Secondary battery)

DC/DC Converter IC for Charging Li-ion Battery

MB39A125/126

■ DESCRIPTION

MB39A125/126 is a DC/DC converter IC for charging Li-ion battery, which is suitable for down-conversion, and uses pulse width modulation (PWM) for controlling the output voltage and current independently. This IC integrates the build-in comparator for the voltage detection of the AC adapter, and selects the AC adapter or battery automatically for power supply to the system.

Provides a wide range of power supply voltage, low standby current, and high efficiency, which makes them ideal as a built-in charging device in products such as notebook PC.

■ FEATURES

- High efficiency : 97% (MAX)
- Built-in two constant current control circuits
- Analog control of the charging current value (+INE1, +INE2 terminal)
- Built-in AC adapter voltage detection function (ACOK, XACOK terminal)

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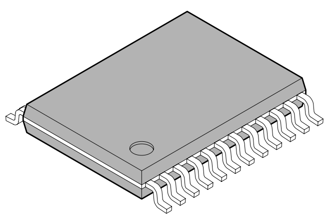
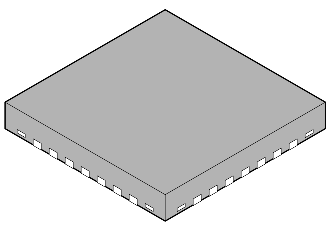
■ PACKAGES

24-pin plastic SSOP



(FPT-24P-M03)

28-pin plastic QFN



(LCC-28P-M11)

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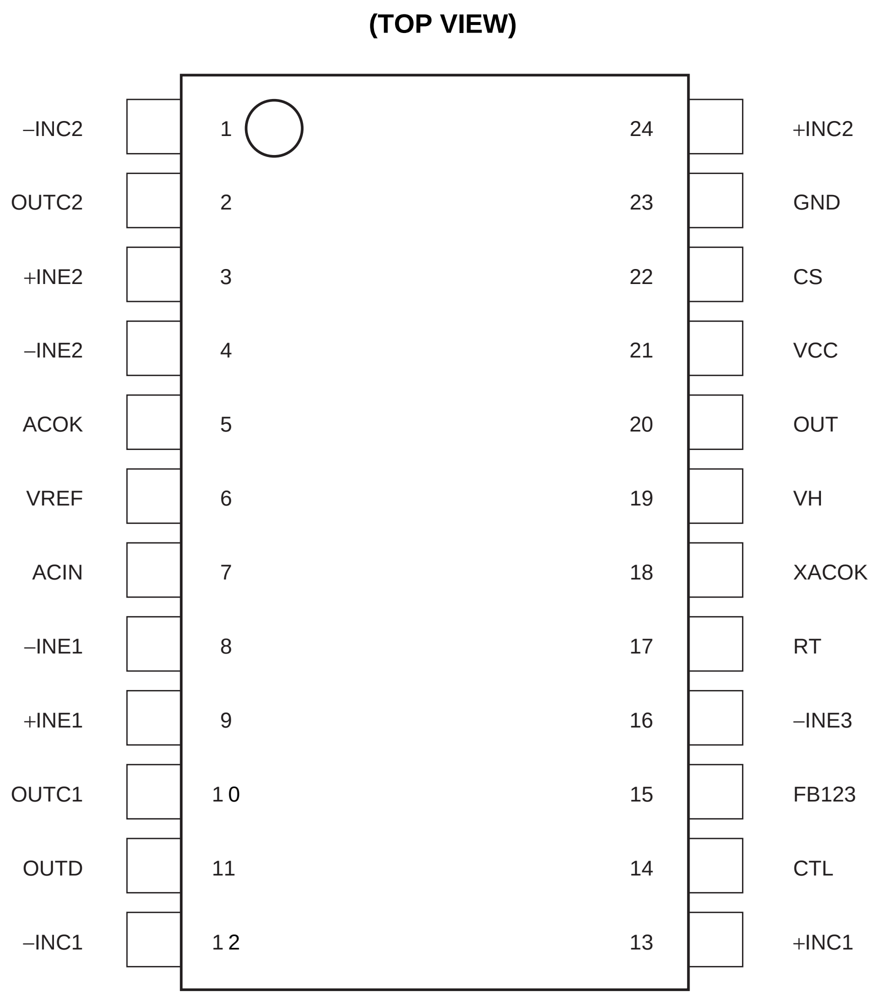
- External output voltage setting resistor : MB39A125
- Built-in output voltage setting resistor : MB39A126
- Built-in charge stop function at low VCC
- Output voltage setting accuracy : ± 0.74% (Ta = –10 °C to +85 °C) : MB39A125
  : 12.6 V/16.8 V ± 0.8% (Ta = –10 °C to +85 °C) : MB39A126
- Built-in high accuracy current detection amplifier (±5%) (At input voltage difference 100 mV) ,
  (±15%) (At input voltage difference 20 mV)
- In IC standby mode (Icc = 0 µA Typ) , make output voltage setting resistor open to prevent inefficient current loss
- Built-in soft-start circuit
- Standby current : 0 µA (Typ)
- Totem-pole type output for Pch MOS FET

■ PIN ASSIGNMENTS

• **MB39A125**



(FPT-24P-M03)

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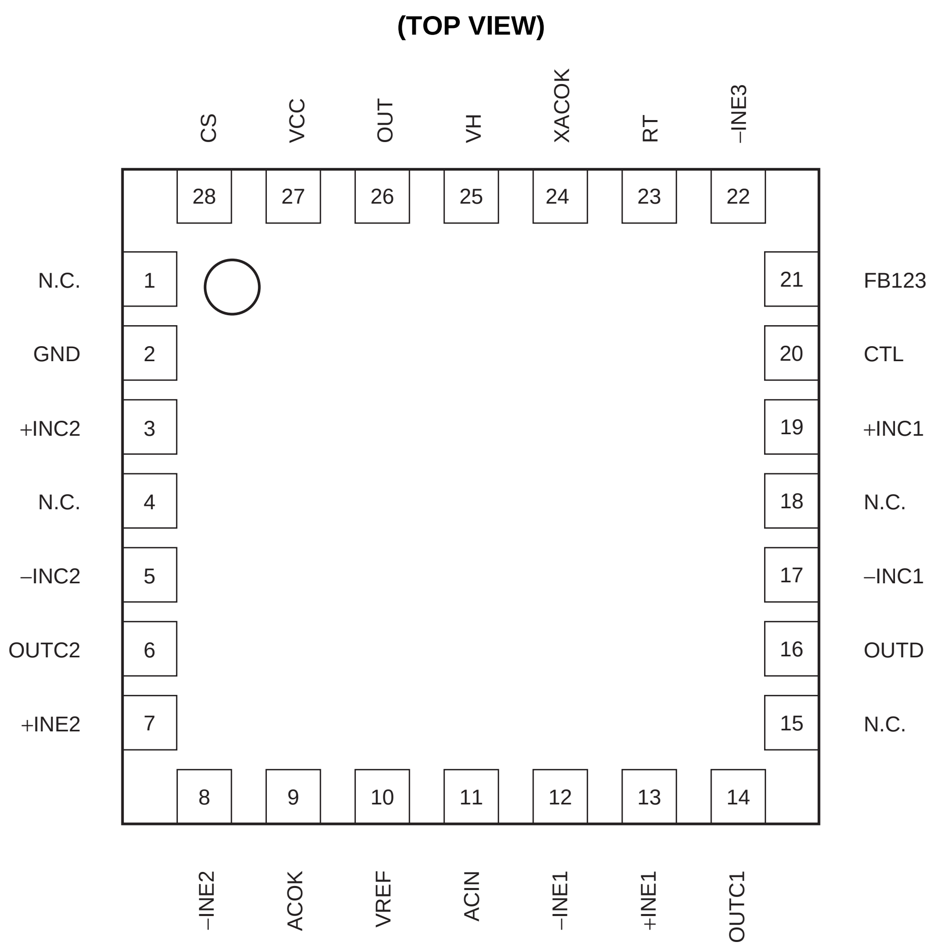
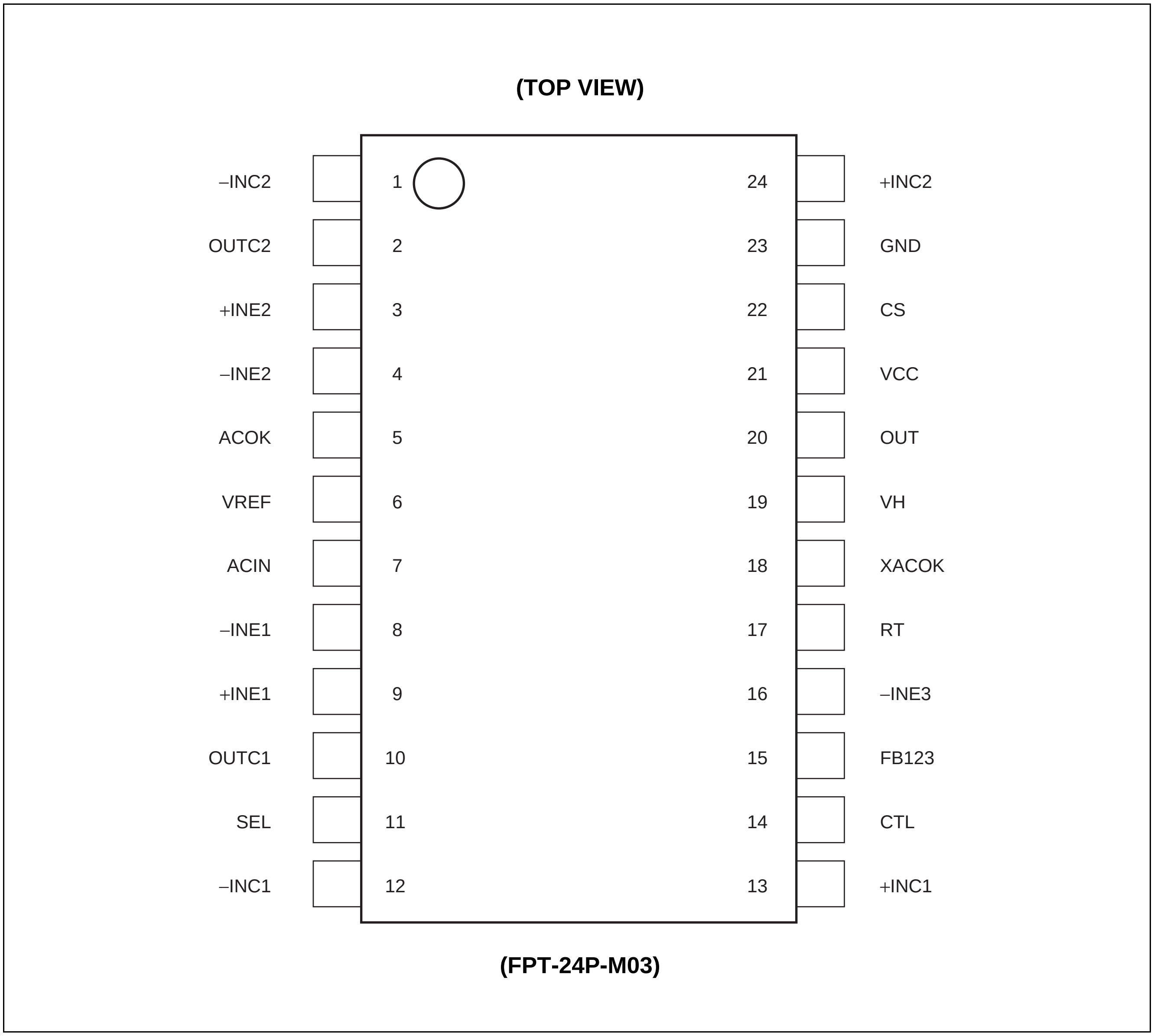


(LCC-28P-M11)

Note : Connect IC's radiation board at bottom side to potential of GND.

• **MB39A126**



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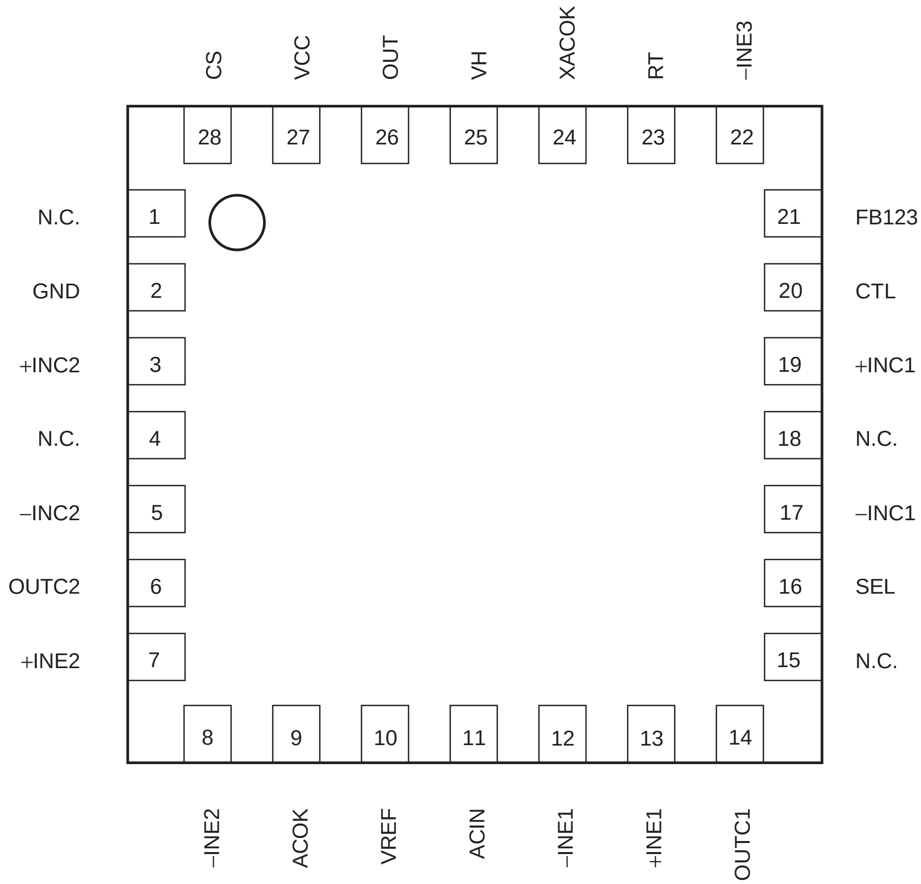
(TOP VIEW)



(LCC-28P-M11)

Note : Connect IC's radiation board at bottom side to potential of GND.

■ PIN DESCRIPTIONS

• MB39A125 : SSOP-24

Pin No.	Pin Name	I/O	Description
1	–INC2	I	Current detection amplifier (Current Amp2) inverted input terminal
2	OUTC2	O	Current detection amplifier (Current Amp2) output terminal
3	+INE2	I	Error amplifier (Error Amp2) non-inverted input terminal
4	–INE2	I	Error amplifier (Error Amp2) inverted input terminal
5	ACOK	O	AC adapter voltage detection block (AC Comp.) output terminal ACOK = L when ACIN = H, ACOK = Hi-Z when ACIN = L, ACOK = Hi-Z when CTL = L
6	VREF	O	Reference voltage output terminal
7	ACIN	I	AC adapter voltage detection block (AC Comp.) input terminal
8	–INE1	I	Error amplifier (Error Amp1) inverted input terminal
9	+INE1	I	Error amplifier (Error Amp1) non-inverted input terminal
10	OUTC1	O	Current detection amplifier (Current Amp1) output terminal
11	OUTD	O	When IC is standby mode, this terminal is set to “Hi-Z” to prevent loss of inefficient current through the output voltage setting resistor. Set CTL terminal to “H” level to output “L” level.
12	–INC1	I	Current detection amplifier (Current Amp1) inverted input terminal
13	+INC1	I	Current detection amplifier (Current Amp1) non-inverted input terminal
14	CTL	I	Power supply control terminal Setting the CTL terminal at “L” level places the IC in the standby mode.
15	FB123	O	Error amplifier (Error Amp1, 2, 3) output terminal
16	–INE3	I	Error amplifier (Error Amp3) inverted input terminal
17	RT	—	Triangular wave oscillation frequency setting resistor connection terminal
18	XACOK	O	AC adapter voltage detection block (AC Comp.) output terminal XACOK = Hi-Z when ACIN = H, XACOK = L when ACIN = L, XACOK = Hi-Z when CTL = L
19	VH	O	Power supply terminal for FET drive circuit (VH = VCC – 6 V)
20	OUT	O	External FET gate drive terminal
21	VCC	—	Power supply terminal for reference voltage, control circuit, and output circuit
22	CS	—	Soft-start setting capacitor connection terminal
23	GND	—	Ground terminal
24	+INC2	I	Current detection amplifier (Current Amp2) non-inverted input terminal

• **MB39A125 : QFN-28**

Pin No.	Pin Name	I/O	Description
1	N.C.	—	No connection
2	GND	—	Ground terminal
3	+INC2	I	Current detection amplifier (Current Amp2) non-inverted input terminal
4	N.C.	—	No connection
5	–INC2	I	Current detection amplifier (Current Amp2) inverted input terminal
6	OUTC2	O	Current detection amplifier (Current Amp2) output terminal
7	+INE2	I	Error amplifier (Error Amp2) non-inverted input terminal
8	–INE2	I	Error amplifier (Error Amp2) inverted input terminal
9	ACOK	O	AC adapter voltage detection block (AC Comp.) output terminal ACOK = L when ACIN = H, ACOK = Hi-Z when ACIN = L, ACOK = Hi-Z when CTL = L
10	VREF	O	Reference voltage output terminal
11	ACIN	I	AC adapter voltage detection block (AC Comp.) input terminal
12	–INE1	I	Error amplifier (Error Amp1) inverted input terminal
13	+INE1	I	Error amplifier (Error Amp1) non-inverted input terminal
14	OUTC1	O	Current detection amplifier (Current Amp1) output terminal
15	N.C.	—	No connection
16	OUTD	O	When IC is standby mode, this terminal is set to “Hi-Z” to prevent loss of inefficient current through the output voltage setting resistor. Set CTL terminal to “H” level to output “L” level.
17	–INC1	I	Current detection amplifier (Current Amp1) inverted input terminal
18	N.C.	—	No connection
19	+INC1	I	Current detection amplifier (Current Amp1) non-inverted input terminal
20	CTL	I	Power supply control terminal Setting the CTL terminal at “L” level places the IC in the standby mode.
21	FB123	O	Error amplifier (Error Amp1, 2, 3) output terminal
22	–INE3	I	Error amplifier (Error Amp3) inverted input terminal
23	RT	—	Triangular wave oscillation frequency setting resistor connection terminal
24	XACOK	O	AC adapter voltage detection block (AC Comp.) output terminal XACOK = Hi-Z when ACIN = H, XACOK = L when ACIN = L, XACOK = Hi-Z when CTL = L
25	VH	O	Power supply terminal for FET drive circuit (VH = VCC - 6 V)
26	OUT	O	External FET gate drive terminal
27	VCC	—	Power supply terminal for reference voltage, control circuit, and output circuit
28	CS	—	Soft-start setting capacitor connection terminal

• **MB39A126 : SSOP-24**

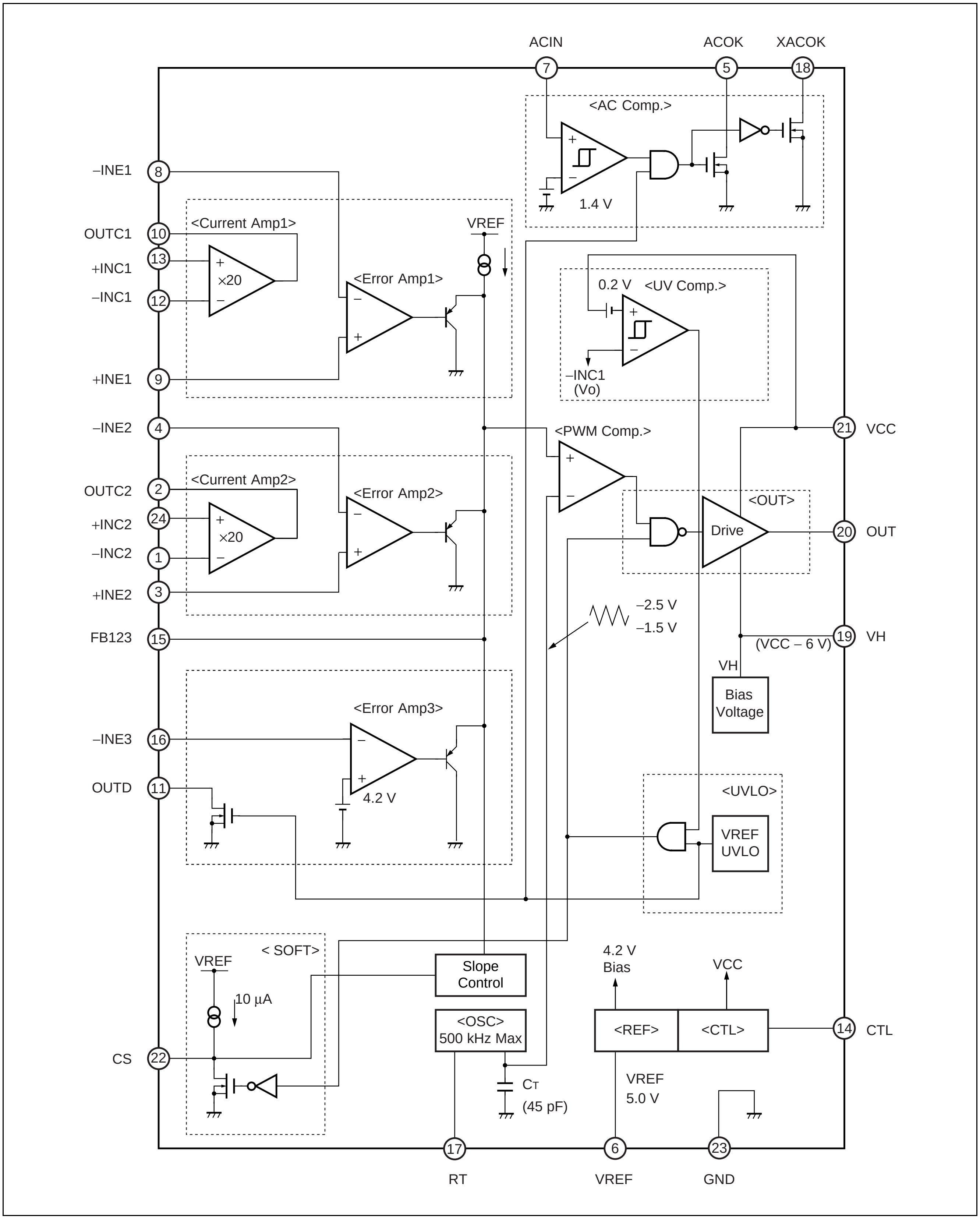
Pin No.	Pin Name	I/O	Description
1	–INC2	I	Current detection amplifier (Current Amp2) inverted input terminal
2	OUTC2	O	Current detection amplifier (Current Amp2) output terminal
3	+INE2	I	Error amplifier (Error Amp2) non-inverted input terminal
4	–INE2	I	Error amplifier (Error Amp2) inverted input terminal
5	ACOK	O	AC adapter voltage detection block (AC Comp.) output terminal ACOK = L when ACIN = H, ACOK = Hi-Z when ACIN = L, ACOK = Hi-Z when CTL = L
6	VREF	O	Reference voltage output terminal
7	ACIN	I	AC adapter voltage detection block (AC Comp.) input terminal
8	–INE1	I	Error amplifier (Error Amp1) inverted input terminal
9	+INE1	I	Error amplifier (Error Amp1) non-inverted input terminal
10	OUTC1	O	Current detection amplifier (Current Amp1) output terminal
11	SEL	I	Charge voltage setting switch terminal (3cells or 4cells) SEL terminal "H" level : Charge voltage setting 16.8 V (4cells) SEL terminal "L" level : Charge voltage setting 12.6 V (3cells)
12	–INC1	I	Current detection amplifier (Current Amp1) inverted input terminal
13	+INC1	I	Current detection amplifier (Current Amp1) non-inverted input terminal
14	CTL	I	Power supply control terminal Setting the CTL terminal at "L" level places the IC in the standby mode.
15	FB123	O	Error amplifier (Error Amp1, 2, 3) output terminal
16	–INE3	I	Error amplifier (Error Amp3) inverted input terminal
17	RT	—	Triangular wave oscillation frequency setting resistor connection terminal
18	XACOK	O	AC adapter voltage detection block (AC Comp.) output terminal XACOK = Hi-Z when ACIN = H, XACOK = L when ACIN = L, XACOK = Hi-Z when CTL = L
19	VH	O	Power supply terminal for FET drive circuit (VH = VCC - 6 V)
20	OUT	O	External FET gate drive terminal
21	VCC	—	Power supply terminal for reference voltage, control circuit, and output circuit
22	CS	—	Soft-start setting capacitor connection terminal
23	GND	—	Ground terminal
24	+INC2	I	Current detection amplifier (Current Amp2) non-inverted input terminal

• **MB39A126 : QFN-28**

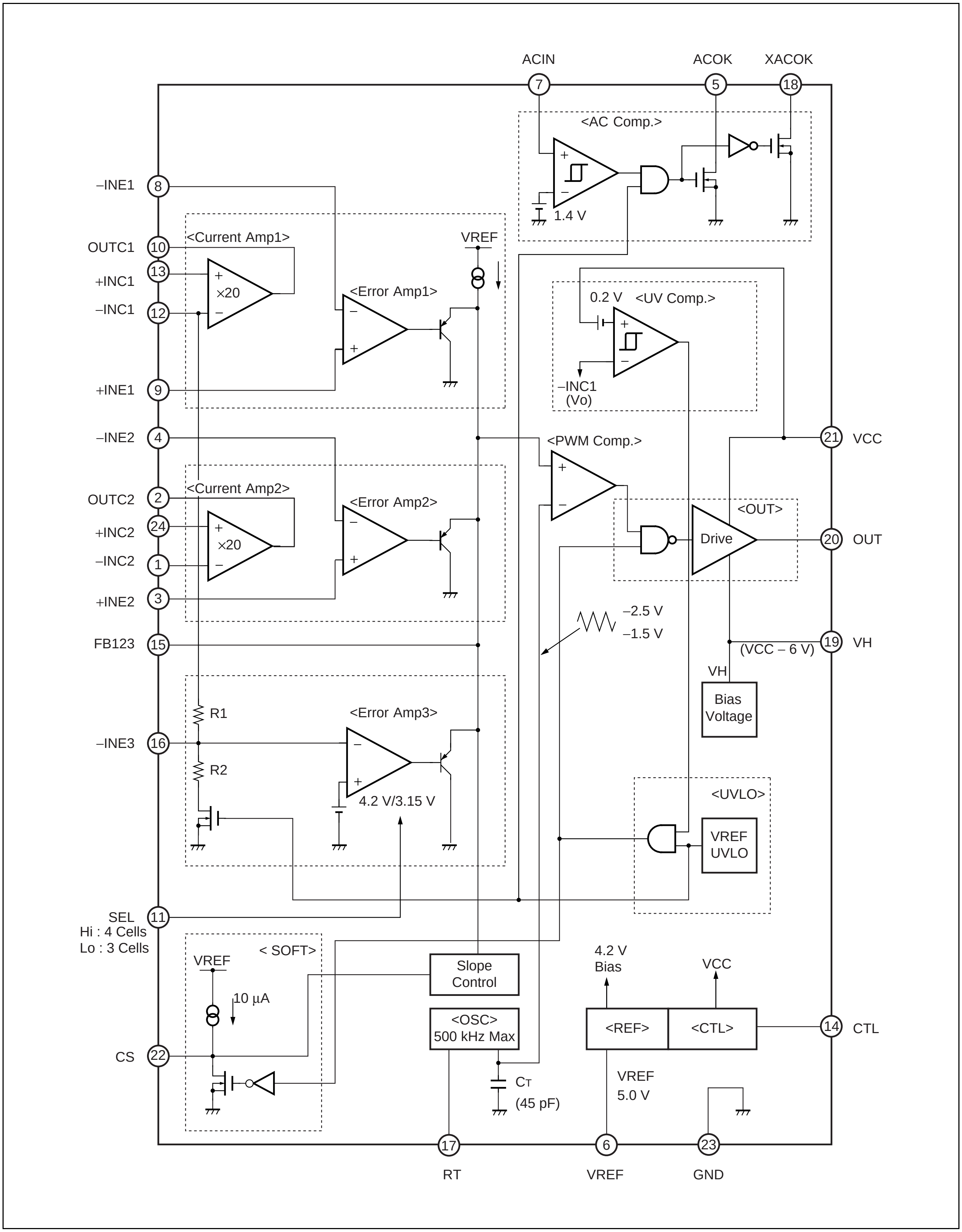
Pin No.	Pin Name	I/O	Description
1	N.C.	—	No connection
2	GND	—	Ground terminal
3	+INC2	I	Current detection amplifier (Current Amp2) non-inverted input terminal
4	N.C.	—	No connection
5	–INC2	I	Current detection amplifier (Current Amp2) inverted input terminal
6	OUTC2	O	Current detection amplifier (Current Amp2) output terminal
7	+INE2	I	Error amplifier (Error Amp2) non-inverted input terminal
8	–INE2	I	Error amplifier (Error Amp2) inverted input terminal
9	ACOK	O	AC adapter voltage detection block (AC Comp.) output terminal ACOK = L when ACIN = H, ACOK = Hi-Z when ACIN = L, ACOK = Hi-Z when CTL = L
10	VREF	O	Reference voltage output terminal
11	ACIN	I	AC adapter voltage detection block (AC Comp.) input terminal
12	–INE1	I	Error amplifier (Error Amp1) inverted input terminal
13	+INE1	I	Error amplifier (Error Amp1) non-inverted input terminal
14	OUTC1	O	Current detection amplifier (Current Amp1) output terminal
15	N.C.	—	No connection
16	SEL	I	Charge voltage setting switch terminal (3cells or 4cells) . SEL terminal “H” level : Charge voltage setting 16.8 V (4cells) SEL terminal “L” level : Charge voltage setting 12.6 V (3cells)
17	–INC1	I	Current detection amplifier (Current Amp1) inverted input terminal
18	N.C.	—	No connection
19	+INC1	I	Current detection amplifier (Current Amp1) non-inverted input terminal
20	CTL	I	Power supply control terminal Setting the CTL terminal at “L” level places the IC in the standby mode.
21	FB123	O	Error amplifier (Error Amp1, 2, 3) output terminal
22	–INE3	I	Error amplifier (Error Amp3) inverted input terminal
23	RT	—	Triangular wave oscillation frequency setting resistor connection terminal
24	XACOK	O	AC adapter voltage detection block (AC Comp.) output terminal XACOK = Hi-Z when ACIN = H, XACOK = L when ACIN = L, XACOK = Hi-Z when CTL = L
25	VH	O	Power supply terminal for FET drive circuit (VH = VCC - 6 V)
26	OUT	O	External FET gate drive terminal
27	VCC	—	Power supply terminal for reference voltage, control circuit, and output circuit
28	CS	—	Soft-start setting capacitor connection terminal

■ BLOCK DIAGRAMS

• MB39A125



• MB39A126


ACIN
ACOK
XACOK
<AC Comp.>
1.4 V
–INE1
OUTC1
+INC1
–INC1
<Current Amp1>
×20
VREF
<Error Amp1>
+INE1
0.2 V
<UV Comp.>
–INC1
(Vo)
–INE2
OUTC2
+INC2
–INC2
+INE2
<Current Amp2>
×20
<Error Amp2>
<PWM Comp.>
<OUT>
Drive
VCC
OUT
–2.5 V
–1.5 V
FB123
(VCC – 6 V)
VH
VH
Bias
Voltage
R1
<Error Amp3>
–INE3
R2
4.2 V/3.15 V
<UVLO>
VREF
UVLO
SEL
Hi : 4 Cells
Lo : 3 Cells
< SOFT>
VREF
10 µA
CS
Slope
Control
<OSC>
500 kHz Max
CT
(45 pF)
4.2 V
Bias
VCC
<REF>
<CTL>
CTL
VREF
5.0 V
RT
VREF
GND

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	VCC terminal	—	28	V
Output current	I_{OUT}	—	—	60	mA
Peak output current	I_{OUT}	Duty ≤ 5% (t = 1 / fosc × Duty)	—	700	mA
Power dissipation	P_D	Ta ≤ +25 °C (SSOP-24)	—	740*1	mW
		Ta ≤ +25 °C (QFN-28)	—	3700*2	mW
Storage temperature	T_{STG}	—	–55	+125	°C

*1 : When mounted on a 10cm square epoxy double-sided.

*2 : The packages are mounted on the dual-sided epoxy board (10 cm × 10 cm) . Connect IC’s radiation board at bottom side to potential of GND.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			MIN	TYP	MAX	
Power supply voltage	V_{CC}	VCC terminal	8	—	25	V
Reference voltage Output current	I_{REF}	—	–1	—	0	mA
VH terminal output current	I_{VH}	—	0	—	30	mA
Input voltage	V_{INE}	+INE, –INE terminal	0	—	5	V
	V_{INC}	+INC, –INC terminal	0	—	V_{CC}	V
CTL terminal input voltage	V_{CTL}	—	0	—	25	V
Output current	I_{OUT}	—	–45	—	+45	mA
Peak output current	I_{OUT}	Duty ≤ 5% (t = 1 / fosc × Duty)	–600	—	+600	mA
ACIN terminal input Voltage	V_{ACIN}	—	0	—	V_{CC}	V
ACOK terminal output voltage	V_{ACOK}	—	0	—	25	V
ACOK terminal output current	I_{ACOK}	—	0	—	1	mA
XACOK terminal output voltage	V_{XACOK}	—	0	—	25	V
XACOK terminal output current	I_{XACOK}	—	0	—	1	mA
OUTD terminal output voltage : MB39A125	V_{OUTD}	—	0	—	17	V
OUTD terminal output current : MB39A125	I_{OUTD}	—	0	—	2	mA
SEL terminal input voltage : MB39A126	V_{SEL}	—	0	—	25	V
Oscillation frequency	f_{OSC}	—	100	300	500	kHz
Timing resistor	R_T	—	27	47	130	kΩ
Soft-start capacitor	C_S	—	—	0.22	1.0	µF
VH terminal capacitor	C_{VH}	—	—	0.1	1.0	µF
Reference voltage output capacitor	C_{REF}	—	—	0.22	1.0	µF
Operating ambient Temperature	Ta	—	–30	+25	+85	°C

Note : The terminal number which has been described in the text is the one of the SSOP-24P package after this.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(VCC = 19 V, VREF = 0 mA, Ta = +25 °C)

Parameter		Sym-bol	Pin No.	Condition	Value			Unit	Remarks
					Min	Typ	Max		
1. Reference voltage block [REF]	Output voltage	V_{REF1}	6	Ta = +25 °C	4.963	5.000	5.037	V	MB39A125
		V_{REF2}	6	Ta = –10 °C to +85 °C	4.95	5.000	5.05	V	MB39A125
		V_{REF1}	6	Ta = +25 °C	4.943	4.980	5.017	V	MB39A126
		V_{REF2}	6	Ta = –10 °C to +85 °C	4.930	4.980	5.030	V	MB39A126
	Input stability	Line	6	VCC = 8 V to 25 V	—	3	10	mV	
	Load stability	Load	6	VREF = 0 mA to –1 mA	—	1	10	mV	
	Output current at short circuit	Ios	6	VREF = 1 V	–50	–25	–12	mA	
2. Under voltage lockout protection circuit block [UVLO]	Threshold voltage	V_{TLH}	6	VREF =	2.6	2.8	3.0	V	
		V_{THL}	6	VREF =	2.4	2.6	2.8	V	
	Hysteresis width	V_H	6	—	—	0.2*	—	V	
3. Soft start block [SOFT]	Charge current	I_{CS}	22	—	–14	–10	–6	µA	
4. Triangular wave oscillator block [OSC]	Oscillation frequency	f_{OSC}	20	RT = 47 kΩ	270	300	330	kHz	
	Frequency temperature stability	Δf/fdt	20	Ta = –30 °C to +85 °C	—	1*	—	%	
5-1. Error amplifier block [Error Amp1, Error Amp2]	Input offset voltage	V_{IO}	3, 4, 8, 9	FB123 = 2 V	—	1	5	mV	
	Input bias current	I_B	3, 4, 8, 9	—	–100	–30	—	nA	
	Common mode input voltage range	V_{CM}	3, 4, 8, 9	—	0	—	5	V	
	Voltage gain	Av	15	DC	—	100*	—	dB	
	Frequency bandwidth	BW	15	AV = 0 dB	—	1.3*	—	MHz	
	Output voltage	V_{FBH}	15	—	4.8	5.0	—	V	
		V_{FBL}	15	—	—	0.8	0.9	V	
	Output source current	I_{SOURCE}	15	FB123 = 2 V	—	–120	–60	µA	
	Output sink current	I_{SINK}	15	FB123 = 2 V	2.0	4.0	—	mA	

* : Standard design value

(Continued)

(VCC = 19 V, VREF = 0 mA, Ta = +25 °C)

Parameter		Symbol	Pin No.	Condition	Value Min	Value Typ	Value Max	Unit	Remarks
5-2. Error amplifier block [Error Amp3]	Input current	I_{INE}	16	–INE3 = 0 V	–100	–30	—	nA	MB39A125
	Voltage gain	Av	15	DC	—	100*	—	dB	
	Frequency bandwidth	BW	15	AV = 0 dB	—	1.3*	—	MHz	
	Output voltage	V_{FBH}	15	—	4.8	5.0	—	V	
		V_{FBL}	15	—	—	0.8	0.9	V	
	Output source current	I_{SOURCE}	15	FB123 = 2 V	—	–120	–60	µA	
	Output sink current	I_{SINK}	15	FB123 = 2 V	2.0	4.0	—	mA	
	Threshold voltage	V_{TH1}	16	FB123 = 2 V, Ta = +25 °C	4.179	4.200	4.220	V	MB39A125
		V_{TH2}	16	FB123 = 2 V, Ta = –10 °C to +85 °C	4.169	4.200	4.231	V	MB39A125
		V_{TH3}	12	SEL = 5 V, FB123 = 2 V, Ta = +25 °C	16.700	16.800	16.900	V	MB39A126
		V_{TH4}	12	SEL = 5 V, FB123 = 2 V, Ta = –10 °C to +85 °C	16.666	16.800	16.934	V	MB39A126
		V_{TH5}	12	SEL = 0 V, FB123 = 2 V, Ta = +25 °C	12.525	12.600	12.675	V	MB39A126
		V_{TH6}	12	SEL = 0 V, FB123 = 2 V, Ta = –10 °C to +85 °C	12.500	12.600	12.700	V	MB39A126
	OUTD terminal output leak current	I_{LEAK}	11	OUTD = 17 V	—	0	1	µA	MB39A125
	OUTD terminal output ON resistance	R_{ON}	11	OUTD = 1 mA	—	35	50	Ω	MB39A125
	Input current	I_{IN}	12	–INC1 = 16.8 V	—	84	150	µA	MB39A126
	Input resistance	R1	12, 16	—	105	150	195	kΩ	MB39A126
		R2	16	—	35	50	65	kΩ	MB39A126

* : Standard design value

(Continued)

(VCC = 19 V, VREF = 0 mA, Ta = +25 °C)

Parameter		Symbol	Pin No.	Condition	Value Min	Value Typ	Value Max	Unit	Remarks
5-2. Error amplifier block [Error Amp3]	SEL input voltage	V_{ON}	11	Error Amp3 reference voltage = 4.2 V (4-cell setting)	2	—	25	V	MB39A126
		V_{OFF}	11	Error Amp3 reference voltage = 3.15 V (3-cell setting)	0	—	0.8	V	MB39A126
	Input current	I_{SELH}	11	SEL = 5 V	—	50	100	µA	MB39A126
		I_{SELL}	11	SEL = 0 V	—	0	1	µA	MB39A126
6. Current Detection Amplifier Block [Current Amp1, Current Amp2]	Input offset voltage	V_{IO}	1, 12, 13, 24	+INC1 = +INC2 = –INC1 = –INC2 = 3 V to VCC	–3	—	+3	mV	
	Input current	I_{+INCH}	13, 24	+INC1 = +INC2 = 3 V to VCC, ΔV_{IN} = –100 mV	—	20	30	µA	
		I_{-INCH}	1, 12	+INC1 = +INC2 = 3 V to VCC, ΔV_{IN} = –100 mV	—	0.1	0.2	µA	MB39A125
			1	+INC1 = +INC2 = 3 V to VCC, ΔV_{IN} = –100 mV	—	0.1	0.2	µA	MB39A126
		I_{+INCL}	13, 24	+INC1 = +INC2 = 0 V, ΔV_{IN} = –100 mV	–180	–120	—	µA	
		I_{-INCL}	1, 12	+INC1 = +INC2 = 0 V, ΔV_{IN} = –100 mV	–195	–130	—	µA	
	Current detection voltage	V_{OUTC1}	2, 10	+INC1 = +INC2 = 3 V to VCC, ΔV_{IN} = –100 mV	1.9	2.0	2.1	V	
		V_{OUTC2}	2, 10	+INC1 = +INC2 = 3 V to VCC, ΔV_{IN} = –20 mV	0.34	0.40	0.46	V	
		V_{OUTC3}	2, 10	+INC1 = +INC2 = 0 V, ΔV_{IN} = –100 mV	1.8	2.0	2.2	V	
		V_{OUTC4}	2, 10	+INC1 = +INC2 = 0 V, ΔV_{IN} = –20 mV	0.2	0.4	0.6	V	
	Common mode input voltage range	V_{CM}	1, 12, 13, 24	—	0	—	V_{CC}	V	
	Voltage gain	Av	2, 10	+INC1 = +INC2 = 3 V to VCC, ΔV_{IN} = –100 mV	19	20	21	V/V	

(Continued)

(VCC = 19 V, VREF = 0 mA, Ta = +25 °C)

Parameter		Symbol	Pin No.	Condition	Value Min	Value Typ	Value Max	Unit	Remarks
6. Current Detection Amplifier Block [Current Amp1, Current Amp2]	Frequency bandwidth	BW	2, 10	AV = 0 dB	—	2*	—	MHz	
	Output voltage	V_{OUTCH}	2, 10	—	4.7	4.9	—	V	
		V_{OUTCL}	2, 10	—	—	20	200	mV	
	Output source current	I_{SOURCE}	2, 10	OUTC1 = OUTC2 = 2 V	—	–2	–1	mA	
	Output sink current	I_{SINK}	2, 10	OUTC1 = OUTC2 = 2 V	150	300	—	µA	
7. PWM Comp. Block [PWM Comp.]	Threshold voltage	V_{TL}	15	Duty cycle = 0%	1.4	1.5	—	V	
		V_{TH}	15	Duty cycle = 100%	—	2.5	2.6	V	
8. Output block [OUT]	Output source current	I_{SOURCE}	20	OUT = 13 V, Duty ≤ 5% (t = 1 / fosc × Duty)	—	–400*	—	mA	
	Output sink current	I_{SINK}	20	OUT = 19 V, Duty ≤ 5% (t = 1 / fosc × Duty)	—	400*	—	mA	
	Output ON resistance	R_{OH}	20	OUT = –45 mA	—	6.5	9.8	Ω	
		R_{OL}	20	OUT = 45 mA	—	5.0	7.5	Ω	
	Rise time	tr1	20	OUT = 3300 pF	—	50*	—	ns	
	Fall time	tf1	20	OUT = 3300 pF	—	50*	—	ns	
9. Low Input Voltage Detection Block [UV Comp.]	Threshold voltage	V_{TLH}	21	VCC = ↑, –INC1 = 16.8 V	17.2	17.4	17.6	V	
		V_{THL}	21	VCC = ↓, –INC1 = 16.8 V	16.8	17.0	17.2	V	
	Hysteresis width	V_H	21	—	—	0.4*	—	V	
10. AC Adapter Voltage Detection Block [AC Comp.]	Threshold voltage	V_{TLH}	7	ACIN = ↑	1.3	1.4	1.5	V	
		V_{THL}	7	ACIN = ↓	1.2	1.3	1.4	V	
	Hysteresis width	V_H	7	—	—	0.1*	—	V	

* : Standard design value

(Continued)

(Continued)

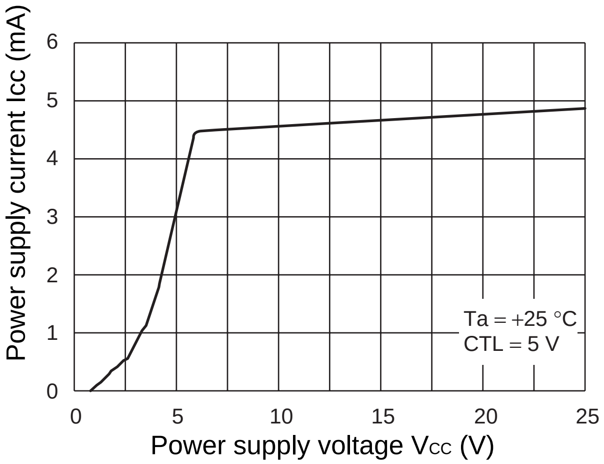
(VCC = 19 V, VREF = 0 mA, Ta = +25 °C)

Parameter		Symbol	Pin No.	Condition	Value			Unit	Remarks
					Min	Typ	Max		
10. AC Adapter Voltage Detection Block [AC Comp.]	ACOK terminal output leak current	I_{LEAK}	5	ACOK = 25 V	—	0	1	µA	
	ACOK terminal output ON resistance	R_{ON}	5	ACOK = 1 mA	—	200	400	Ω	
	XACOK terminal output leak current	I_{LEAK}	18	XACOK = 25 V	—	0	1	µA	
	XACOK terminal output ON resistance	R_{ON}	18	XACOK = 1 mA	—	200	400	Ω	
11. Power Supply Control Block [CTL]	CTL input voltage	V_{ON}	14	IC operation mode	2	—	25	V	
		V_{OFF}	14	IC standby mode	0	—	0.8	V	
	Input current	I_{CTLH}	14	CTL = 5 V	—	100	150	µA	
		I_{CTLL}	14	CTL = 0 V	—	0	1	µA	
12. Bias Voltage Block [VH]	Output Voltage	V_H	19	VCC = 8 V to 25 V, VH = 0 mA to 30 mA	V_{CC} – 6.5	V_{CC} – 6.0	V_{CC} – 5.5	V	
13. General	Standby current	I_{CCS}	21	CTL = 0 V	—	0	10	µA	
	Power supply current	I_{CC}	21	CTL = 5 V	—	5	7.5	mA	

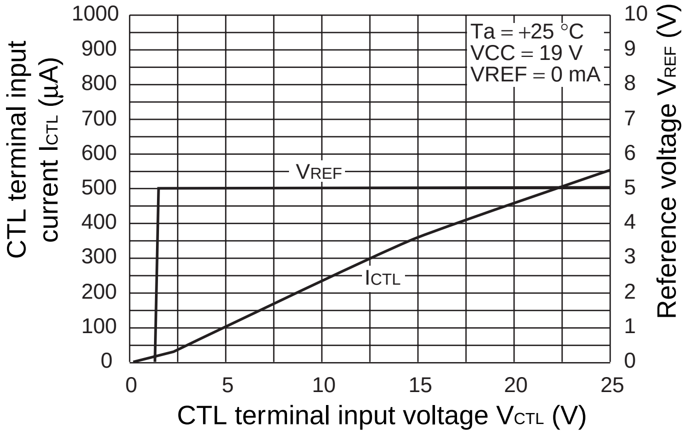
* : Standard design value

■ TYPICAL CHARACTERISTICS

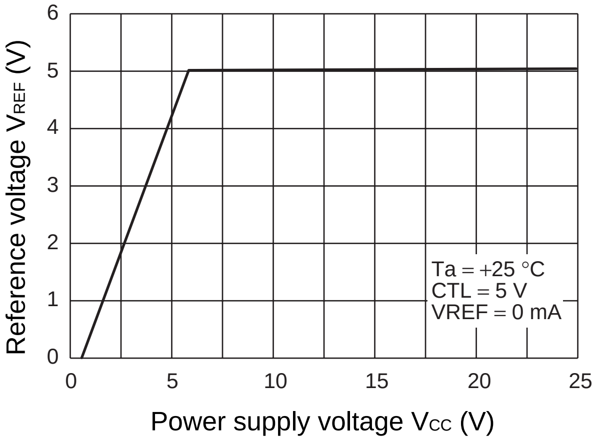
Power Supply Current vs. Power Supply Voltage



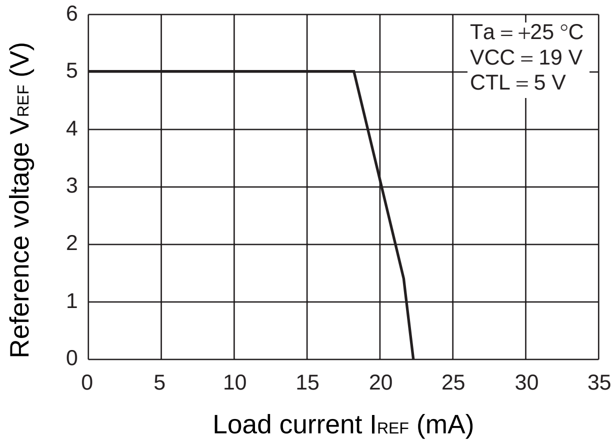
CTL Terminal Input Current, Reference Voltage vs. CTL Terminal Input Voltage



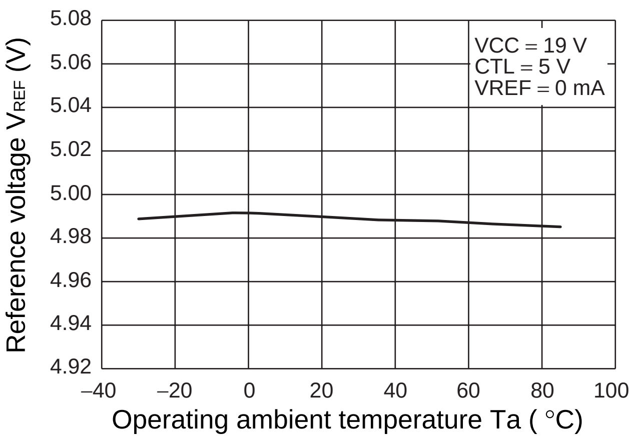
Reference Voltage vs. Power Supply Voltage



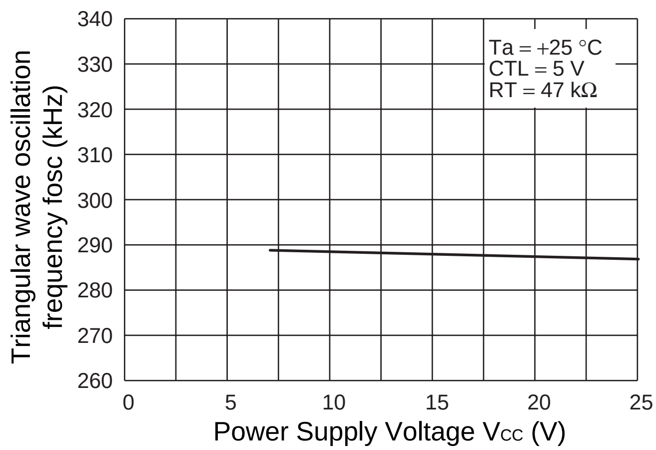
Reference Voltage vs. Load Current



Reference Voltage vs. Operating Ambient Temperature



Triangular Wave Oscillation Frequency vs. Power Supply Voltage



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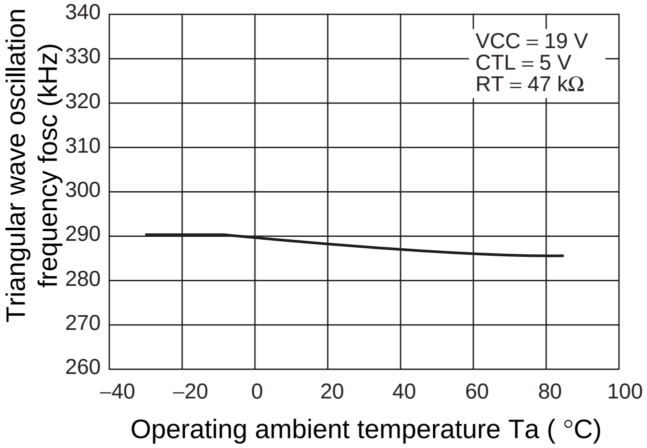
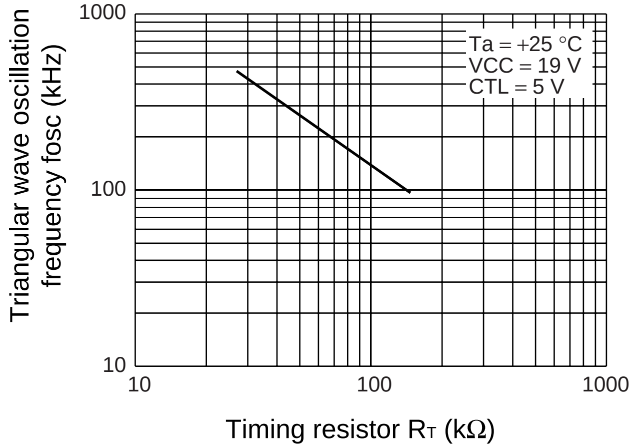
Triangular Wave Oscillation Frequency vs.
Operating Ambient Temperature

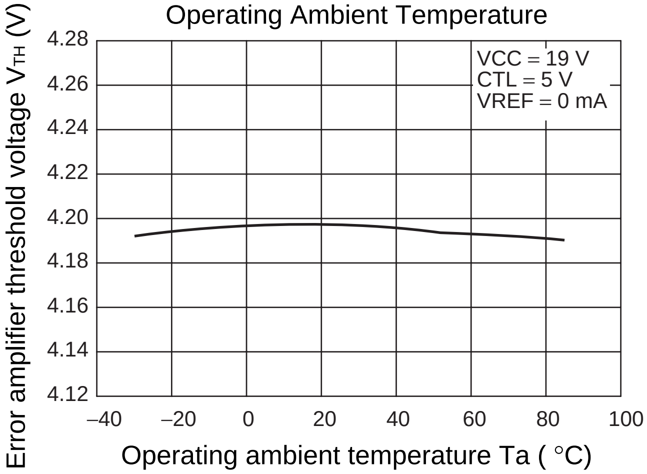


Triangular Wave Oscillation Frequency vs.
Timing Resistor



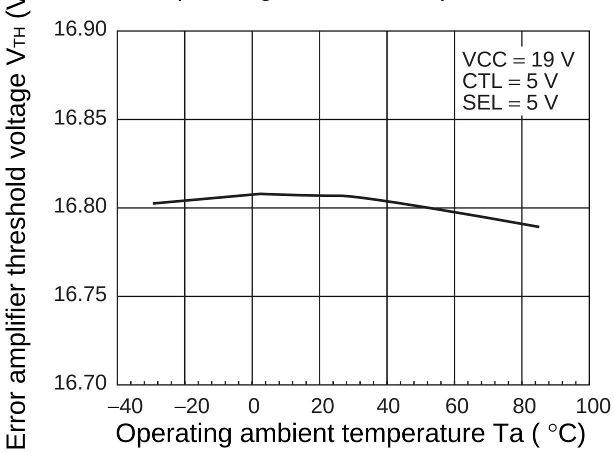
<MB39A125>

Error Amplifier Threshold Voltage vs.
Operating Ambient Temperature

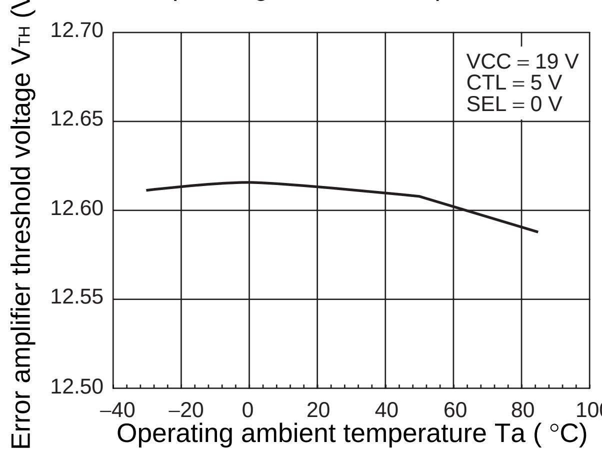


<MB39A126>

Error Amplifier Threshold Voltage vs.
Operating Ambient Temperature



Error Amplifier Threshold Voltage vs.
Operating Ambient Temperature



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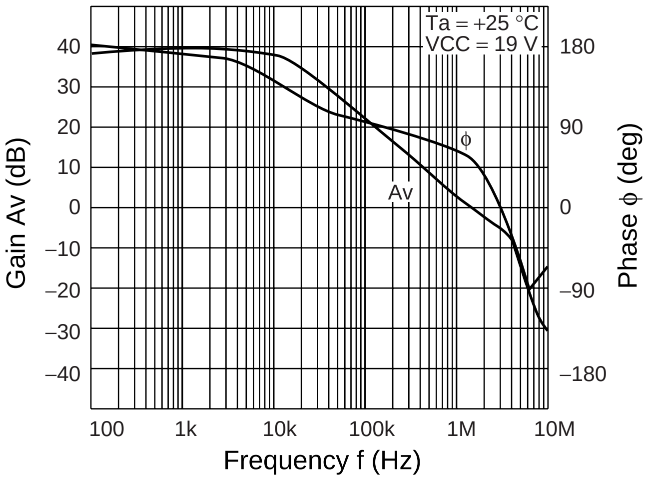
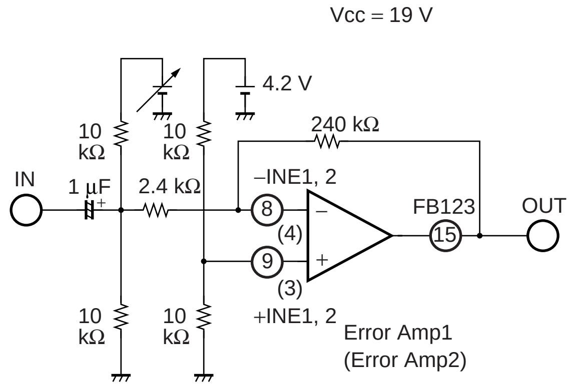
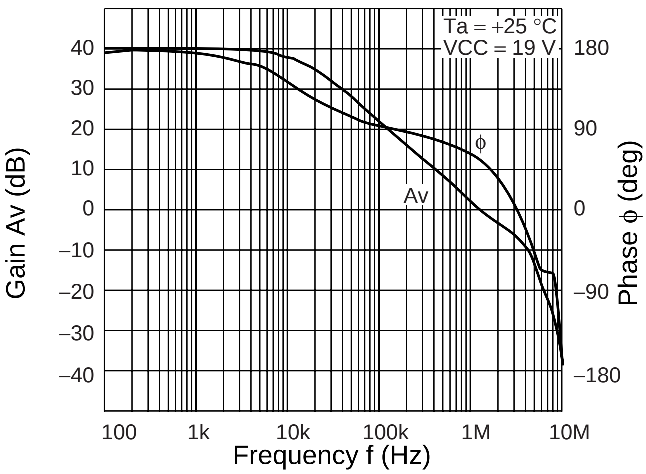
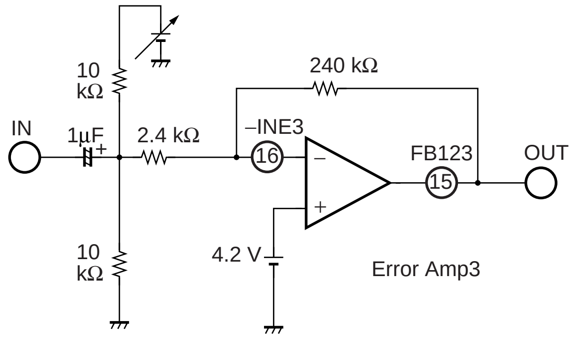
Error Amplifier, Gain, Phase vs. Frequency



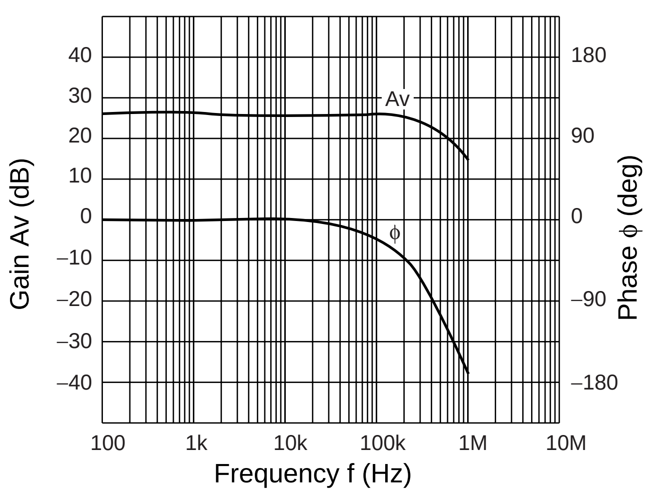


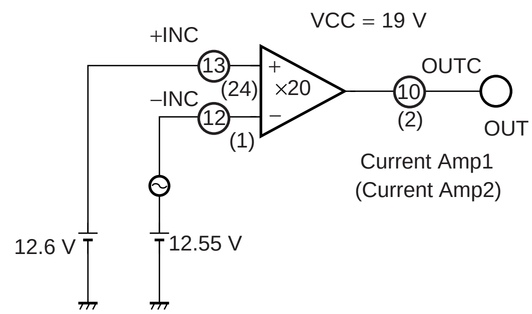
Error Amplifier, Gain, Phase vs. Frequency





Current Detection Amplifier, Gain, Phase vs. Frequency





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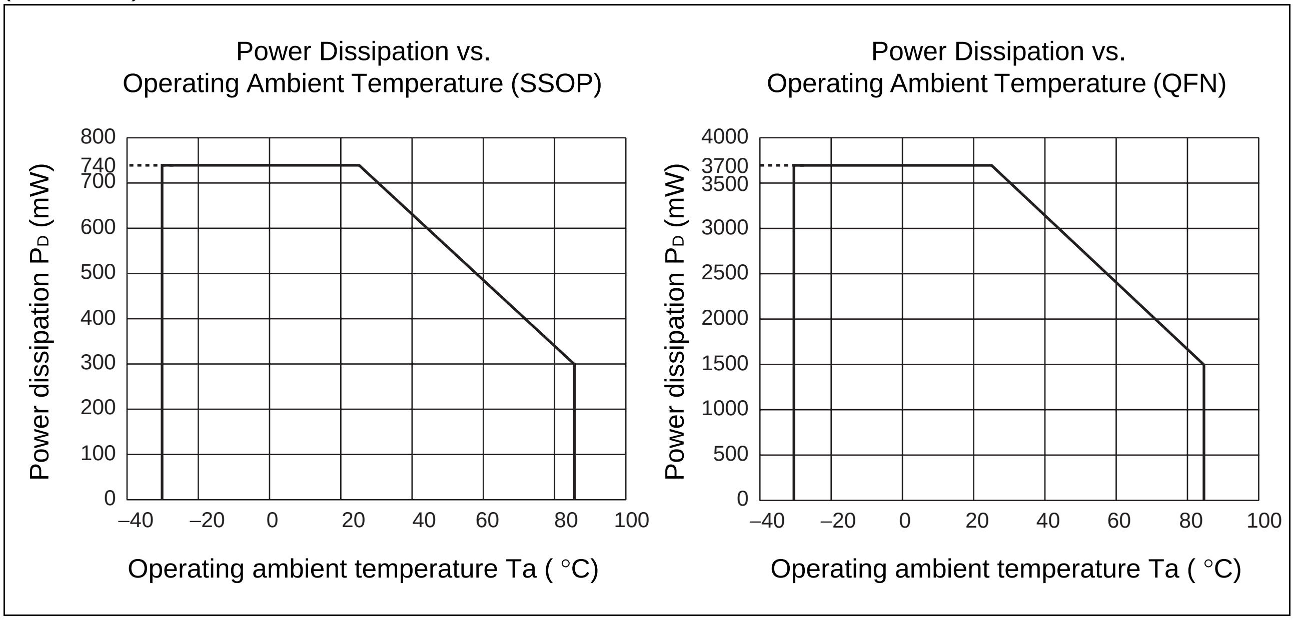

Power Dissipation vs.
Operating Ambient Temperature (SSOP)
Power dissipation PD (mW)
800
740
700
600
500
400
300
200
100
0
–40
–20
0
20
40
60
80
100
Operating ambient temperature Ta (°C)
Power Dissipation vs.
Operating Ambient Temperature (QFN)
Power dissipation PD (mW)
4000
3700
3500
3000
2500
2000
1500
1000
500
0
–40
–20
0
20
40
60
80
100
Operating ambient temperature Ta (°C)

■ FUNCTIONAL DESCRIPTION

1. DC/DC Converter Block

(1) Reference voltage block (REF)

The reference voltage circuit uses the voltage supplied from the VCC terminal (pin 21) to generate a temperature compensated, stable voltage (5.0 V Typ) used as the reference power supply voltage for the IC's internal circuitry.

This block can also be used to obtain a load current to a maximum of 1 mA from the reference voltage VREF terminal (pin 6) .

(2) Triangular wave oscillator block (OSC)

The triangular wave oscillator block has built-in capacitor for frequency setting into and generates the triangular wave oscillation waveform by connecting the frequency setting resistor with the RT terminal (pin 17) .

The triangular wave is input to the PWM comparator circuits on the IC.

(3) Error amplifier block (Error Amp1)

This amplifier detects the output signal from the current detection amplifier (Current Amp1) , compares this to the +INE1 terminal (pin 9) , and outputs a PWM control signal to be used in controlling the charge current.

In addition, an arbitrary loop gain can be set up by connecting a feedback resistor and capacitor between the FB123 terminal (pin 15) and –INE1 terminal (pin 8) , providing stable phase compensation to the system.

(4) Error amplifier block (Error Amp2)

This amplifier detects the output signal from the current detection amplifier (Current Amp2) , compares this to the +INE2 terminal (pin 3) , and outputs a PWM control signal to be used in controlling the charge current.

In addition, an arbitrary loop gain can be set up by connecting a feedback resistor and capacitor between the FB123 terminal (pin 15) and –INE2 terminal (pin 4) , providing stable phase compensation to the system.

(5) Error amplifier block (Error Amp3)

This error amplifier (Error Amp3) detects the output voltage from the DC/DC converter and outputs the PWM control signal. MB39A125 can set the desired level of output voltage from 1 cell to 4 cells by connecting external output voltage setting resistors to the error amplifier inverted input terminal. MB39A126 can set the output voltage for 3 cells or 4 cells by SEL terminal (pin 11) input.

In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the FB123 terminal (pin 15) to the –INE3 terminal (pin 16) , enabling stable phase compensation to the system.

(6) Current detection amplifier block (Current Amp1)

The current detection amplifier (Current Amp1) detects a voltage drop which occurs between both ends of the output sense resistor (RS2) due to the flow of the charge current, using the +INC1 terminal (pin 13) and –INC1 terminal (pin 12) . The signal amplified to 20 times is output to the OUTC1 terminal (pin 10) .

(7) Current detection amplifier block (Current Amp2)

The current detection amplifier (Current Amp2) detects a voltage drop which occurs between both ends of the output sense resistor (RS1) due to the flow of the AC adapter current, using the +INC2 terminal (pin 24) and –INC2 terminal (pin 1) . The signal amplified to 20 times is output to the OUTC2 terminal (pin 2) .

(8) PWM comparator block (PWM Comp.)

The PWM comparator circuit is a voltage-pulse width converter for controlling the output duty of the error amplifiers (Error Amp1 to Error Amp3) depending on their output voltage.

The PWM comparator circuit compares the triangular wave voltage the lowest generated by the triangular wave oscillator to the error amplifier output voltage and turns on the external output transistor, during the interval in which the triangular wave voltage is lower than the error amplifier output voltage.

(9) Output block (OUT)

The output circuit uses a totem-pole configuration capable of driving an external Pch MOS FET.

The output "L" level sets the output amplitude to 6 V (Typ) using the voltage generated by the bias voltage block (VH) .

This results in increasing conversion efficiency and suppressing the withstand voltage of the connected external transistor in a wide range of input voltages.

(10) Power supply control block (CTL)

Setting the CTL terminal (pin 14) low places the IC in the standby mode. (The power supply current is 10µA at maximum in the standby mode.)

CTL function table : MB39A125

CTL	Power	OUTD
L	OFF (Standby)	Hi-Z
H	ON (Active)	L

CTL function table : MB39A126

CTL	Power
L	OFF (Standby)
H	ON (Active)

(11) Bias voltage block (VH)

The bias voltage circuit outputs V_{CC} – 6 V (Typ) as the minimum potential of the output circuit. In the standby mode, this circuit outputs the potential equal to V_{CC}.

2. Protection Functions

(1) Under voltage lockout protection circuit block (UVLO)

The transient state or a momentary decrease in power supply voltage or internal reference voltage (VREF) , which occurs when the power supply (VCC) is turned on, may cause malfunctions in the control IC, resulting in breakdown or deterioration of the system.

To prevent such malfunction, the under voltage lockout protection circuit detects internal reference voltage drop and fixes the OUT terminal (pin 20) to the “H” level. The system restores voltage supply when the internal reference voltage reaches the threshold voltage of the under voltage lockout protection circuit.

Protection circuit (UVLO) operation function table : MB39A125

When UVLO is operating (VREF voltage is lower than UVLO threshold voltage, the logic of the following terminal is fixed.)

OUTD	OUT	CS	ACOK	XACOK
Hi-Z	H	L	H	L

Protection circuit (UVLO) operation function table : MB39A126

When UVLO is operating (VREF voltage is lower than UVLO threshold voltage, the logic of the following terminal is fixed.)

OUT	CS	ACOK	XACOK
H	L	H	L

(2) Low input voltage detection block (UV Comp.)

UV Comp. detects that power supply voltage (VCC) is lower than the battery voltage +0.2 V (Typ) and fixes the OUT terminal (pin 20) to the “H” level.

The system restores voltage supply when the power supply voltage reaches the threshold voltage of the AC adapter detection block.

Protection circuit (UV Comp.) operation function table : MB39A125

When UV Comp. is operating (VCC voltage is lower than UV Comp. threshold voltage, the logic of the following terminal is fixed.)

OUTD	OUT	CS
L	H	L

Protection circuit (UV Comp.) operation function table : MB39A126

When UV Comp. is operating (VCC voltage is lower than UV Comp. threshold voltage, the logic of the following terminal is fixed.)

OUT	CS
H	L

3. Detection Function

(1) AC adapter voltage detection block (AC Comp.)

When ACIN terminal (pin 7) voltage is lower than 1.3 V (Typ) , AC adapter voltage detection block (AC Comp.) outputs "Hi-Z" level to the ACOK terminal (pin 5) and outputs "L" level to the XACOK terminal (pin 18) . When CTL terminal (pin 14) is set to "L" level, ACOK terminal (pin 5) and XACOK terminal (pin 18) are fixed to "Hi-Z" level.

ACIN	ACOK	XACOK
H	L	Hi-Z
L	Hi-Z	L

4. Switch Function : MB39A126

The charge voltage can be set to 16.8 V/12.6 V with the SEL terminal (pin 11) .

SEL function table

SEL	DC/DC output setting voltage
H	16.8 V
L	12.6 V

■ CONSTANT CHARGING VOLTAGE AND CURRENT OPERATION

MB39A125/126 is DC/DC converter with the pulse width modulation (PWM) .

MB39A125 is in the output voltage control loop, the Error Amp3 compares internal voltage reference voltage 4.2 V and DC/DC converter output to output the PWM controlled signal.

MB39A126 is in the output voltage control loop, the Error Amp3 compares internal voltage reference voltage 4.2 V/3.15 V and DC/DC converter output to output the PWM controlled signal.

In the charging current control loop, the voltage drop generated at both ends of charging current sense resistor (RS2) is sensed by +INC1 terminal (pin 13) , –INC1 terminal (pin 12) of Current Amp1, and the signal is output to OUTC1 terminal (pin 10) , which is amplified by 20 times. Error Amp1 compares the OUTC1 terminal (pin 10) voltage, which is the output of Current Amp1, and +INE1 terminal (pin 9) to output the PWM control signal and regulates the charging current.

In the AC adapter current control loop, the voltage drop generated at both ends of AC adapter current sense resistor (RS1) is sensed by +INC2 terminal (pin 24) , –INC2 terminal (pin 1) of Current Amp2, and the signal is output to OUTC2 terminal (pin 2) , which is amplified by 20 times. Error Amp2 compares OUTC2 terminal (pin 2) voltage, which is output of Current Amp2, and +INE2 terminal (pin 3) voltage and outputs PWM controlled signal, and it limits the charging current due to the AC adapter current not to exceed the setting value.

The PWM comparator compares the triangular wave to the smallest terminal voltage among the Error AMP1, Error AMP2 and Error AMP3. And the triangular wave voltage generated by the triangular wave oscillator. When the triangular wave voltage is smaller than the error amplifier output voltage, the main side output transistor is turned on.

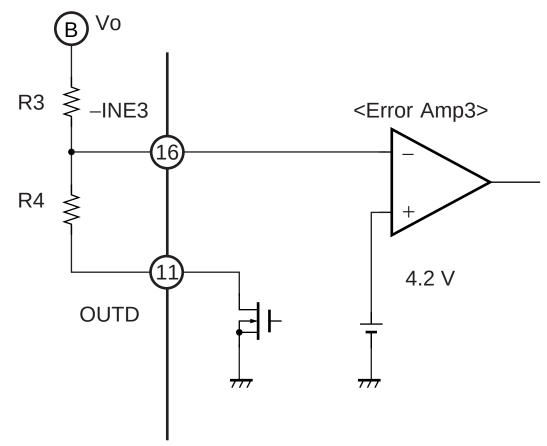
■ SETTING THE CHARGE VOLTAGE

MB39A125

The charging voltage (DC/DC output voltage) can be set by connecting external output voltage setting resistors (R3, R4) to the –INE3 terminal (pin 16) . Be sure to select a resistor value that allows you to ignore the on-resistance (35 Ω, 1 mA) of the internal FET connected to the OUTD terminal (pin 11) .

Battery charging voltage : Vo

Vo (V) = (R3 + R4) / R4 × 4.2 (V)



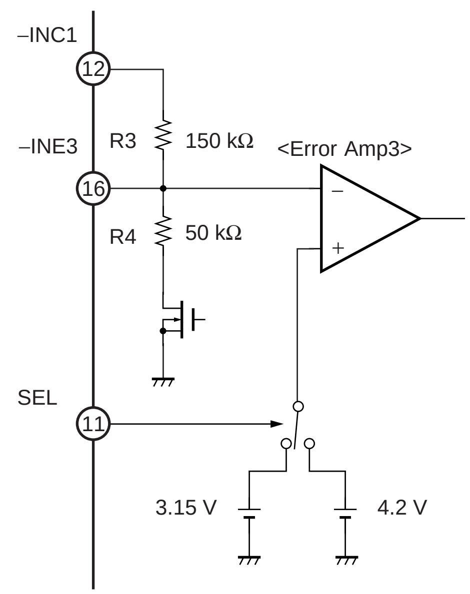
MB39A126

The setting of the charge voltage is switched to 3cells or 4cells by the SEL terminal (pin 11) .

Charge voltage is set to 16.8 V when SEL terminal is “H” level, and charge voltage is set to 12.6 V when SEL terminal is “L” level.

Battery charging voltage : Vo

Vo (V) = (150 kΩ + 50 kΩ) / 50 kΩ × 4.2 (V) = 16.8 (V) (SEL = H)
Vo (V) = (150 kΩ + 50 kΩ) / 50 kΩ × 3.15 (V) = 12.6 (V) (SEL = L)



■ SETTING THE CHARGE CURRENT

The charge current value can be set at the analog voltage value of the +INE1 terminal (pin 9) .

Charge current formula : $Ichg\ (A) = V_{+INE1}\ (V)\ /\ (20 \times R_{S1}\ (\Omega))$
Charge current setting voltage : $V_{+INE1}\ (V) = 20 \times Ichg\ (A) \times R_{S1}\ (\Omega)$

■ SETTING THE INPUT CURRENT

The input limit current value can be set at the analog voltage value of the +INE2 terminal (pin 3) .

Input current formula : $I_{IN}\ (A) = V_{+INE2}\ (V)\ /\ (20 \times R_{S2}\ (\Omega))$
Input current setting voltage : $V_{+INE2}\ (V) = 20 \times I_{IN}\ (A) \times R_{S2}\ (\Omega)$

■ SETTING THE TRIANGULAR WAVE OSCILLATION FREQUENCY

The triangular wave oscillation frequency can be set by the timing resistor (R_T) connected to the RT terminal (pin 17) .

Triangular wave oscillation frequency fosc
$fosc\ (kHz) \fallingdotseq 14100\ /\ R_T\ (k\Omega)$

■ SETTING THE SOFT-START TIME

Soft-start function prevents rush current at start-up of IC when the Soft-start capacitor (Cs) is connected to the CS terminal (pin 22) . This IC charges external soft-start capacitor (Cs) with 10 μA after CTL terminal (pin 14) voltage level becomes high and IC starts (when $V_{CC} \geq$ UVLO threshold voltage) .

Output ON duty depends on PWM comparator, which compares the FB123 terminal (pin 15) voltage with the triangular wave oscillator output voltage.

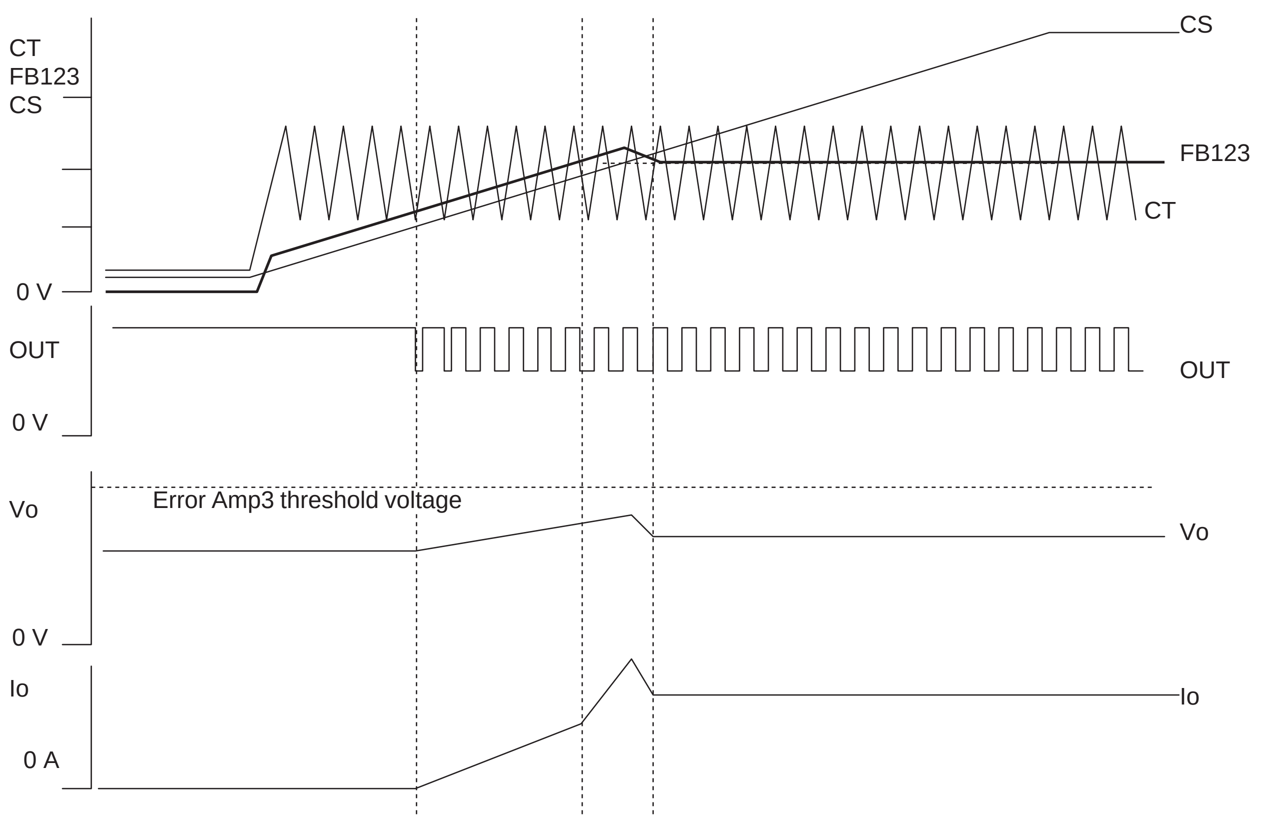
During soft start, FB123 terminal (pin 15) voltage increases with sum voltage of CS terminal and diode voltage. Therefore, the output voltage of the DC/DC converter and current increase can be set by output ON duty in proportion to rise of CS terminal (pin 22) voltage. The ON Duty is affected by the ramp voltage of FB123 terminal (pin 15) until an output voltage of one Error Amp reaches the DC/DC converter loop controlled voltage.

Soft-start time is obtained from the following formula :

Soft-start time : ts (time to output on duty 80 %)

ts (s) $\fallingdotseq 0.13 \times$ Cs (μF)

• **Soft-start timing chart**



■ TRANSIENT RESPONSE AT LOAD-STEP

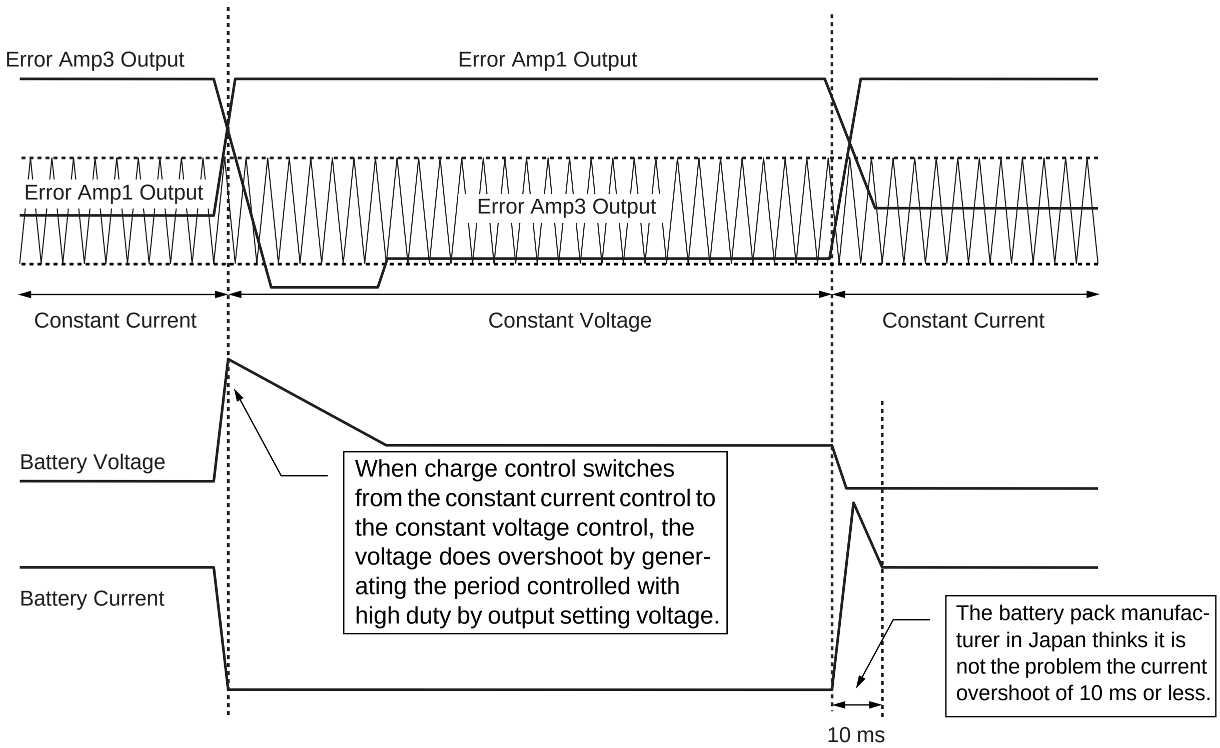
The constant voltage control loop and the constant current control loop are independent. With the load-step, these two control loops change.

The battery voltage and current overshoot are generated by the delay time of the control loop when the mode changes. The delay time is determined by phase compensation constant. When the battery is removed if the charge control is switched from the constant current control to the constant voltage control, and the charging voltage does overshoot by generating the period controlled with high duty by output setting voltage. The excessive voltage is not applied to the battery because the battery is not connected.

When the battery is connected if the charge control is switched from the constant voltage control to the constant current control, and the charging current does overshoot by generating the period controlled with high duty by charge current setting.

The battery pack manufacturer in Japan thinks it is not the problem the current overshoot of 10 ms or less.

- **Timing chart at load-step**



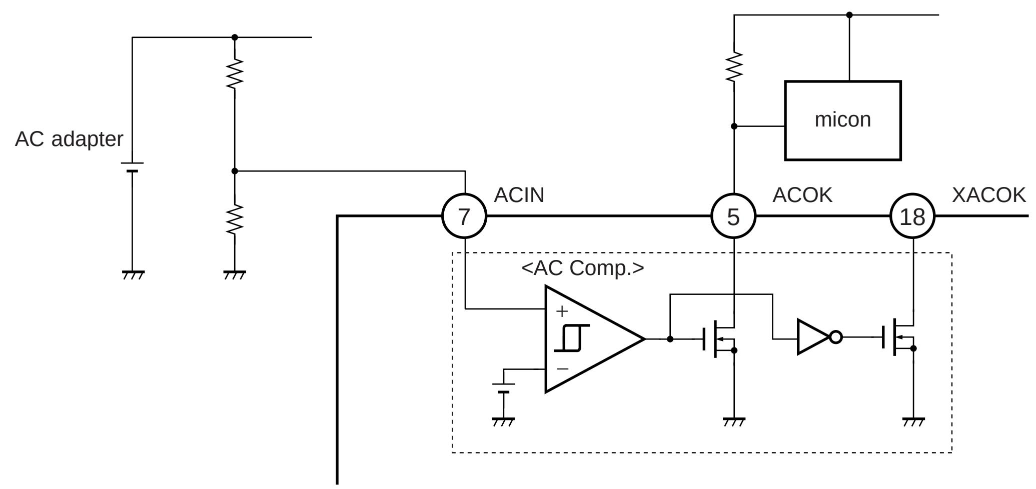
■ AC ADAPTER DETECTION FUNCTION

When ACIN terminal (pin 7) voltage is lower than 1.3 V (Typ) , AC adapter voltage detection block (AC Comp.) outputs “Hi-Z” level to the ACOK terminal (pin 5) and outputs “L” level to the XACOK terminal (pin 18) . When CTL terminal (pin 14) is set to “L” level, ACOK terminal (pin 5) and XACOK terminal (pin 18) are fixed to “Hi-Z” level.

(1) AC adapter presence

If you connect as shown in the figure below the presence of AC adapter can be easily detected because the signal is output from the ACOK terminal (pin 5) to microcomputer etc. In this case, if the CTL terminal is set to “L” level, IC becomes the standby state (I_{CC} = 0 µA Typ).

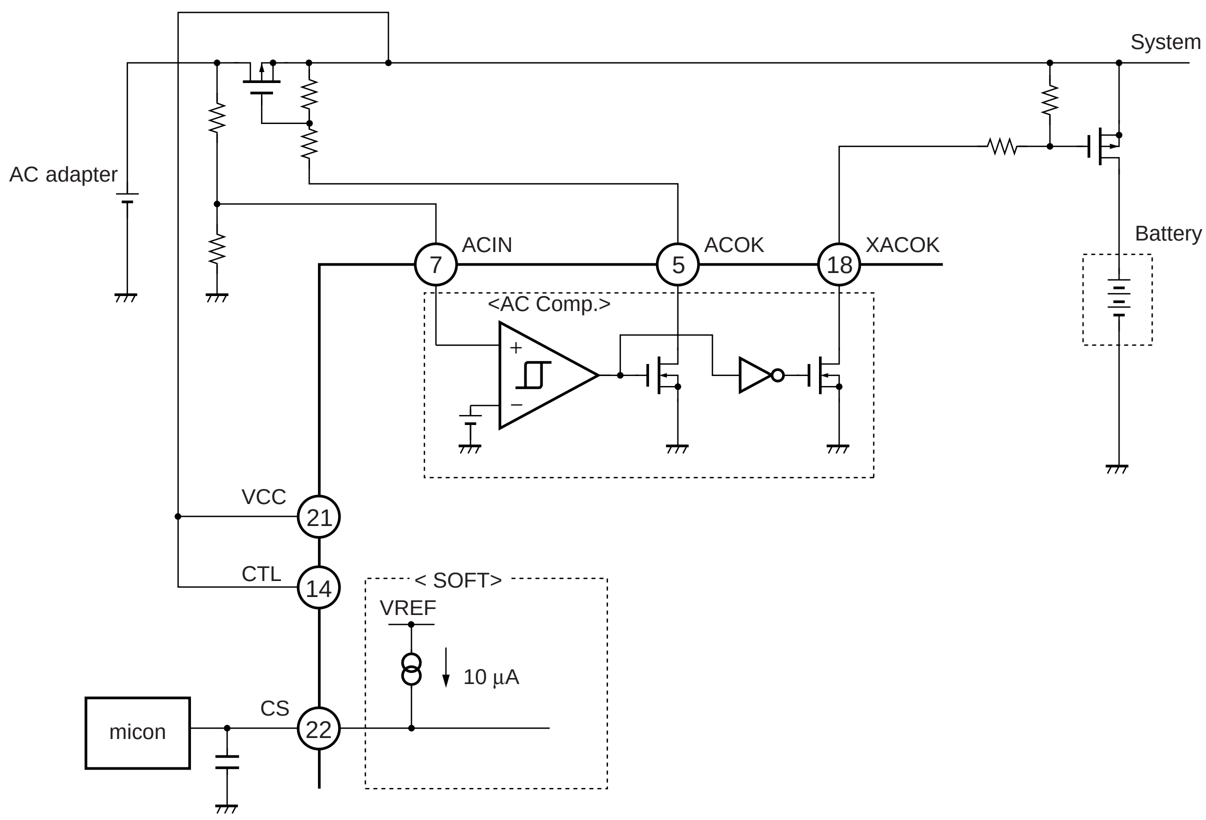
• **Connection example of detecting AC adapter presence**



(2) Automatic changing system power supply between AC adapter and battery

The AC adapter voltage is detected and external switch at input side and battery side can be changed automatically with the connection as follows. Connect CTL terminal (pin 14) to VCC terminal (pin 21) for this function. OFF duty cycle becomes 100% when CS terminal (pin 22) voltage is made to be 0 V, if it is needed after full charge.

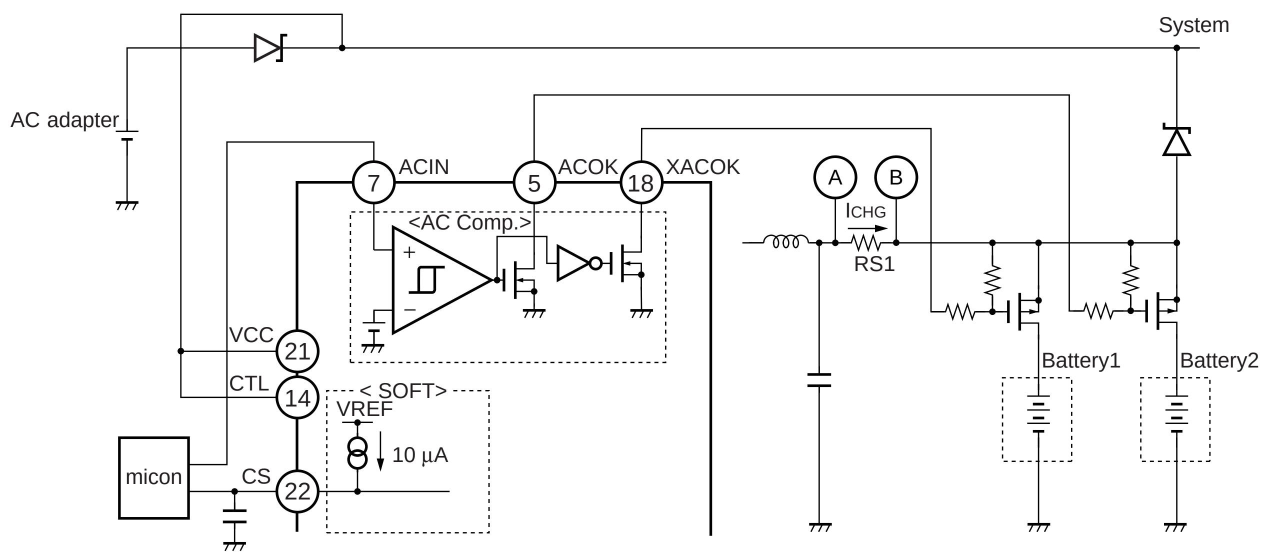
- **Connection example of automatic changing system power supply between AC adapter and battery**



(3) Battery selector function

When control signal from microcomputer etc. is input to ACIN terminal (pin 7) as shown in the following diagram, ACOK terminal (pin 5) output voltage and XACOK terminal (pin 18) output voltage are controlled to select one of the two batteries for charge. Connect CTL terminal (pin 14) to VCC terminal (pin 21) for this function. OFF duty cycle becomes 100% when CS terminal (pin 22) voltage is made to be 0 V, if it is needed after full charge.

- **Connection example of battery selector function**

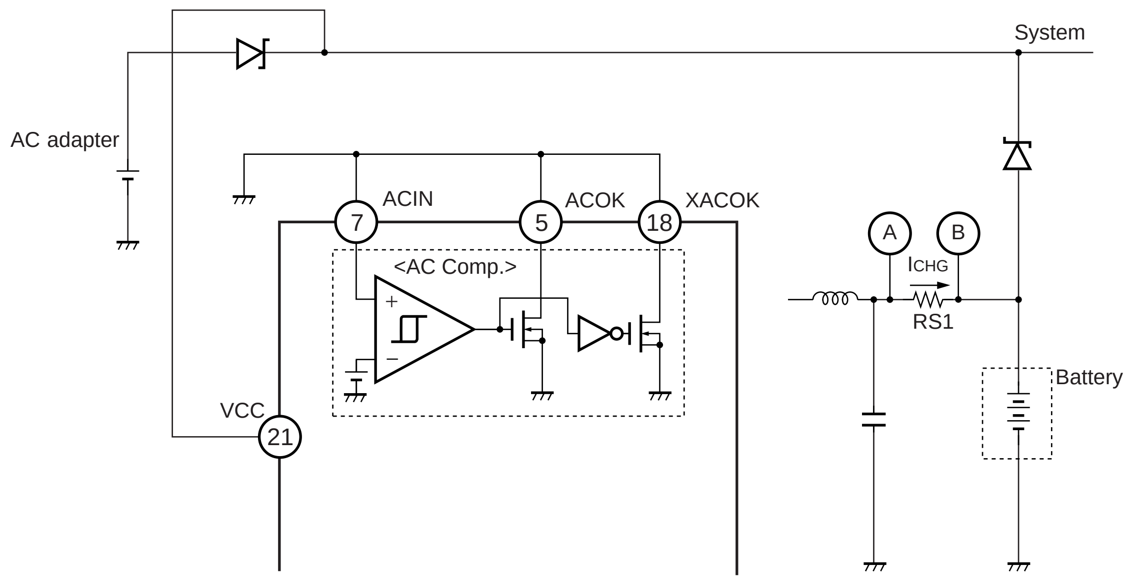


(4) When AC Comp. is not used

When AC Comp. (ACIN (pin 7) , ACOK (pin 5) , and XACOK (pin 18) terminals) is not used as follows, connect the ACIN (pin 7) , ACOK (pin 5) , and XACOK (pin 18) terminals to GND terminal (pin 23) .

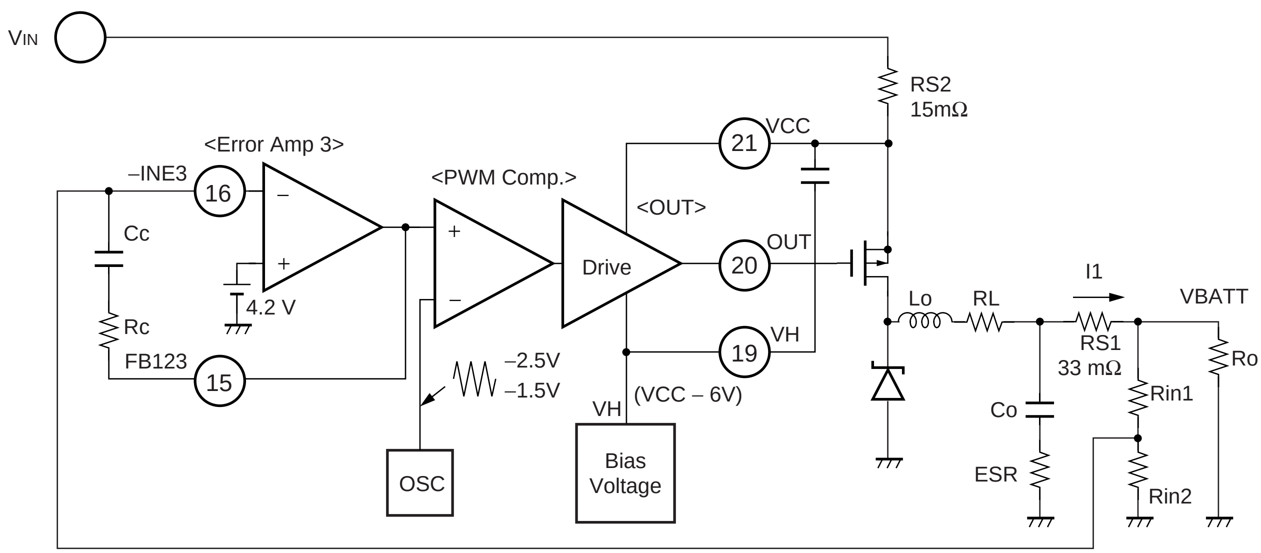
And connect VCC terminal (pin 21) to system, as follows, to avoid the reverse current from the battery to the VCC terminal (pin 21) .

- **Connection example when AC Comp. is not used**



■ PHASE COMPENSATION

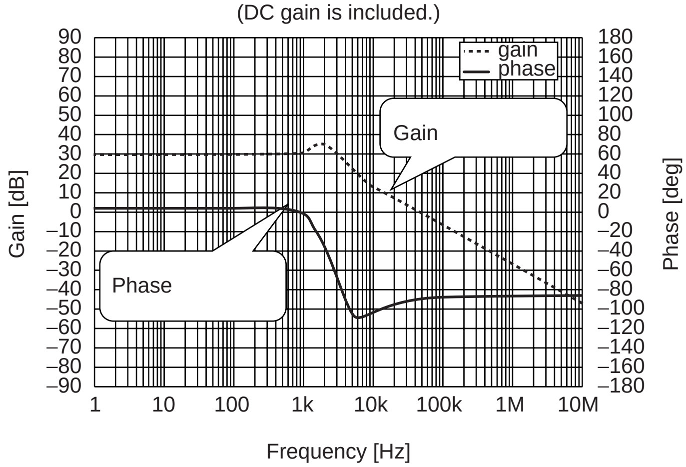
• **Example Circuit**



Lo : Inductance
RL : Equivalent series resistance of inductance
Co : Capacity of condenser
ESR : Equivalent series resistance of condenser
Ro : Load resistance

• Frequency Characteristics of LC filter

Frequency characteristic of power output LC filter
(DC gain is included.)

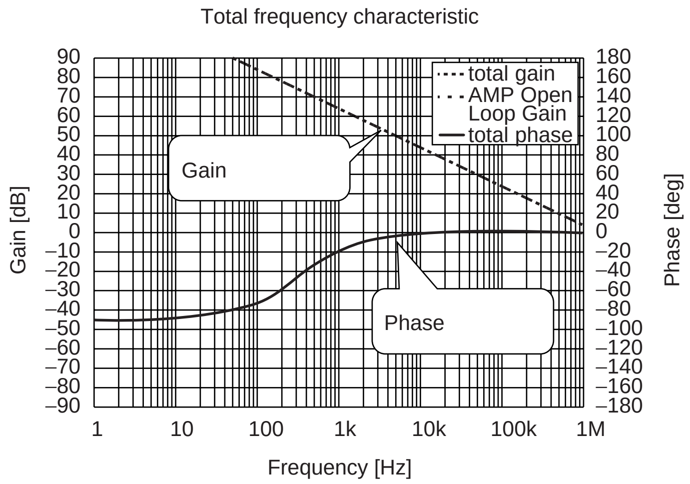


Cut-off frequency

$$f1\ (Hz) = \frac{1}{2\pi \sqrt{Lo \times Co \times \dfrac{(Ro + ESR)}{(Ro + RL)}}}$$

Lo = 15 µH
Co = 14.1 µF
Ro = 4.2 Ω
RL = 30 mΩ
ESR = 100 mΩ

• Frequency Characteristics of Error Amp

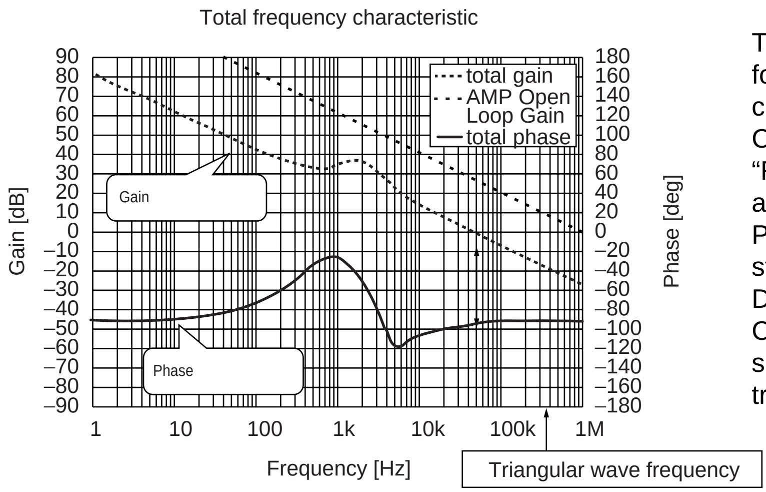


Cut-off frequency

$$f2(Hz) = \frac{1}{2\pi \times Rc \times Cc}$$

Rc = 150 kΩ
Cc = 3300 pF

• Frequency Characteristics of DC/DC converter

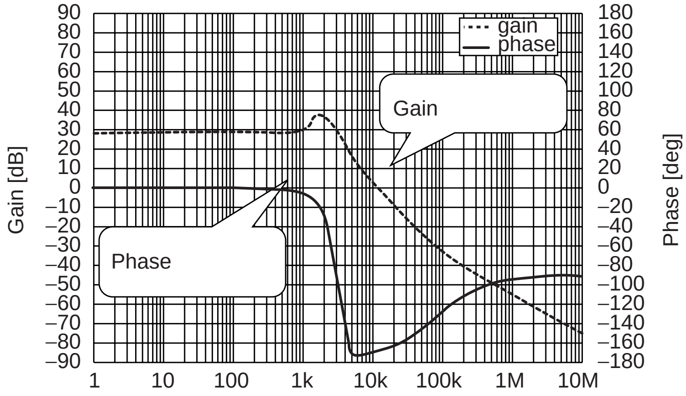


The overview of frequency characteristic for DC/DC converter can be obtained in combination between "Frequency Characteristics of LC filter" and "Frequency Characteristics of Error Amp " as mentioned above.
Please note the following point in order to stabilize the frequency characteristics of DC/DC converter .
Cut-off frequency of DC/DC converter should be set to half or less of the triangular wave oscillator frequency.

Notes : 1) Please review the Error Amp frequency characteristics, when LC filter parameter is modified.
2) When the ceramic capacitor is used as smoothing capacitor Co, phase margin is reduced because ESR of the ceramic capacitor is extremely small as shown in "Frequency Characteristics of LC filter which is using low ESR".
Therefore, change phase compensation of Error Amp or create resistance equivalent to ESR using pattern.

- Frequency Characteristics of LC filter which is using low ESR

Frequency characteristic of power output LC filter
(DC gain is included.)

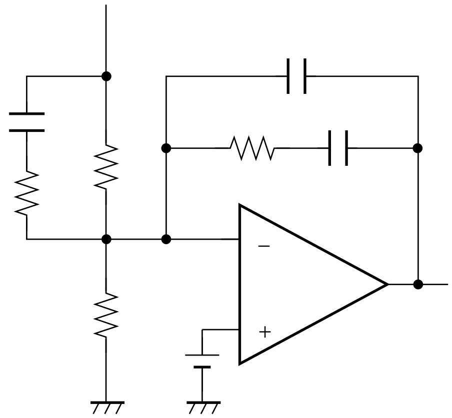


Cut-off frequency

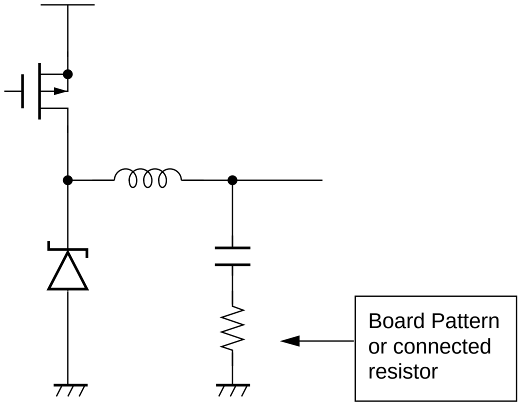
$$f1\ (Hz) = \frac{1}{2\pi\sqrt{Lo \times Co \times \dfrac{(Ro + ESR)}{(Ro + RL)}}}$$

Lo = 15 µH
Co = 14.1 µF
Ro = 4.2 Ω
RL = 30 mΩ
ESR = 100 mΩ

<3Pole2Zero>
DC/DC output



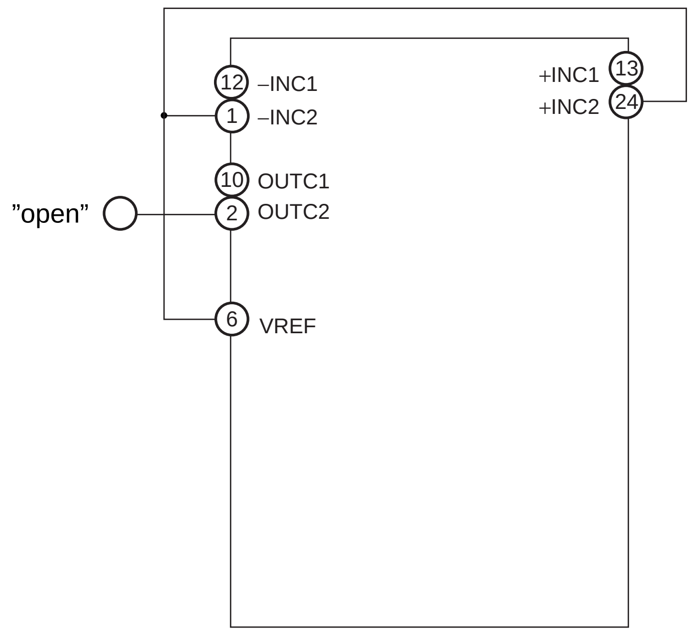
< Additional ESR>



■ PROCESSING WITHOUT USING OF THE CURRENT AMP1 AND AMP2

When Current Amp is not used, connect the +INC1 terminal (pin 13) , +INC2 terminal (pin 24) , –INC1 terminal (pin 12) , and –INC2 terminal (pin 1) to VREF terminal (pin 6) , and then leave OUTC1 terminal (pin 10) and OUTC2 terminal (pin 2) open.

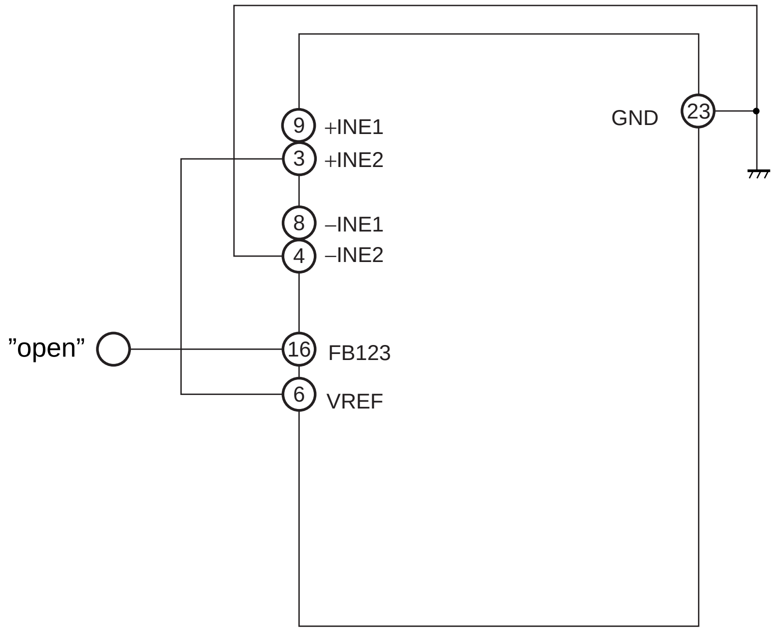
- **Connection when Current Amp is not used**



■ PROCESSING WITHOUT USING OF THE ERROR AMP1 AND AMP2

When Error Amp is not used, leave FB123 terminal (pin 15) open, connect the –INE1 terminal (pin 8) and –INE2 terminal (pin 4) to GND, and connect +INE1 terminal (pin 9) and +INE2 terminal (pin 3) to VREF terminal (pin 6) .

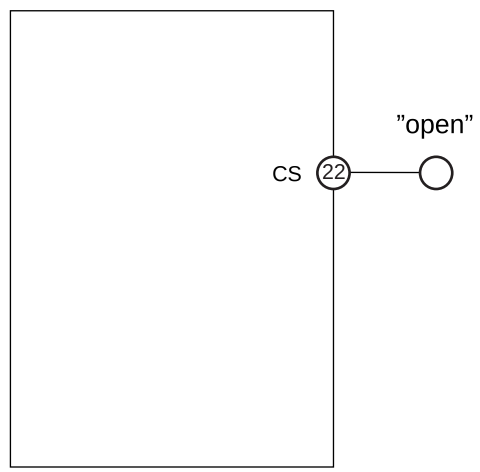
- **Connection when Error Amp is not used**



■ PROCESSING WITHOUT USING OF THE CS TERMINAL

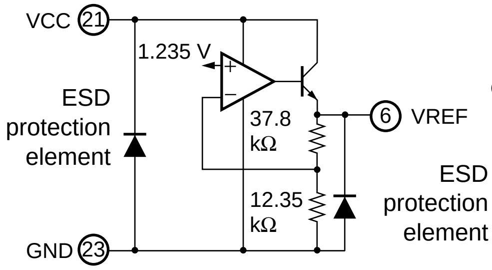
When soft-start function is not used, leave the CS terminal (pin 22) open.

- **Connection when no soft-start time is specified**

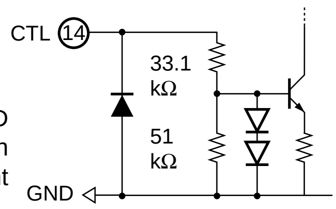


■ I/O EQUIVALENT CIRCUIT

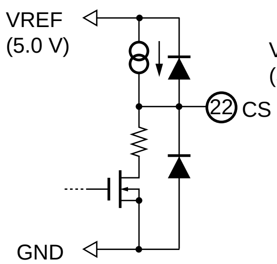
• <Reference voltage block>



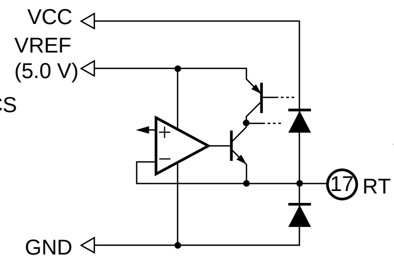
• <Power supply control block>



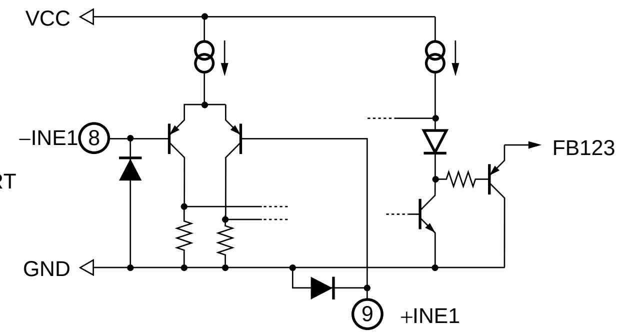
• <Soft-start block>



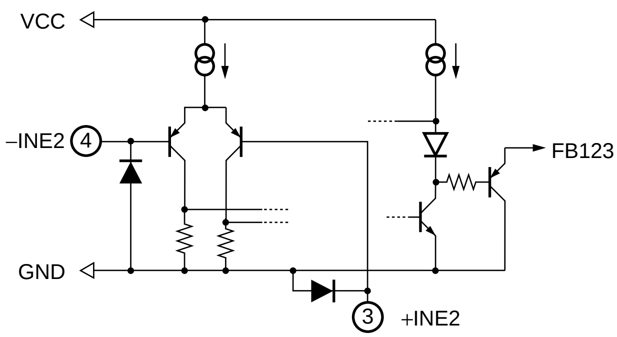
• <Triangular wave oscillator block>



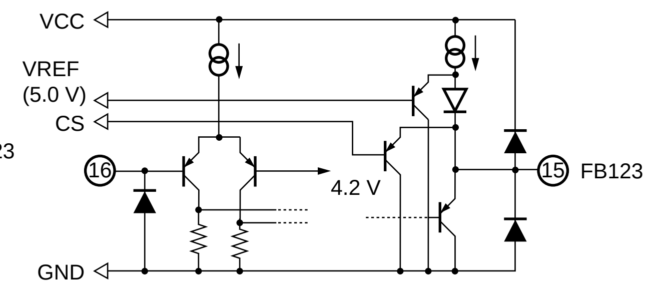
• <Error amplifier block (Error Amp1) >



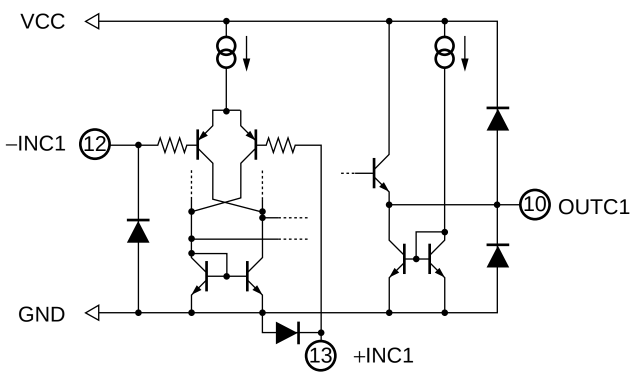
• <Error amplifier block (Error Amp2) >



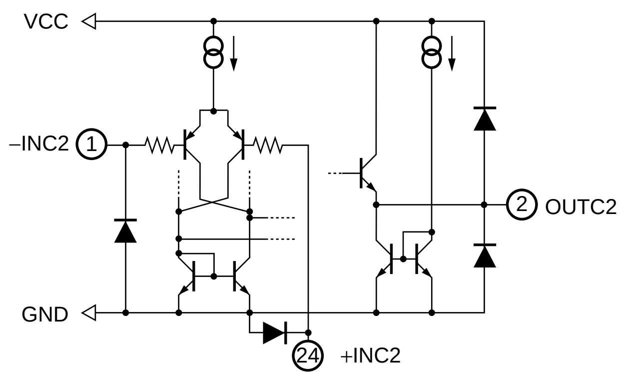
• <Error amplifier block (Error Amp3) >



• <Current detection amplifier block
(Current Amp1) >



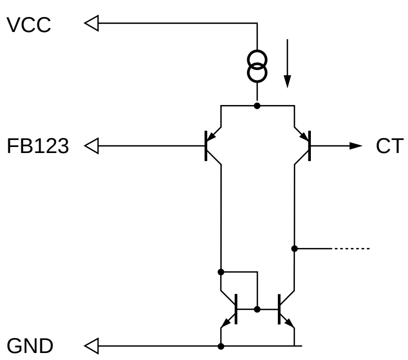
• <Current detection amplifier block
(Current Amp2) >



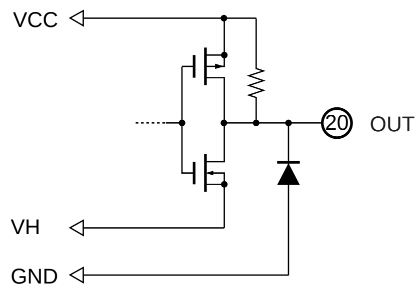
(Continued)

(Continued)

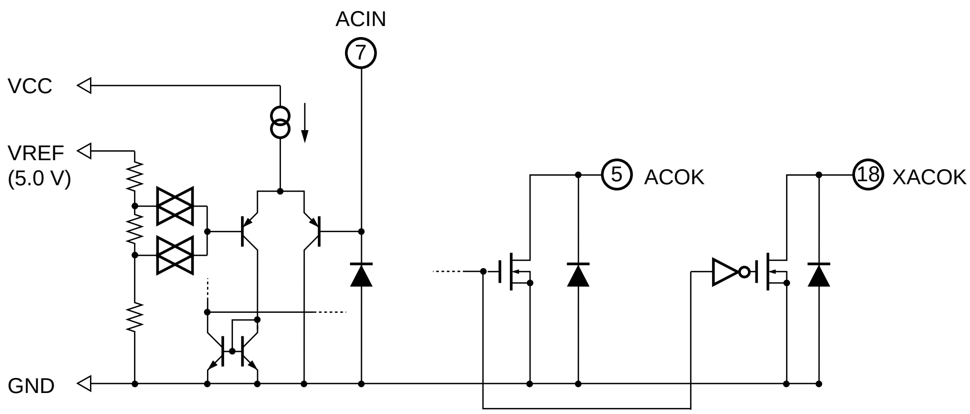
- <PWM comparator block>



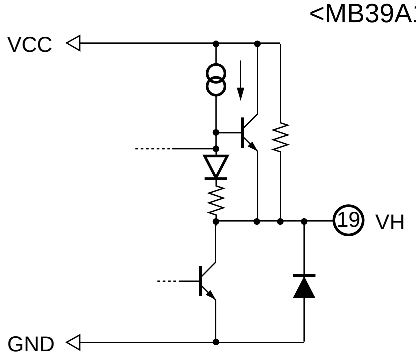
- <Output block>



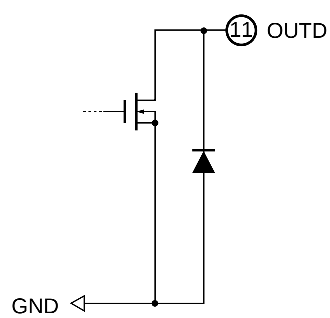
- <AC adapter voltage detection block>



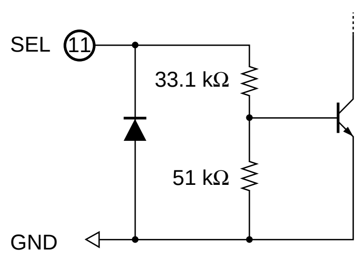
- <Bias voltage block>



- <Invalidity current prevention block>
<MB39A125>

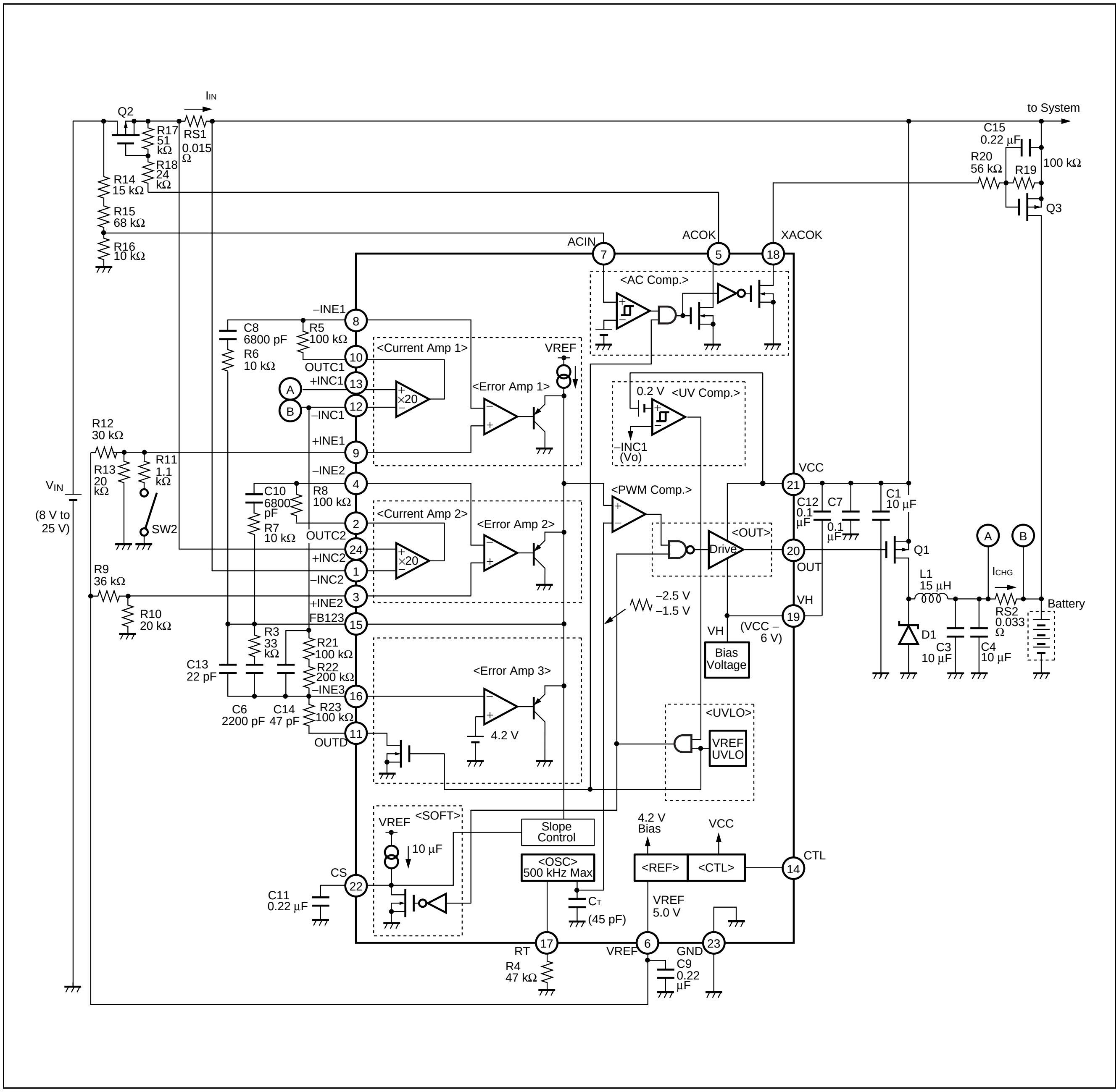


- <Output voltage switching function block>
<MB39A126>



■ APPLICATION EXAMPLE 1

• MB39A125



■ PARTS LIST 1

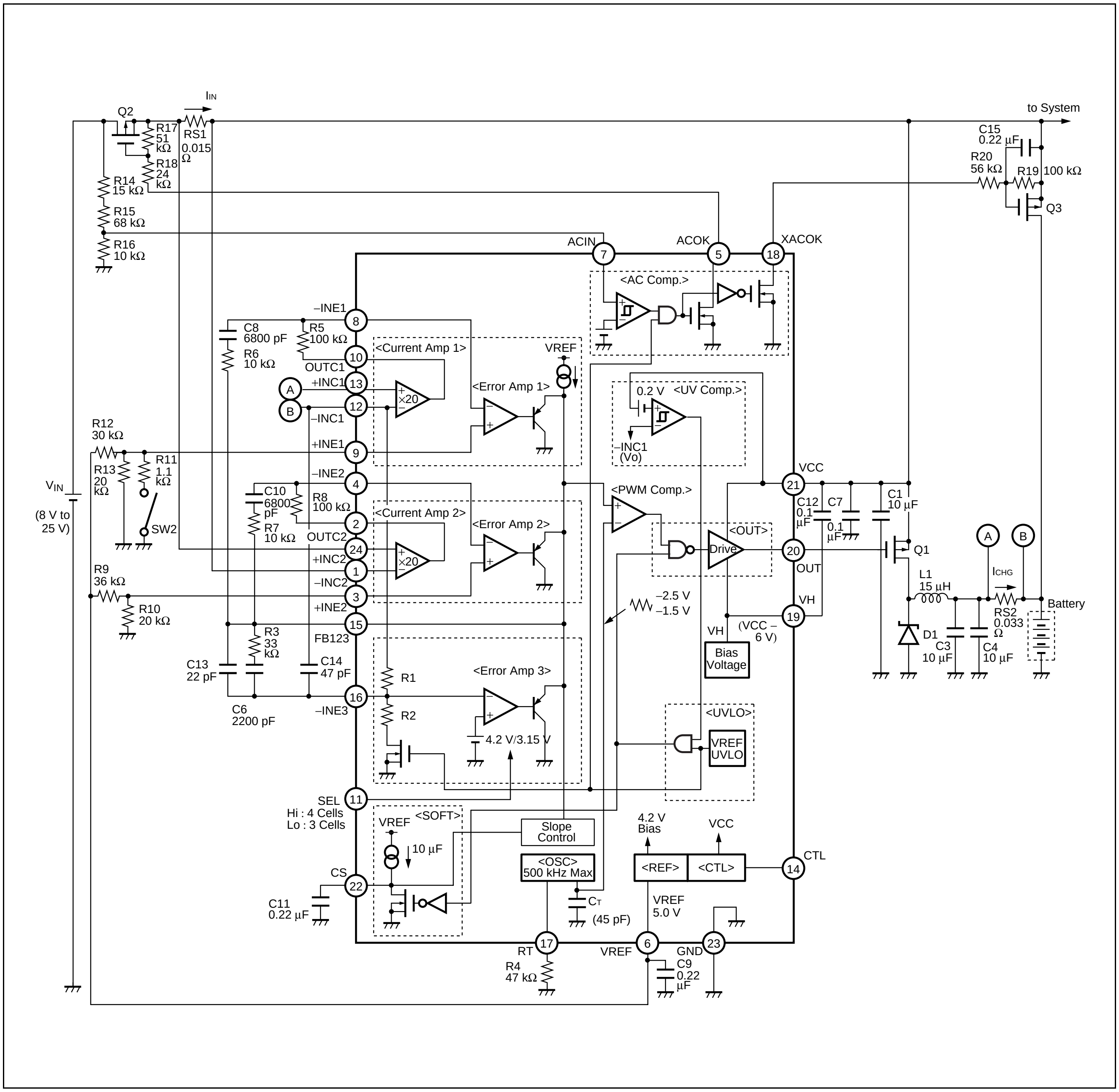
• **MB39A125**

COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS No.
Q1, Q2, Q3	Pch FET	VDS = –30 V, ID = –7.0 A		NEC	µPA2714GR
D1	Diode	VF = 0.42 V (Max) , At IF = 3 A		ROHM	RB053L-30
L1	Inductor	15 µH	3.6 A, 50 mΩ	SUMIDA	CDRH104R-150
C1, C3, C4	Ceramics Condenser	10 µF	25 V	TDK	C3225X5R1E106K
C6	Ceramics Condenser	2200 pF	50 V	TDK	C1608JB1H222K
C7, C12	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
C8, C10	Ceramics Condenser	6800 pF	50 V	TDK	C1608JB1H682K
C9, C11	Ceramics Condenser	0.22 µF	16 V	TDK	C1608JB1C224K
C13	Ceramics Condenser	22 pF	50 V	TDK	C1608CH1H220J
C14	Ceramics Condenser	47 pF	50 V	TDK	C1608CH1H470J
C15	Ceramics Condenser	0.22 µF	25 V	TDK	C2012JB1E224K
RS1	Resistor	15 mΩ	1%	KOA	SL1TTE15LOF
RS2	Resistor	33 mΩ	1%	KOA	SL1TTE33LOF
R3	Resistor	33 kΩ	0.5%	ssm	RR0816P-333-D
R4	Resistor	47 kΩ	0.5%	ssm	RR0816P-473-D
R5, R8	Resistor	100 kΩ	0.5%	ssm	RR0816P-104-D
R6, R7	Resistor	10 kΩ	0.5%	ssm	RR0816P-103-D
R9	Resistor	36 kΩ	0.5%	ssm	RR0816P-363-D
R10	Resistor	20 kΩ	0.5%	ssm	RR0816P-203-D
R11	Resistor	1.1 kΩ	0.5%	ssm	RR0816P-112-D
R12	Resistor	30 kΩ	0.5%	ssm	RR0816P-303-D
R13	Resistor	20 kΩ	0.5%	ssm	RR0816P-203-D
R14	Resistor	15 kΩ	0.5%	ssm	RR0816P-153-D
R15	Resistor	68 kΩ	0.5%	ssm	RR0816P-683-D
R16	Resistor	10 kΩ	0.5%	ssm	RR0816P-103-D
R17	Resistor	51 kΩ	0.5%	ssm	RR0816P-513-D
R18	Resistor	24 kΩ	0.5%	ssm	RR0816P-243-D
R19, R21, R23	Resistor	100 kΩ	0.5%	ssm	RR0816P-104-D
R20	Resistor	56 kΩ	0.5%	ssm	RR0816P-563-D
R22	Resistor	200 kΩ	0.5%	ssm	RR0816P-204-D

Note : NEC : NEC Corporation
ROHM : ROHM CO., LTD.
SUMIDA : Sumida Corporation
TDK : TDK Corporation
KOA : KOA Corporation
ssm : SUSUMU CO., LTD.

■ APPLICATION EXAMPLE 2

• MB39A126



■ PARTS LIST 2

• MB39A126

COMPONENT	ITEM	SPECIFICATION		VENDOR	PARTS No.
Q1, Q2, Q3	Pch FET	VDS = –30 V, ID = -7.0 A		NEC	µPA2714GR
D1	Diode	VF = 0.42 V (Max) , At IF = 3 A		ROHM	RB053L-30
L1	Inductor	15 µH	3.6 A, 50 mΩ	SUMIDA	CDRH104R-150
C1, C3, C4	Ceramics Condenser	10 µF	25 V	TDK	C3225X5R1E106K
C6	Ceramics Condenser	2200 pF	50 V	TDK	C1608JB1H222K
C7, C12	Ceramics Condenser	0.1 µF	50 V	TDK	C1608JB1H104K
C8, C10	Ceramics Condenser	6800 pF	50 V	TDK	C1608JB1H682K
C9, C11	Ceramics Condenser	0.22 µF	16 V	TDK	C1608JB1C224K
C13	Ceramics Condenser	22 pF	50 V	TDK	C1608CH1H220J
C14	Ceramics Condenser	47 pF	50 V	TDK	C1608CH1H470J
C15	Ceramics Condenser	0.22 µF	25 V	TDK	C2012JB1E224K
RS1	Resistor	15 mΩ	1%	KOA	SL1TTE15LOF
RS2	Resistor	33 mΩ	1%	KOA	SL1TTE33LOF
R3	Resistor	33 kΩ	0.5%	ssm	RR0816P-333-D
R4	Resistor	47 kΩ	0.5%	ssm	RR0816P-473-D
R5, R8	Resistor	100 kΩ	0.5%	ssm	RR0816P-104-D
R6, R7	Resistor	10 kΩ	0.5%	ssm	RR0816P-103-D
R9	Resistor	36 kΩ	0.5%	ssm	RR0816P-363-D
R10	Resistor	20 kΩ	0.5%	ssm	RR0816P-203-D
R11	Resistor	1.1 kΩ	0.5%	ssm	RR0816P-112-D
R12	Resistor	30 kΩ	0.5%	ssm	RR0816P-303-D
R13	Resistor	20 kΩ	0.5%	ssm	RR0816P-203-D
R14	Resistor	15 kΩ	0.5%	ssm	RR0816P-153-D
R15	Resistor	68 kΩ	0.5%	ssm	RR0816P-683-D
R16	Resistor	10 kΩ	0.5%	ssm	RR0816P-103-D
R17	Resistor	51 kΩ	0.5%	ssm	RR0816P-513-D
R18	Resistor	24 kΩ	0.5%	ssm	RR0816P-243-D
R19	Resistor	100 kΩ	0.5%	ssm	RR0816P-104-D
R20	Resistor	56 kΩ	0.5%	ssm	RR0816P-563-D

Note : NEC : NEC Corporation
ROHM : ROHM CO., LTD.
SUMIDA : Sumida Corporation
TDK : TDK Corporation
KOA : KOA Corporation
ssm : SUSUMU CO., LTD.

■ SELECTION OF COMPONENTS

• Pch MOS FET

The Pch MOS FET for switching use should be rated for at least +20% more than the input voltage. To minimize continuity loss, use a FET with low R_{DS} (ON) between the drain and source. For high input voltage and high frequency operation, on-cycle switching loss will be higher so that power dissipation must be considered. In this application, the NEC μPA2714GR is used. Continuity loss, on/off switching loss, and total loss are determined by the following formulas. The selection must ensure that peak drain current does not exceed rated values.

Continuity loss : Pc

$$P_C = I_D^2 \times R_{DS(ON)} \times Duty$$

On-cycle switching loss : $P_{S(ON)}$

$$P_{S(ON)} = \frac{V_{D(Max)} \times I_D \times tr \times fosc}{6}$$

Off-cycle switching loss : $P_{S(OFF)}$

$$P_{S(OFF)} = \frac{V_{D(Max)} \times I_{D(Max)} \times tf \times fosc}{6}$$

Total loss : P_T

$$P_T = P_C + P_{S(ON)} + P_{S(OFF)}$$

Example) Using the μPA2714GR
16.8 V setting

Input voltage $V_{IN(Max)} = 25$ V, output voltage $V_O = 16.8$ V, drain current $I_D = 3$ A, oscillation frequency fosc = 300 kHz, L = 15 μH, drain-source on resistance $R_{DS(ON)} \fallingdotseq 18$ mΩ, tr ≒ 15 ns, tf ≒ 42 ns

Drain current (Max) : $I_{D(Max)}$

$$I_{D(Max)} = Io + \frac{V_{IN} - Vo}{2L} t_{ON}$$

$$= 3 + \frac{25 - 16.8}{2 \times 15 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.672$$

$$\fallingdotseq \underline{3.6\ A}$$

Drain current (Min) : $I_{D(Min)}$

$$I_{D(Min)} = Io - \frac{V_{IN} - Vo}{2L} t_{ON}$$

$$= 3 - \frac{25 - 16.8}{2 \times 15 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.672$$

$$\fallingdotseq \underline{2.4\ A}$$

$$P_C = I_D^2 \times R_{DS(ON)} \times Duty$$
$$= 3^2 \times 0.018 \times 0.672$$
$$\fallingdotseq \underline{0.109\ W}$$

$$P_{S(ON)} = \frac{V_D \times I_D \times tr \times fosc}{6}$$
$$= \frac{25 \times 3 \times 15 \times 10^{-9} \times 300 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.056\ W}$$

$$P_{S(OFF)} = \frac{V_D \times I_{D(Max)} \times tf \times fosc}{6}$$
$$= \frac{25 \times 3.6 \times 42 \times 10^{-9} \times 300 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.189\ W}$$

$$P_T = P_C + P_{S(ON)} + P_{S(OFF)}$$
$$\fallingdotseq 0.109 + 0.056 + 0.189$$
$$\fallingdotseq \underline{0.354\ W}$$

The above power dissipation figures for the µPA2714GR are satisfied with ample margin at 2.0 W.

12.6 V setting

Input voltage $V_{IN(Max)} = 22$ V, output voltage $V_O = 12.6$ V, drain current $I_D = 3$ A, oscillation frequency fosc $= 300$ kHz, L $= 15$ µH, drain-source on resistance $R_{DS(ON)} \fallingdotseq 18$ mΩ, tr $\fallingdotseq$ 15 ns, tf $\fallingdotseq$ 42 ns

Drain current (Max) : $I_{D(Max)}$

$$I_{D(Max)} = Io + \frac{V_{IN} - Vo}{2L} t_{ON}$$
$$= 3 + \frac{22 - 12.6}{2 \times 15 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.572$$
$$\fallingdotseq \underline{3.6\ A}$$

Drain current (Min) : $I_{D(Min)}$

$$I_{D(Min)} = Io - \frac{V_{IN} - Vo}{2L} t_{ON}$$
$$= 3 - \frac{22 - 12.6}{2 \times 15 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.572$$
$$\fallingdotseq \underline{2.4\ A}$$

$$P_C = I_D^2 \times R_{DS(ON)} \times Duty$$
$$= 3^2 \times 0.018 \times 0.572$$
$$\fallingdotseq \underline{0.093\ W}$$

$$P_{S(ON)} = \frac{V_D \times I_D \times tr \times fosc}{6}$$
$$= \frac{22 \times 3 \times 15 \times 10^{-9} \times 300 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.050\ W}$$

$$P_{S(OFF)} = \frac{V_D \times I_{D(Max)} \times tf \times fosc}{6}$$
$$= \frac{22 \times 3.6 \times 42 \times 10^{-9} \times 300 \times 10^3}{6}$$
$$\fallingdotseq \underline{0.166\ W}$$

$$P_T = P_C + P_{S(ON)} + P_{S(OFF)}$$
$$\fallingdotseq 0.093 + 0.050 + 0.166$$
$$\fallingdotseq \underline{0.309\ W}$$

The above power dissipation figures for the µPA2714GR are satisfied with ample margin at 2.0 W.

The Pch MOS FET for switching use must use the one of more than input voltage +20%.

FET which operates when the AC adapter is connected should select FET which satisfies the current decided by sense resistance R1 enough. Because FET which operates when the AC adapter is not connected becomes a supply by the battery, it is necessary to select FET which satisfies the current of the system enough.

In this application, the NEC µPA2714GR is used.

- **Inductor**

In selecting inductors, it is of course essential not to apply more current than the rated capacity of the inductor, but also to note that the lower limit for ripple current is a critical point that if reached will cause discontinuous operation and a considerable drop in efficiency. This can be prevented by choosing a higher inductance value, which will enable continuous operation under light-loads.

Note that if the inductance value is too high, however, direct current resistance (DCR) is increased and this will also reduce efficiency. The inductance must be set at the point where efficiency is greatest.

Note also that the DC superimposition characteristic becomes worse as the load current value approaches the rated current value of the inductor, so that the inductance value is reduced and ripple current increases, causing loss of efficiency.

The selection of rated current value and inductance value will vary depending on where the point of peak efficiency lies with respect to load current.

Inductance values are determined by the following formulas.

The L value for all load current conditions is set so that the peak to peak value of the ripple current is 1/2 the load current or less.

Inductance value : L

$$L \geq \frac{2(V_{IN} - Vo)}{Io} t_{ON}$$

16.8 V output
Example)

$$L \geq \frac{2(V_{IN\,(Max)} - Vo)}{Io} t_{ON}$$

$$\geq \frac{2 \times (25 - 16.8)}{3} \times \frac{1}{300 \times 10^3} \times 0.672$$

$$\geq \underline{12.2\ \mu H}$$

12.6 V output
Example)

$$L \geq \frac{2(V_{IN\,(Max)} - Vo)}{Io} t_{ON}$$

$$\geq \frac{2 \times (22 - 12.6)}{3} \times \frac{1}{300 \times 10^3} \times 0.572$$

$$\geq \underline{12.0\ \mu H}$$

Inductance values derived from the above formulas are values that provide sufficient margin for continuous operation at maximum load current, but at which continuous operation is not possible at light loads. It is therefore necessary to determine the load level at which continuous operation becomes possible. In this application, the SUMIDA CDRH104R-150 is used. The following formula is available to obtain the load current as a continuous current condition when 15 µH is used.

The value of the load current satisfying the continuous current condition : Io

$$Io \geq \frac{Vo}{2L} t_{OFF}$$

Example) Using the CDRH104R-150

15 µH (tolerance ± 30%) , rated current = 3.6 A

16.8 V output

$$Io \geq \frac{Vo}{2L} t_{OFF}$$

$$\geq \frac{16.8}{2 \times 15 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times (1 - 0.672)$$

$$\geq \underline{0.61\ A}$$

12.6 V output

$$Io \geq \frac{Vo}{2L} t_{OFF}$$

$$\geq \frac{12.6}{2 \times 15 \times 10^{-6}} \times \frac{1}{300 \times 10^{3}} \times (1 - 0.572)$$

$$\geq \underline{0.60\ A}$$

To determine whether the current through the inductor is within rated values, it is necessary to determine the peak value of the ripple current as well as the peak-to-peak values of the ripple current that affects the output ripple voltage. The peak value and peak-to-peak value of the ripple current can be determined by the following formulas.

Peak Value : I_L

$$I_L \geq Io + \frac{V_{IN} - Vo}{2L} t_{ON}$$

Peak-to-peak Value : ΔI_L

$$\Delta I_L = \frac{V_{IN} - Vo}{L} t_{ON}$$

Example) Using the CDRH104R-150
15 µH (tolerance ± 30%) , rated current = 3.6 A

Peak Value
16.8 V output

$$I_L \geq Io + \frac{V_{IN} - Vo}{2L} t_{ON}$$

$$\geq 3 + \frac{25 - 16.8}{2 \times 15 \times 10^{-6}} \times \frac{1}{300 \times 10^{3}} \times 0.672$$

$$\geq \underline{3.6\ A}$$

12.6 V output

$$I_L \geq Io + \frac{V_{IN} - Vo}{2L} t_{ON}$$

$$\geq 3 + \frac{22 - 12.6}{2 \times 15 \times 10^{-6}} \times \frac{1}{300 \times 10^{3}} \times 0.572$$

$$\geq \underline{3.6\ A}$$

Peak-to-peak Value
16.8 V output

$$\Delta I_L = \frac{V_{IN} - V_O}{L} t_{ON}$$

$$= \frac{25 - 16.8}{15 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.672$$

$$\fallingdotseq \underline{1.22\ A}$$

12.6 V output

$$\Delta I_L = \frac{V_{IN} - V_O}{L} t_{ON}$$

$$= \frac{22 - 12.6}{15 \times 10^{-6}} \times \frac{1}{300 \times 10^3} \times 0.572$$

$$\fallingdotseq \underline{1.2\ A}$$

• Flyback diode

Shottky barrier diode (SBD) is generally used for the flyback diode when the reverse voltage to the diode is less than 40V. The SBD has the characteristics of higher speed in terms of faster reverse recovery time, and lower forward voltage, and is ideal for achieving high efficiency. As long as the DC reverse voltage is sufficiently higher than the input voltage, and the mean current flowing during the diode conduction time is within the mean output current level, and as the peak current is within the peak surge current limits, there is no problem. In this application the ROHM RB053L-30 are used. The diode mean current and diode peak current can be obtained by the following formulas.

Diode mean current : I_{Di}

$$I_{Di} \geq I_O \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

Diode peak current : I_{Dip}

$$I_{Dip} \geq \left(I_O + \frac{V_O}{2L} t_{OFF}\right)$$

Example) Using the RB053L-30

V_R (DC reverse voltage) = 30 V, mean output current = 3.0 A, peak surge current = 70 A,
V_F (forward voltage) = 0.42 V, at I_F = 3.0 A

16.8 V output

$$I_{Di} \geq I_O \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

$$\geq 3 \times (1 - 0.672)$$

$$\geq \underline{0.984\ A}$$

12.6 V output

$$I_{Di} \geq I_O \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

$$\geq 3 \times (1 - 0.572)$$

$$\geq \underline{1.284\ A}$$

16.8 V output

$$I_{Dip} \geq \left(I_O + \frac{V_O}{2L} t_{OFF}\right)$$

$$\geq \underline{3.6\ A}$$

12.6 V output

$$I_{Dip} \geq \left(I_O + \frac{V_O}{2L} t_{OFF}\right)$$

$$\geq \underline{3.6\ A}$$

- **Charge current sense resistor**

Please note the following in selecting the charge current sense resistance. First of all, meet the electric power to the flowing current. However, the conversion efficiency deteriorates because the loss in the sense resistance grows when resistance is adjusted to a too big value. The accuracy of the charge current deteriorates because the voltage difference of both ends of the sense resistance becomes small when resistance is adjusted to a too small value oppositely. 33 mΩ of the KOA SL1TTE33LOF is used in this application. The sense resistance value can be determined by the following formulas.

In this application, 33 mΩ of the KOA SL1TTE33LOF is used.

Sense resistor : RS2

$$RS2 = \frac{+INE1}{20 \times I_O}$$

Example) When the +INE1 terminal (pin 9) voltage is 2 V and the charge current (Io) is 3.0 A

$$RS2 = \frac{+INE1}{20 \times I_O}$$

$$= \frac{2}{20 \times 3.0}$$

$$= \underline{33.3\ m\Omega}$$

• Input current sense resistor

Please note the following in selecting the input current sense resistance. First of all, meet the electric power to the flowing current. However, the conversion efficiency deteriorates because the loss in the sense resistance grows when resistance is adjusted to a too big value. The accuracy of the input current deteriorates because the voltage difference of both ends of the sense resistance becomes small when resistance is adjusted to a too small value oppositely. 33 mΩ of the KOA SL1TTE33LOF is used in this application. The sense resistance value can be determined by the following formulas.

In this application, 15 mΩ of the KOA SL1TTE15LOF is used.

Sense resistor : RS1

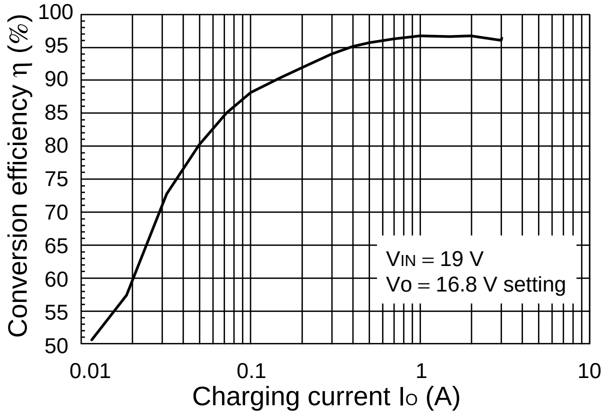
$$RS1 = \frac{+INE2}{20 \times I_{IN}}$$

Example) When the +INE2 terminal (pin 3) voltage is 1.79 V and the input current (I_{IN}) is 6.0 A

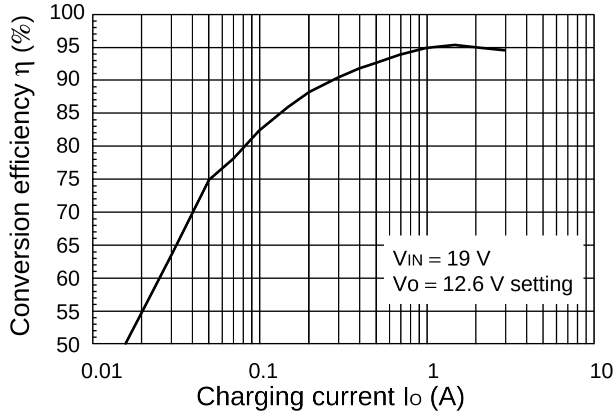
$$RS1 = \frac{+INE2}{20 \times I_{IN}} = \frac{1.79}{20 \times 6.0} = \underline{14.9\ m\Omega}$$

■ REFERENCE DATA

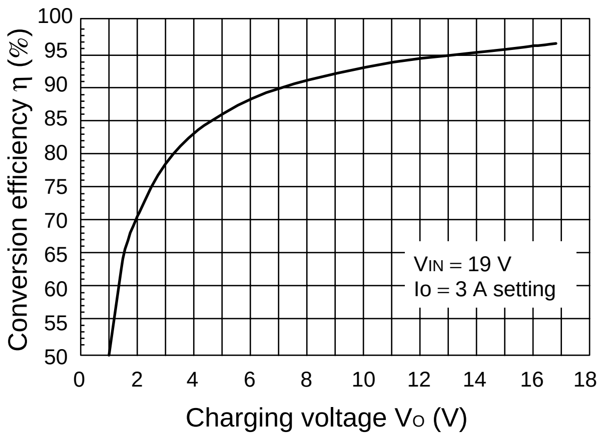
Conversion efficiency vs. Charging current
(Constant Voltage mode)



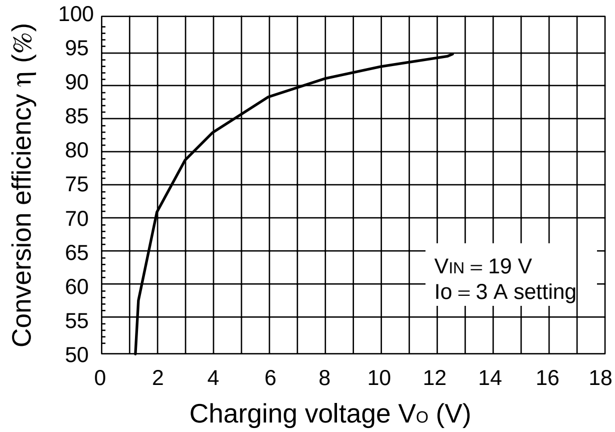
Conversion efficiency vs. Charging current
(Constant Voltage mode)



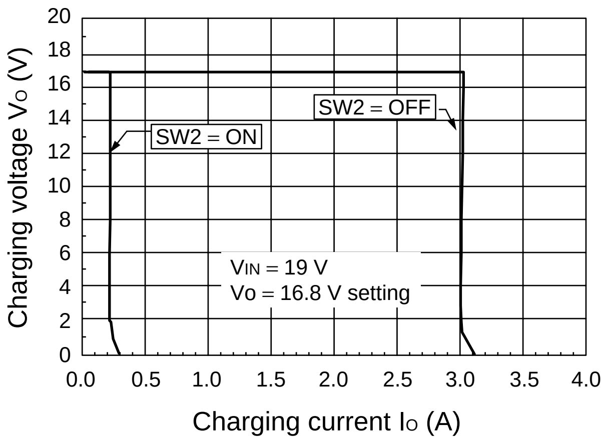
Conversion efficiency vs. Charging voltage
(Constant Current mode)



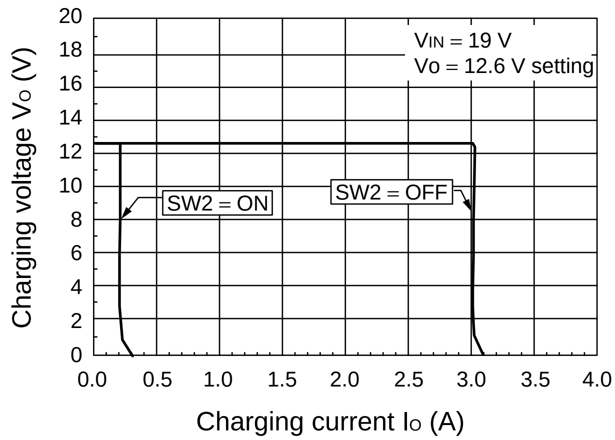
Conversion efficiency vs. Charging voltage
(Constant Current mode)



Charging voltage vs. Charging current



Charging voltage vs. Charging current



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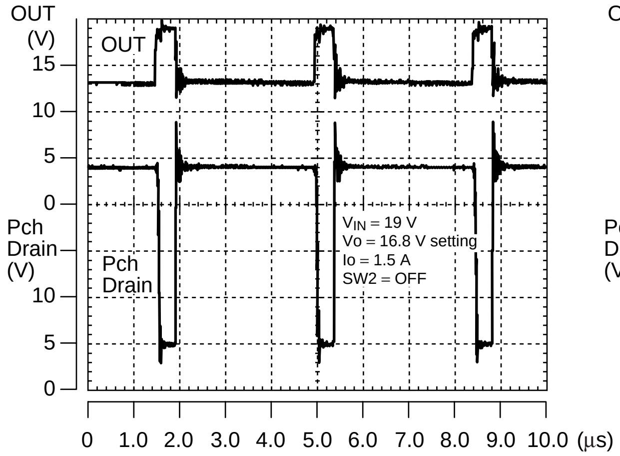
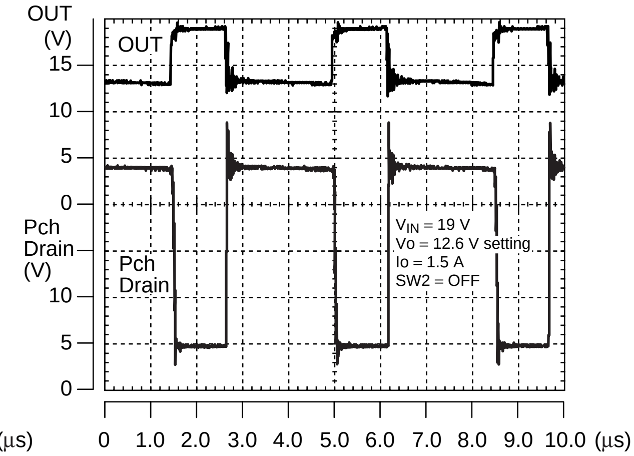
Switching waveform (Constant Voltage Mode)

V_O = 12.6 V setting

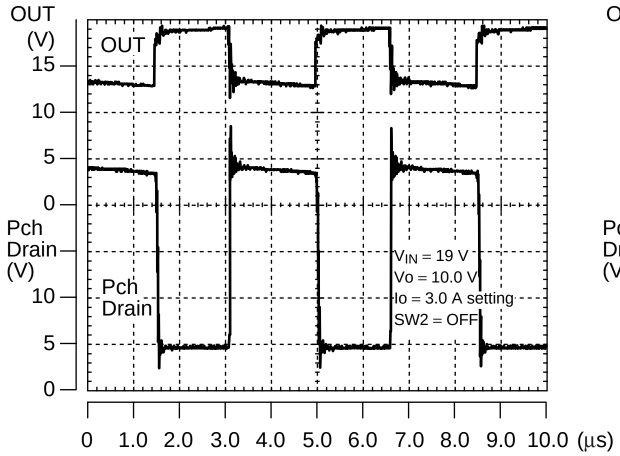


V_O = 16.8 V setting

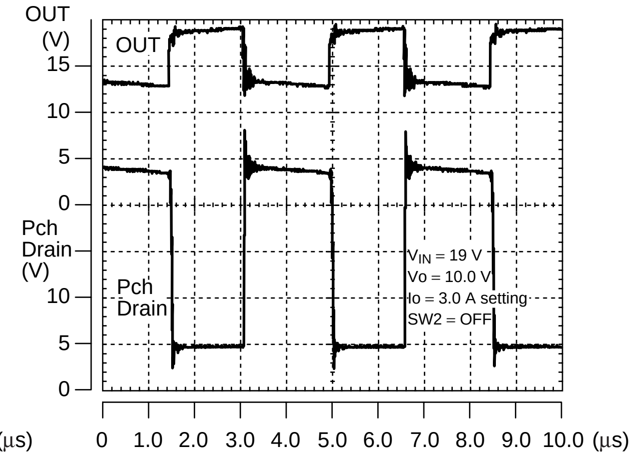


Switching waveform (Constant Current Mode)

V_O = 12.6 V setting



V_O = 16.8 V setting



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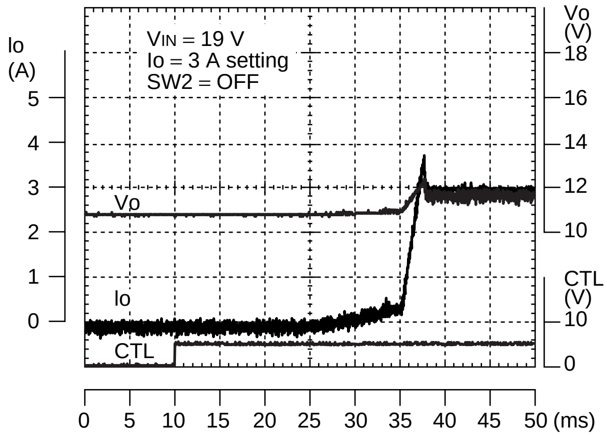
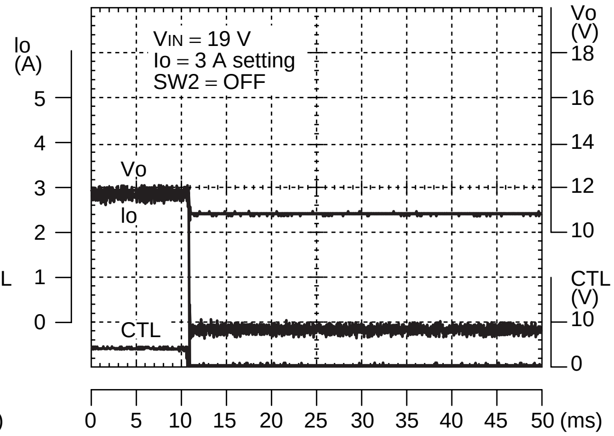
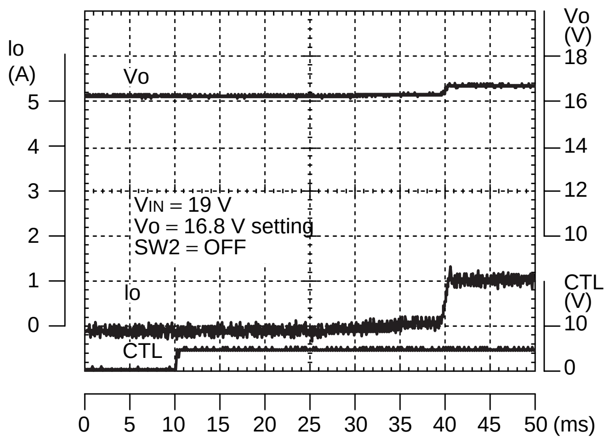
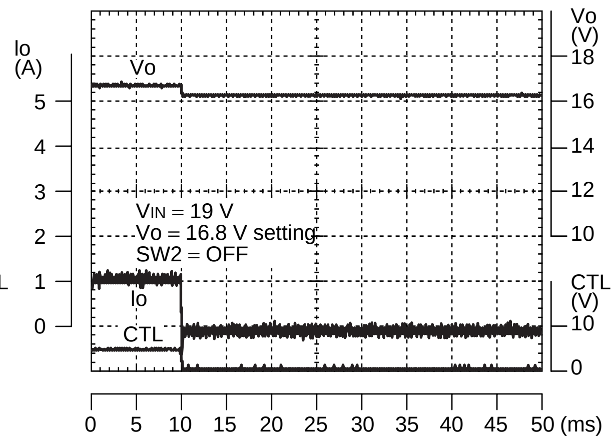
Soft-start operating waveform (Constant Current Mode)





Soft-start operating waveform (Constant Voltage Mode)





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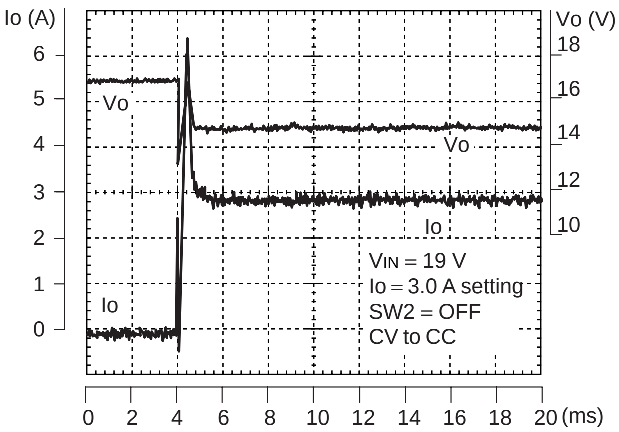
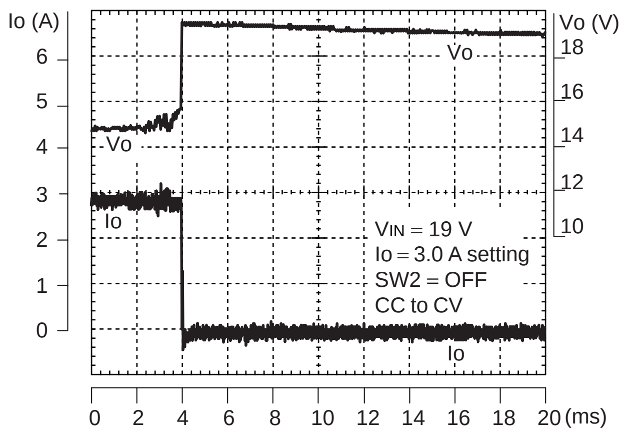
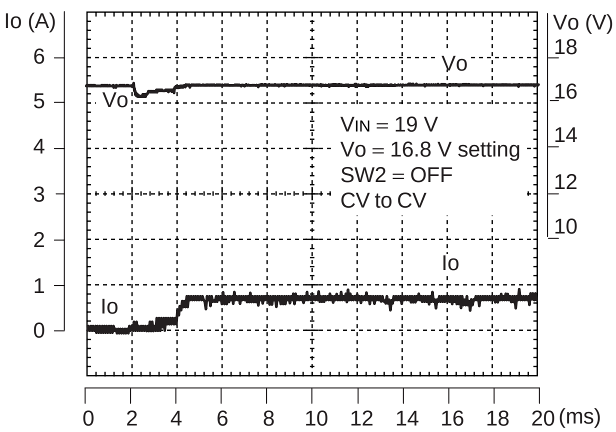
Load-step response operation waveform
(C.V mode → C.C mode)



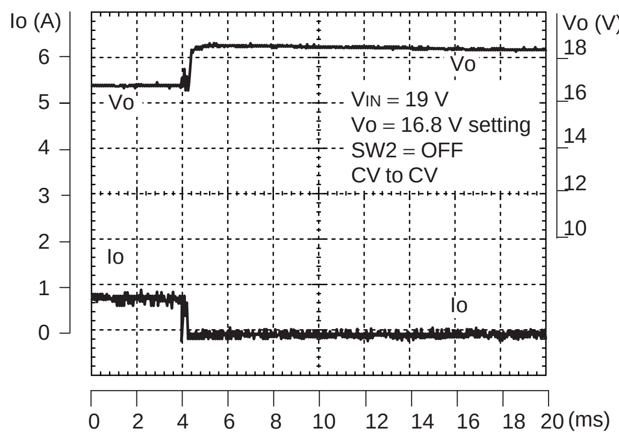
Load-step response operation waveform
(C.C mode → C.V mode)



Load-step response operation waveform
(C.V mode → C.V mode)



Load-step response operation waveform
(C.V mode → C.V mode)



■ USAGE PRECAUTIONS

- Printed circuit board ground lines should be set up with consideration for common impedance.

- Take appropriate static electricity measures.
- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

- Do not apply negative voltages.
- The use of negative voltages below –0.3 V may create parasitic transistors on LSI lines, which can cause abnormal operation.

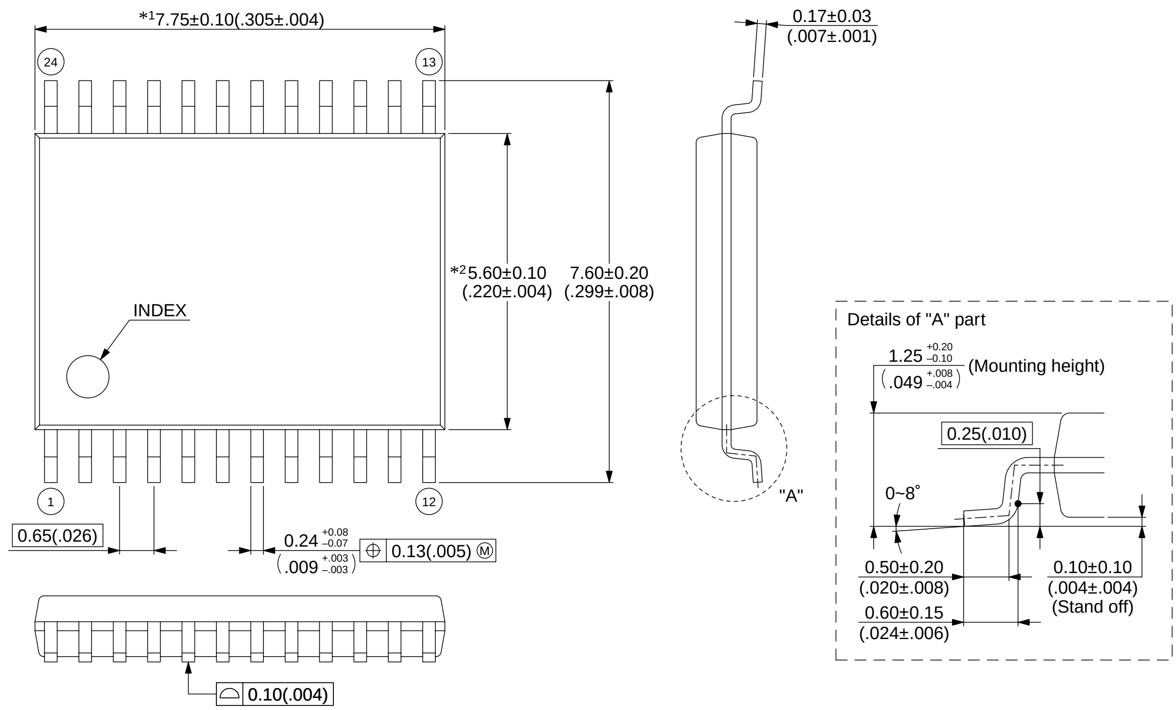
■ ORDERING INFORMATION

Part number	Package	Remarks
MB39A125PFV	24-pin plastic SSOP (FPT-24P-M03)	
MB39A125WQN	28-pin plastic QFN (LCC-28P-M11)	
MB39A126PFV	24-pin plastic SSOP (FPT-24P-M03)	
MB39A126WQN	28-pin plastic QFN (LCC-28P-M11)	

■ PACKAGE DIMENSIONS

24-pin plastic SSOP
(FPT-24P-M03)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max).
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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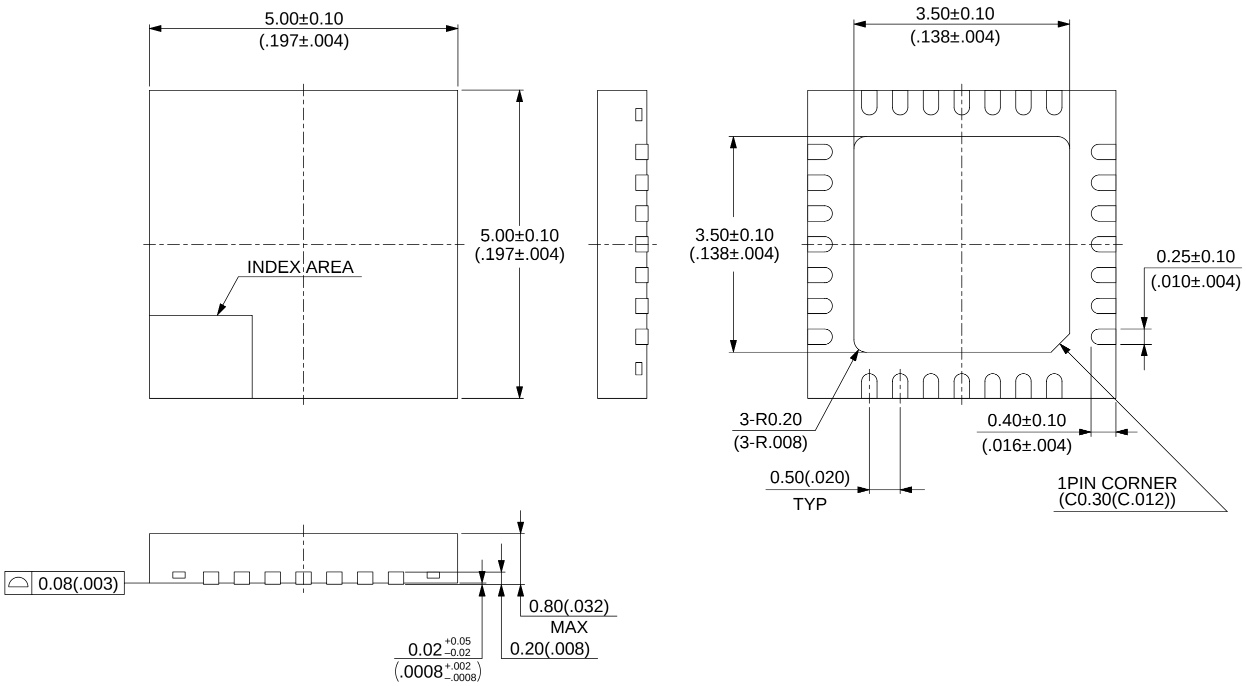
28-pin plastic QFN
(LCC-28P-M11)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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