



LA6541

4-channel Bridge Driver for Compact Discs

Overview

The LA6541 is a 4-channel bridge (BTL) driver with a 5 V power supply (uses an external PNP transistor) developed for compact discs.

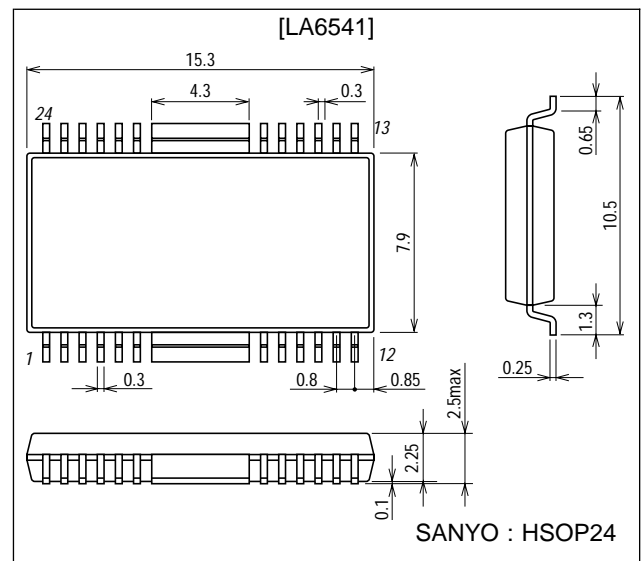
Functions and Features

- 4-channel bridge (BTL) power amplifier.
- I_O max. = 700 mA.
- With mute circuit
(Affects all amplifier outputs, Amp 1 to Amp 8).
(When the mute voltage is low, the outputs turn off;
when the mute voltage is high, the outputs turn on).
- 5.0 V regulator built in (Uses external PNP transistor).
- Reset circuit built in (The reset output delay time can be adjusted through an external capacitor).

Package Dimensions

unit : mm

3227-HSOP24



Specifications

Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		14	V
Maximum input voltage	V_{INB}		13	V
Mute pin voltage	V_{Mute}		13	V
Allowable power dissipation	P_d max	When using standard board 114.3 × 76.1 × 1.5 mm (material: glass epoxy)	2.3	W
Operating temperature	T_{opr}		-20 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended operating voltage	V_{CC}		5.6 to 13	V
Reset output source current	I_{ORH}		0 to 200	μA
Reset output sink current	I_{ORL}		0 to 2	mA

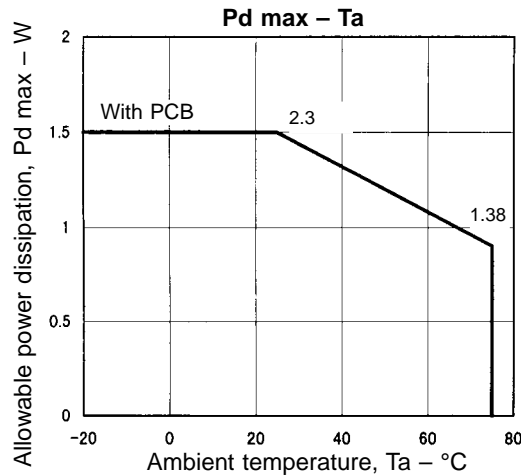
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Electrical Characteristics at Ta = 25°C, VCC = 8.0 V, VREF = 2.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
No-load current drain	ICC1	When all amplifier outputs are on (Mute high)		20	40	mA
	ICC2	When all amplifier outputs are off (Mute low)		15	35	mA
Output offset voltage	VOF1	Amplifier 1 to 2 (VO1 to VO2), Amplifier 3 to 4 (VO3 to VO4)	-50		+50	mV
	VOF2	Amplifier 5 to 6 (VO5 to VO6), Amplifier 7 to 8 (VO7 to VO8)	-50		+50	mV
Buffer amplifier input voltage range	VBIN		1.5		VCC-1.5	V
Input voltage range	VIN		1.0		VCC-1.5	V
Output source voltage	VO1	Note 1, when RL = 8.0 Ω	5.0	5.6		V
Output sink voltage	VO2	Note 2, when RL = 8.0 Ω		1.8	2.4	V
Closed-circuit voltage gain	VG	Between bridge amplifiers		9		dB
Slew rate	SR			0.15		V/μs
Mute on voltage	VMute	Note 3		1.2		V
[Power Supply] (with 2SB632K connected externally)						
Output voltage	VO1	IO = 200 mA	4.75	5.0	5.25	V
Line regulation	ΔVOLN1	5.6 V ≤ VIN1 ≤ 12 V		20	100	mV
Load regulation	ΔVOLD1	5 mA ≤ IO ≤ 200 mA		50	150	mV
[Reset]						
High reset output voltage	VORH	IORH = 200 μA, Cd pin open	4.73	4.98	5.23	V
Low reset output voltage	VORL	ISRL = 2 mA, Cd is shorted to GND		100	200	mV
Reset threshold voltage	VRT	Note 4		4.3		V
Reset hysteresis voltage	Vhys	Note 5	40	100	200	mV
Reset output delay time	td	Cd = 0.1 μF		10		ms

Notes:

- Source voltage to ground when an 8 Ω load is connected between bridge amplifier outputs.
- Sink voltage to ground when an 8 Ω load is connected between bridge amplifier outputs.
- When the mute signal is high, all amplifier outputs turn on, and when low, all amplifier outputs turn off. When the mute signal is low, amplifier output is undefined.
- 5 V supply voltage when the reset output goes low.
- Potential difference from the 5 V supply voltage when the reset output goes low and when it goes high.



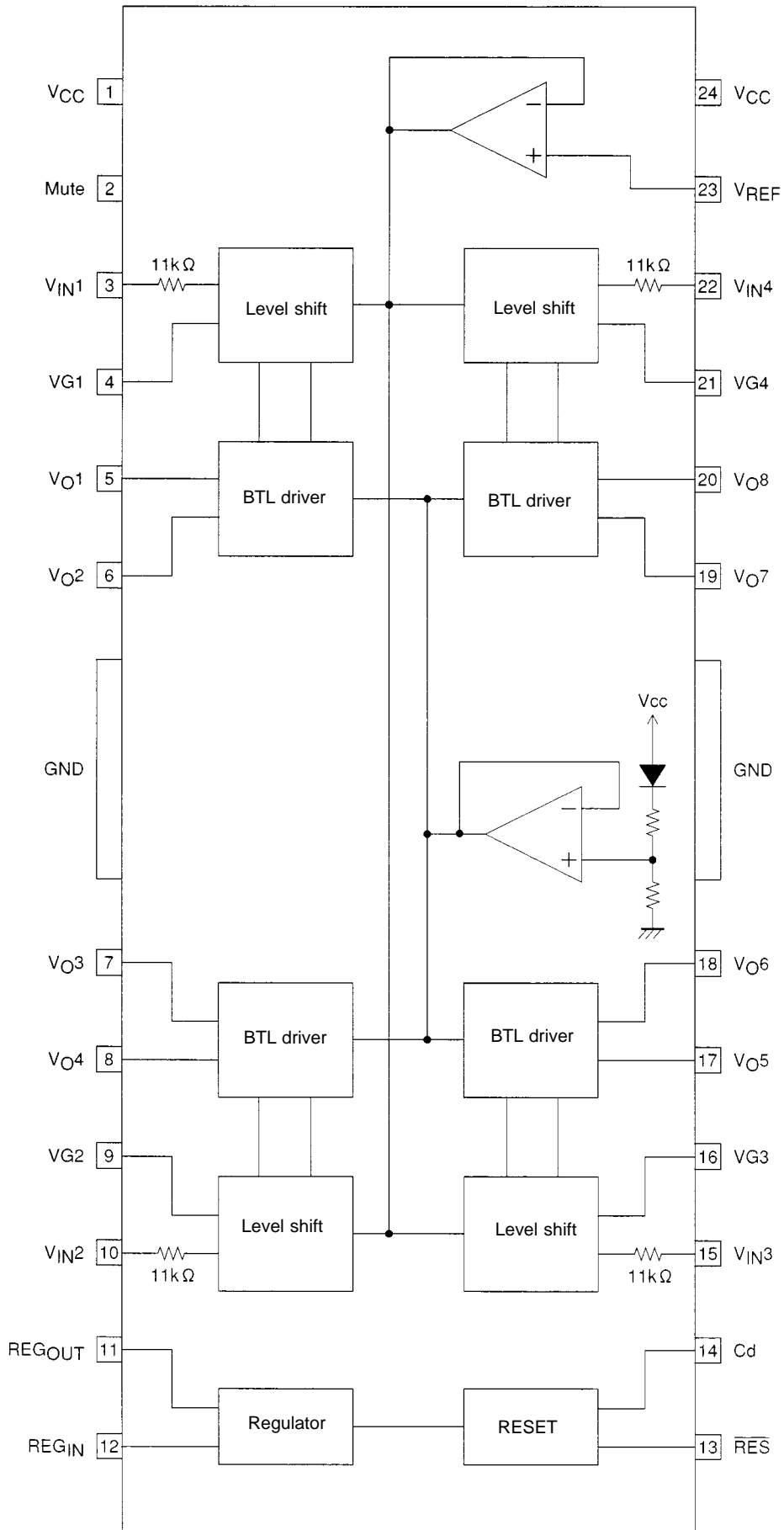
Truth Table

Input	MUTE	CH1		CH2		CH3		CH4	
		VO1 (Amp1)	VO2 (Amp2)	VO3 (Amp3)	VO4 (Amp4)	VO5 (Amp5)	VO6 (Amp6)	VO7 (Amp7)	VO8 (Amp8)
H	H	H	L	L	H	H	L	L	H
	L	—	—	—	—	—	—	—	—
L	H	L	H	H	L	L	H	H	L
	L	—	—	—	—	—	—	—	—

* The “—” symbol means “amplifier output is OFF.”

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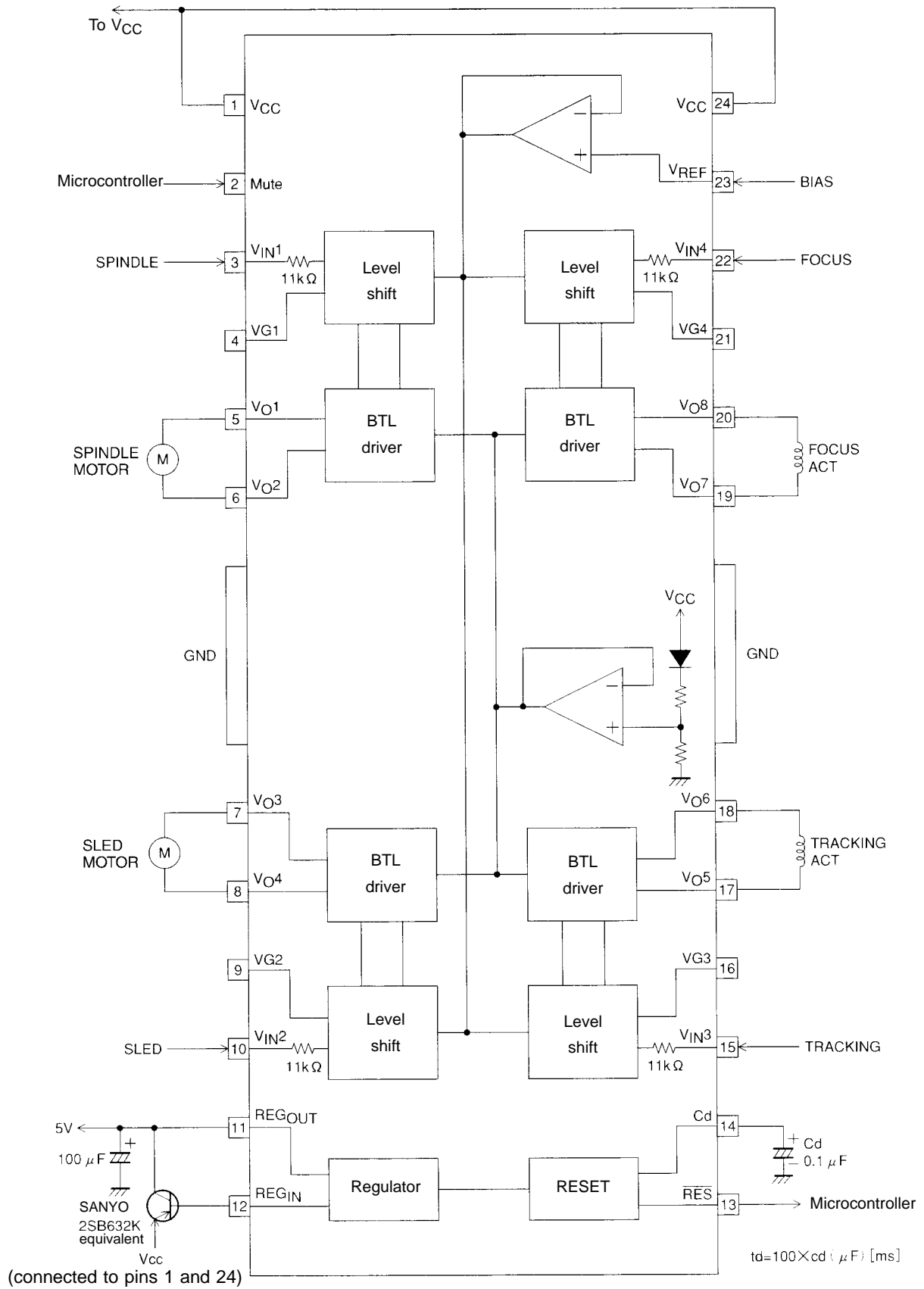
Block Diagram



A06415

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Sample Application Circuit



A06416

Note: Use a delay capacitor (Cd) whose capacitance does not change much according to the temperature.

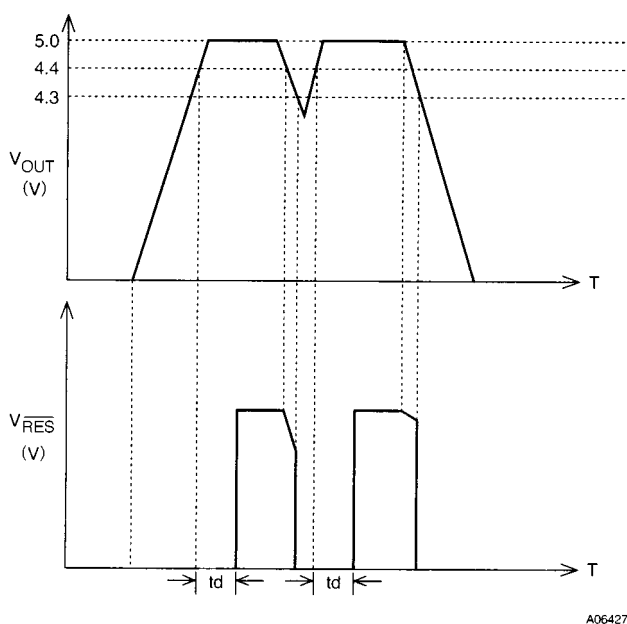
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Pin Functions

Pin No.	Pin Name	Equivalent Circuit	Description
1	V _{CC}		Power supply (shorted with pin 24)
2	Mute	<p style="text-align: right; font-size: small;">A06419</p>	ON/OFF control for all BTL AMP outputs
3 4 9 10 15 16 21 22	V _{IN1} VG1 VG2 V _{IN2} V _{IN3} VG3 VG4 V _{IN4}	<p style="text-align: right; font-size: small;">A06417</p>	BTL AMP 1 input BTL AMP 1 input (for gain control) BTL AMP 2 input (for gain control) BTL AMP 2 input BTL AMP 3 input BTL AMP 3 input (for gain control) BTL AMP 4 input (for gain control) BTL AMP 4 input
5 6 7 8 17 18 19 20	V _{O1} V _{O2} V _{O3} V _{O4} V _{O5} V _{O6} V _{O7} V _{O8}	<p style="text-align: right; font-size: small;">A06418</p>	BTL AMP 1 output (non-inverting side) BTL AMP 1 output (inverting side) BTL AMP 2 output (inverting side) BTL AMP 2 output (non-inverting side) BTL AMP 3 output (non-inverting side) BTL AMP 3 output (inverting side) BTL AMP 4 output (inverting side) BTL AMP 4 output (non-inverting side)
11	REG _{OUT}		Connection for collector of external transistor (PNP); 5 V supply output
12	REG _{IN}		Connection for base of external transistor (PNP)
13	$\overline{\text{RES}}$		Reset output
14	Cd		Reset output delay time setting (with capacitor)
23	V _{REF}		Reference voltage input for level shift circuit
24	V _{CC}		Power supply (shorted with pin 1)

Note: GND (minimum electrical potential) should be connected to the center frame of the pin.

Reset Operation



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