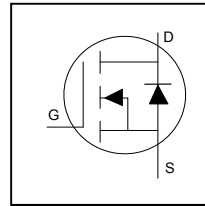


HEXFET® Power MOSFET

Application

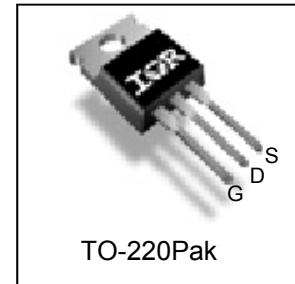
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



V_{DSS}	300V
R_{DS(on)} typ.	56mΩ
	69mΩ
I_D	38A

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB4137PbF	TO-220Pak	Tube	50	IRFB4137PbF

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	38	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	27	
I _{DM}	Pulsed Drain Current ①	152	
P _D @ T _C = 25°C	Maximum Power Dissipation	341	W
	Linear Derating Factor	2.3	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt③	8.9	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf-in (1.1 N·m)	

Avalanche Characteristics

E _{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	414	mJ
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Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case ③	—	0.44	°C/W
R _{θCS}	Case-to-Sink, Flat Greased Surface	0.50	—	
R _{θJA}	Junction-to-Ambient ⑦⑧	—	62	

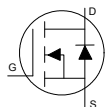
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	300	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.24	—	V/°C	Reference to 25°C, I _D = 3.5mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	56	69	mΩ	V _{GS} = 10V, I _D = 24A ④
V _{GS(th)}	Gate Threshold Voltage	3.0	—	5.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 300V, V _{GS} = 0V
		—	—	250		V _{DS} = 300V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
R _G	Gate Resistance	—	1.3	—	Ω	

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

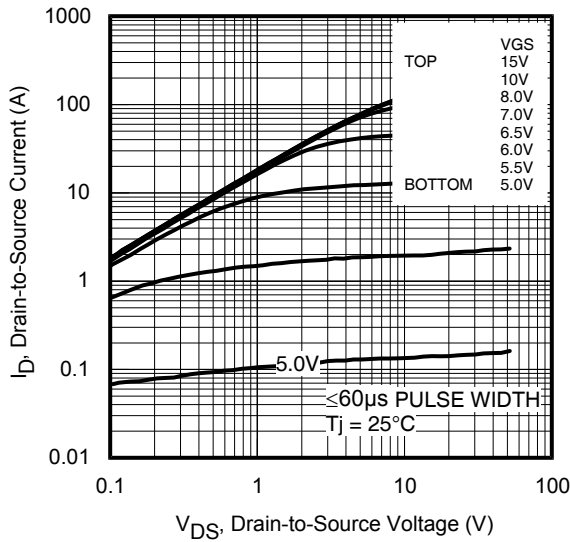
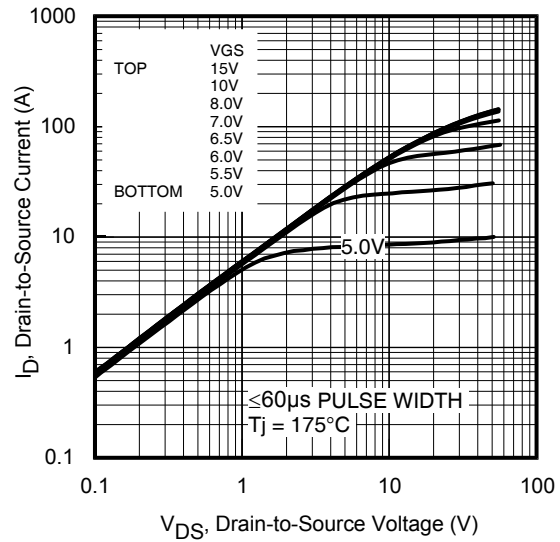
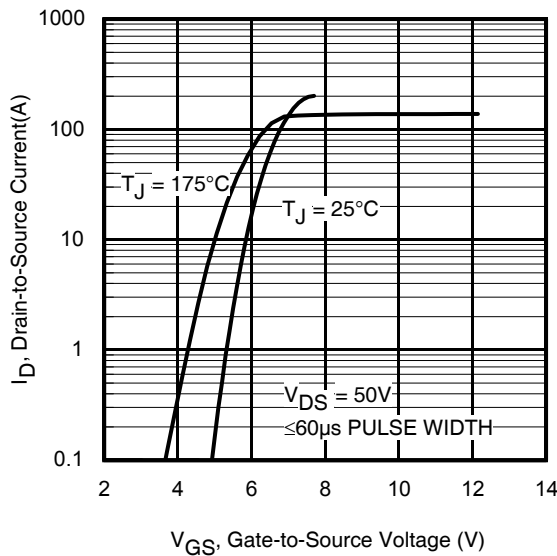
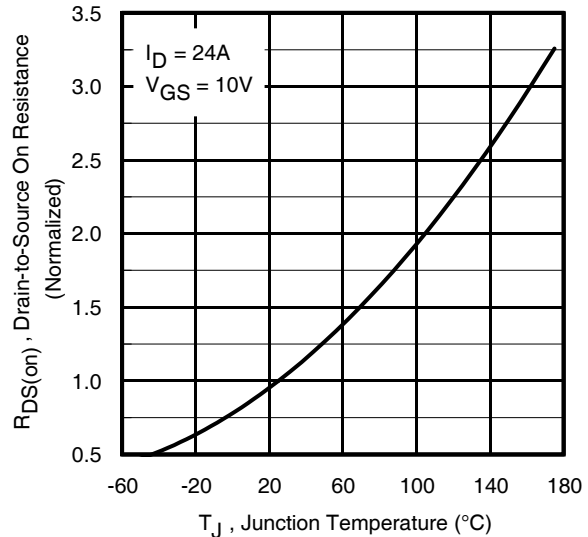
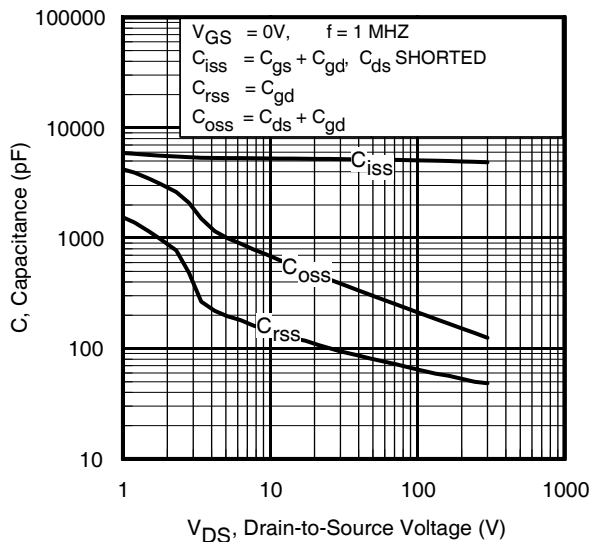
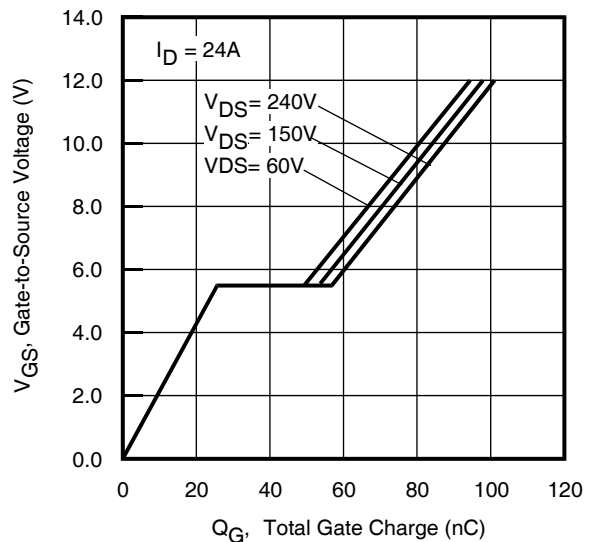
g _{fs}	Forward Transconductance	45	—	—	S	V _{DS} = 50V, I _D = 24A
Q _g	Total Gate Charge	—	83	125	nC	I _D = 24A
Q _{gs}	Gate-to-Source Charge	—	28	42		V _{DS} = 150V
Q _{gd}	Gate-to-Drain Charge	—	26	39		V _{GS} = 10V
t _{d(on)}	Turn-On Delay Time	—	18	—	ns	V _{DD} = 195V
t _r	Rise Time	—	23	—		I _D = 24A
t _{d(off)}	Turn-Off Delay Time	—	34	—		R _G = 2.2Ω
t _f	Fall Time	—	20	—		V _{GS} = 10V
C _{iss}	Input Capacitance	—	5168	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	300	—		V _{DS} = 50V
C _{rss}	Reverse Transfer Capacitance	—	77	—		f = 1.0MHz
C _{oss eff.(ER)}	Effective Output Capacitance (Energy Related)	—	196	—		V _{GS} = 0V, V _{DS} = 0V to 240V ^⑥
C _{oss eff.(TR)}	Output Capacitance (Time Related)	—	265	—		See Fig.11
						V _{GS} = 0V, V _{DS} = 0V to 240V ^⑤

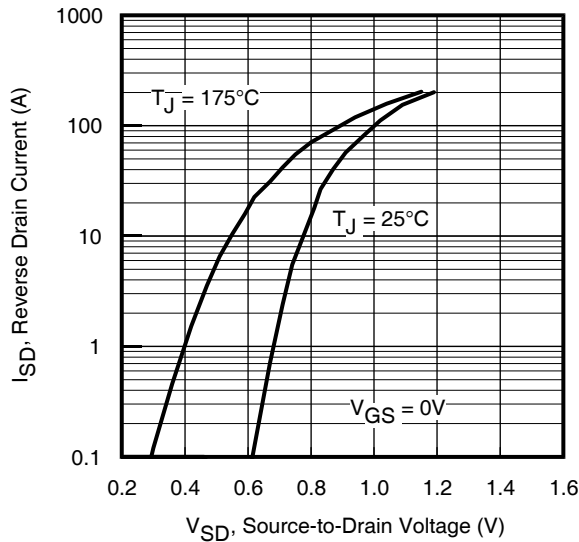
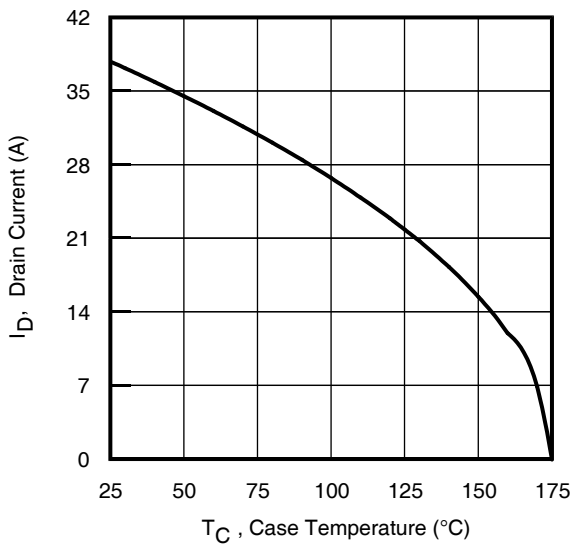
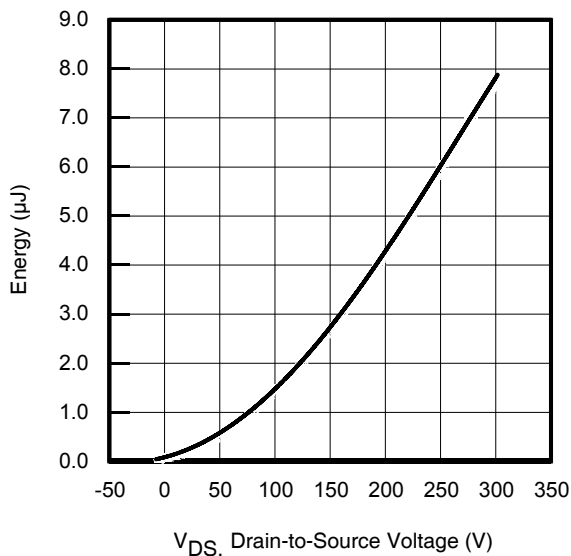
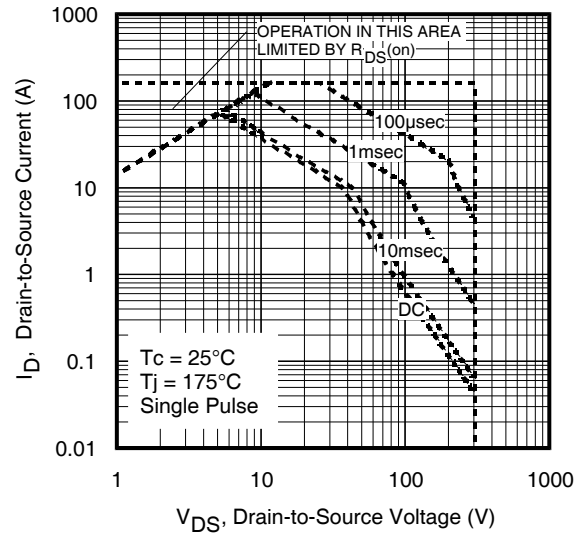
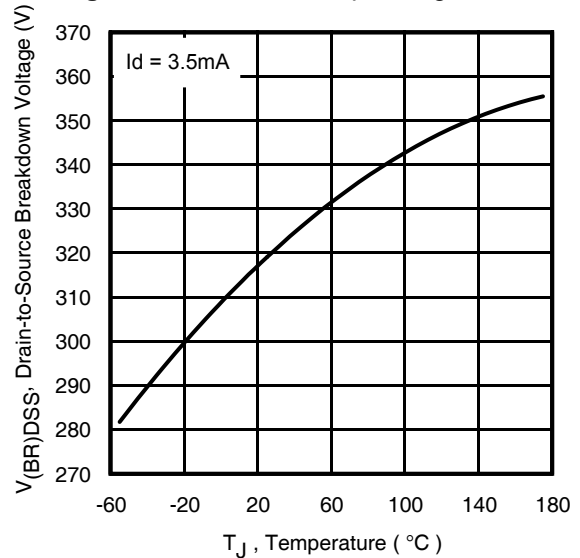
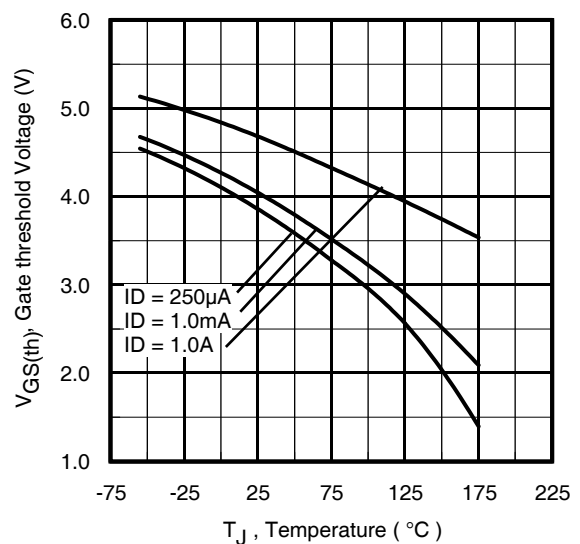
Diode Characteristics

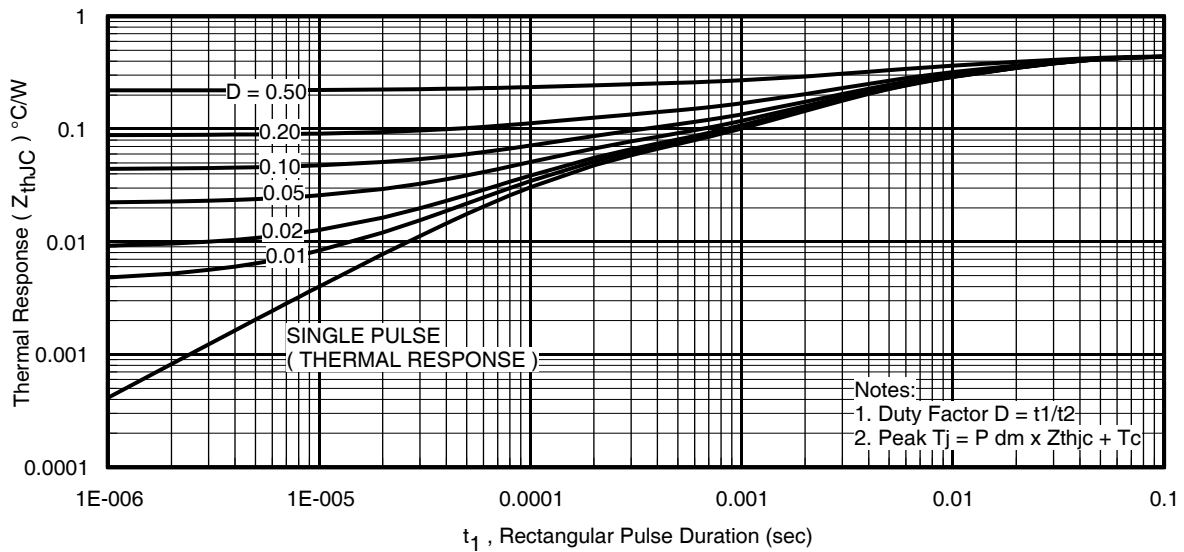
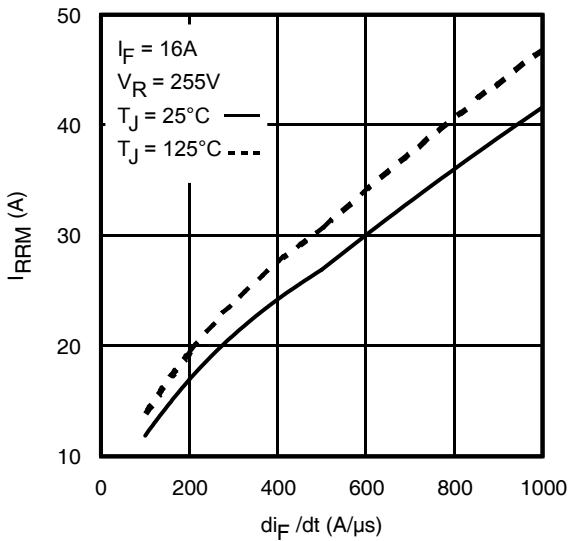
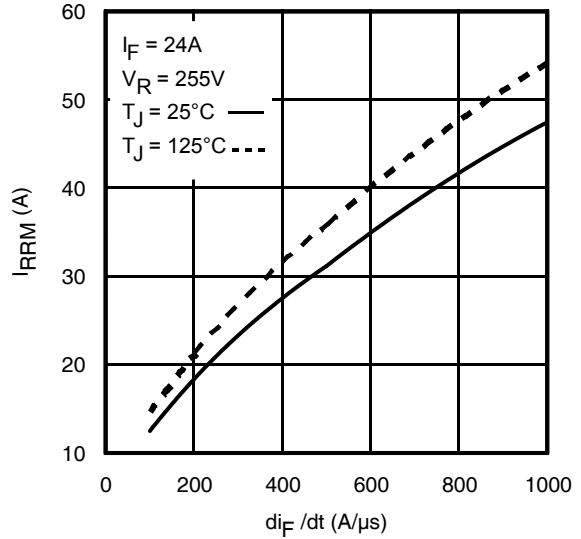
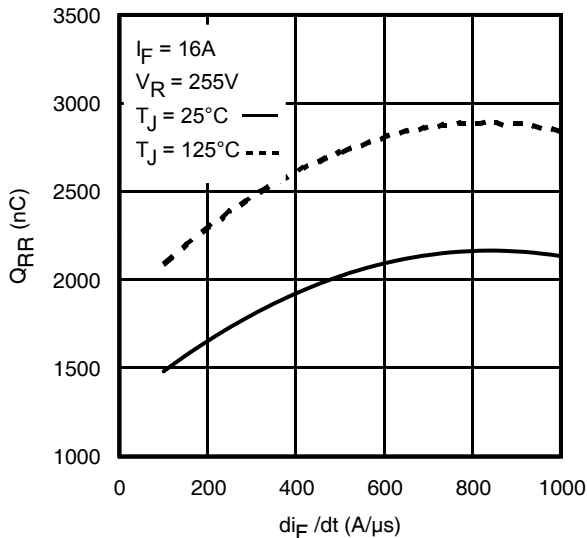
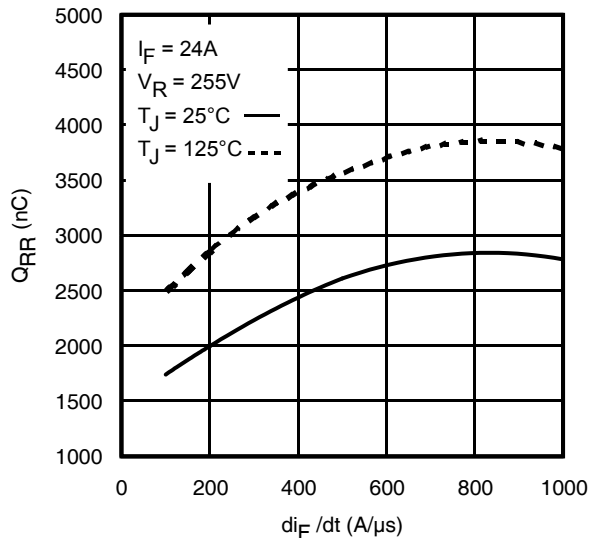
	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode) ①	—	—	38	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	152		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 24A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	302	—	ns	T _J = 25°C V _{DD} = 255V
		—	379	—		T _J = 125°C I _F = 24A,
Q _{rr}	Reverse Recovery Charge	—	1739	—	nC	T _J = 25°C di/dt = 100A/μs ④
		—	2497	—		T _J = 125°C
I _{RSM}	Reverse Recovery Current	—	13	—	A	T _J = 25°C

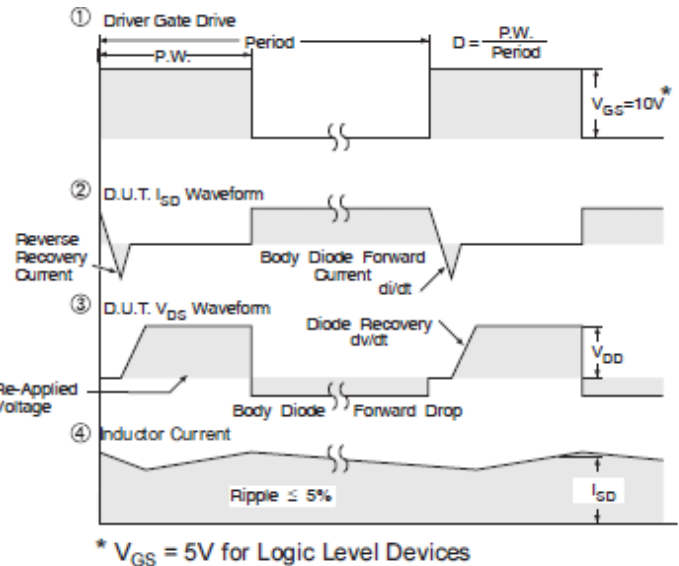
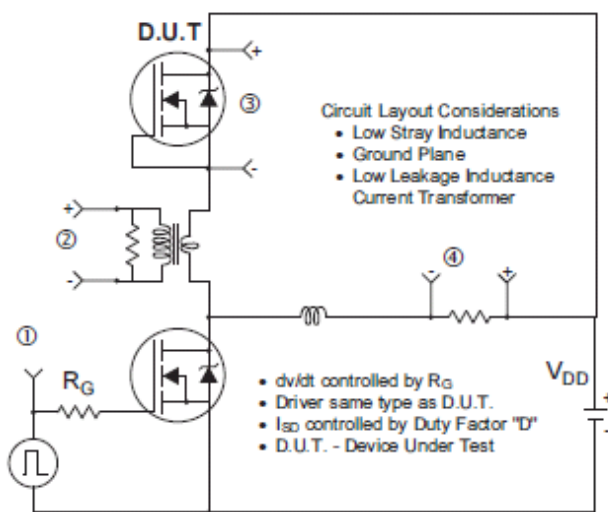
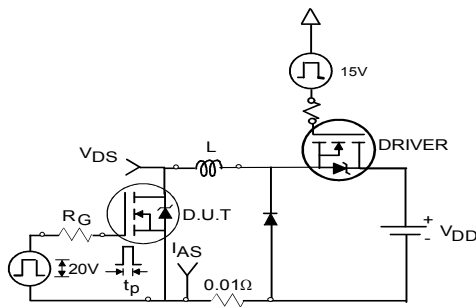
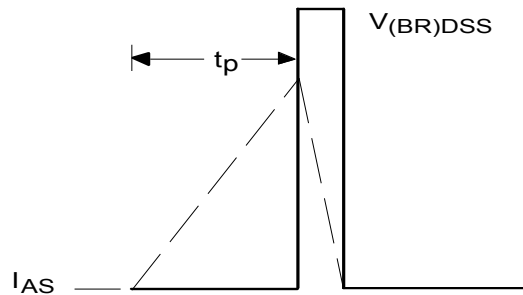
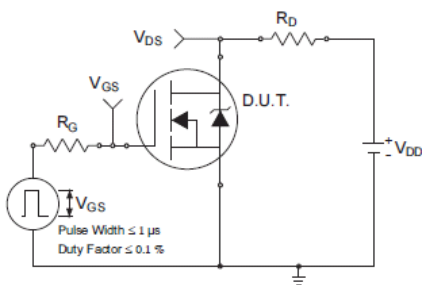
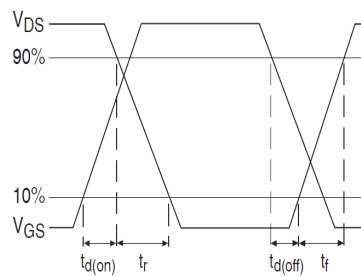
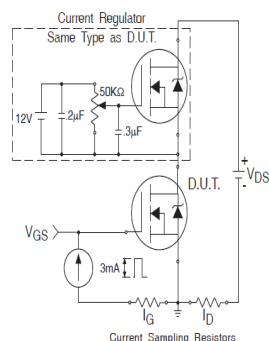
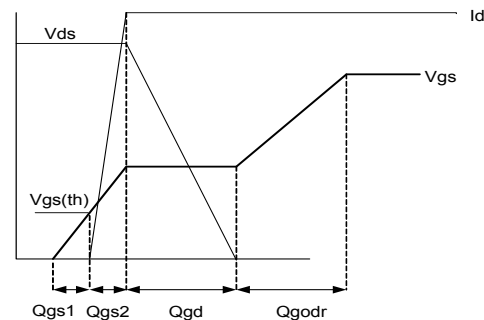
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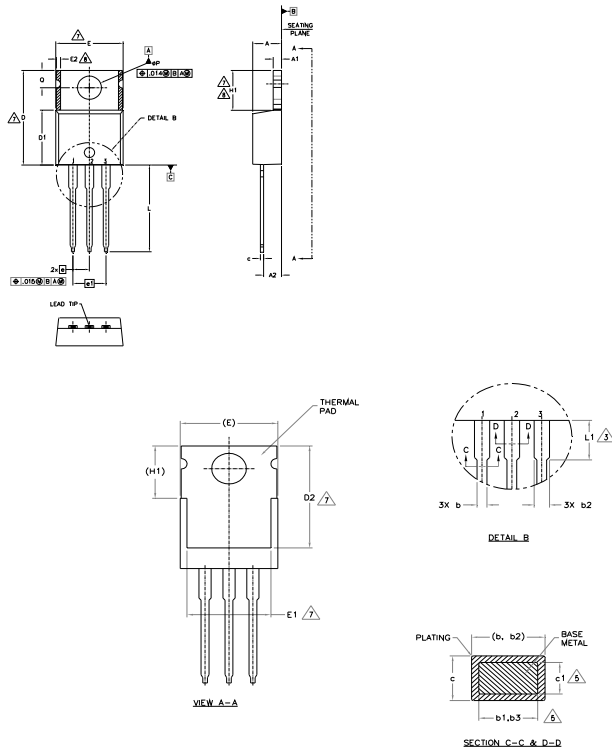
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Recommended max EAS limit, starting T_J = 25°C, L = 1.56mH, R_G = 50Ω, I_{AS} = 24A, V_{GS} = 10V.
- ③ I_{SD} ≤ 24A, di/dt ≤ 1771A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C_{oss eff. (TR)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑥ C_{oss eff. (ER)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑧ R_θ is measured at T_J approximately 90°C


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 11. Typical C_{oss} Stored Energy

Fig 8. Maximum Safe Operating Area

Fig 10. Drain-to-Source Breakdown Voltage

Fig 12. Threshold Voltage vs. Temperature


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig 14. Typical Recovery Current vs. di_f/dt

Fig 15. Typical Recovery Current vs. di_f/dt

Fig 16. Typical Stored Charge vs. di_f/dt

Fig 17. Typical Stored Charge vs. di_f/dt


Fig 18. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

Fig 19a. Unclamped Inductive Test Circuit

Fig 19b. Unclamped Inductive Waveforms

Fig 20a. Switching Time Test Circuit

Fig 20b. Switching Time Waveforms

Fig 21a. Gate Charge Test Circuit

Fig 21b. Gate Charge Waveform

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))


- NOTES:
- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
 - 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
 - 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
 - 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
 - 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
 - 6.- CONTROLLING DIMENSION : INCHES.
 - 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
 - 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
 - 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

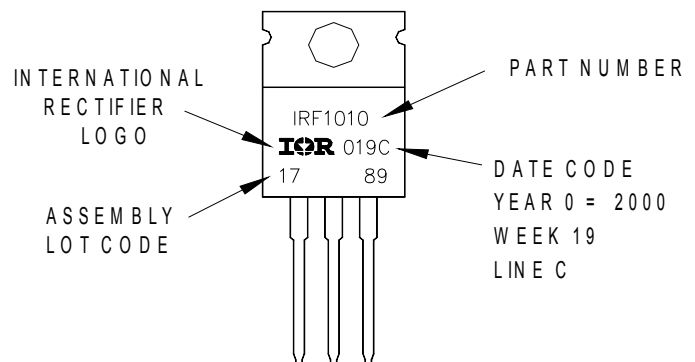
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

- LEAD ASSIGNMENTS
- HEXFET
- 1.- GATE
 - 2.- DRAIN
 - 3.- SOURCE
- IGBTs, CoPACK
- 1.- GATE
 - 2.- COLLECTOR
 - 3.- EMITTER
- DIODES
- 1.- ANODE
 - 2.- CATHODE
 - 3.- ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 2000
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information[†]

Qualification Level	Industrial (per JEDEC JESD47F) ^{††}	
Moisture Sensitivity Level	TO-220	N/A
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier’s web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

Data and specifications subject to change without notice.



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