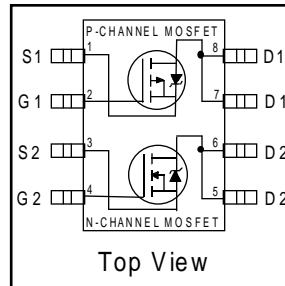


- Generation V Technology
- Ultra Low On-Resistance
- Dual N and P Channel MOSFET
- Very Small SOIC Package
- Low Profile (<1.1mm)
- Available in Tape & Reel
- Fast Switching

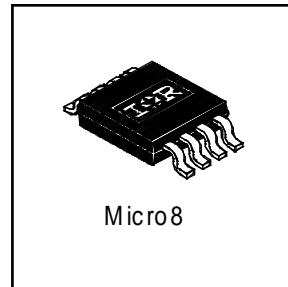
Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The new Micro8 package, with half the footprint area of the standard SO-8, provides the smallest footprint available in an SOIC outline. This makes the Micro8 an ideal device for applications where printed circuit board space is at a premium. The low profile (<1.1mm) of the Micro8 will allow it to fit easily into extremely thin application environments such as portable electronics and PCMCIA cards.



	N-Ch	P-Ch
V_{DSS}	30V	-30V
$R_{DS(on)}$	0.135 Ω	0.27 Ω



Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
I_D @ $T_A = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	2.4	-1.7	A
I_D @ $T_A = 70^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	1.9	-1.4	
I_{DM}	Pulsed Drain Current ①	14	-9.6	
P_D @ $T_A = 25^\circ\text{C}$	Power Dissipation	1.25		W
	Linear Derating Factor	10		mW/°C
V_{GS}	Gate-to-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	-5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④	—	100	°C/W

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Description		Min.	Typ.	Max.	Unit	Conditions	
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$	
		P-Ch	-30	—	—		$V_{GS} = 0V, I_D = -250\mu A$	
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.059	—	$V/^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$	
		P-Ch	—	-0.024	—		Reference to $25^\circ\text{C}, I_D = -1\text{mA}$	
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	N-Ch	—	—	0.135	Ω	$V_{GS} = 10V, I_D = 1.7A$ ③	
			—	—	0.222		$V_{GS} = 4.5V, I_D = 0.85A$ ③	
		P-Ch	—	—	0.27		$V_{GS} = -10V, I_D = -1.2A$ ③	
			—	—	0.45		$V_{GS} = -4.5V, I_D = -0.60A$ ③	
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$	
		P-Ch	-1.0	—	—		$V_{DS} = V_{GS}, I_D = -250\mu A$	
g_{fs}	Forward Transconductance	N-Ch	1.9	—	—	S	$V_{DS} = 10V, I_D = 0.85A$ ③	
		P-Ch	0.94	—	—		$V_{DS} = -10V, I_D = -0.60A$ ③	
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$	
		P-Ch	—	—	-1.0		$V_{DS} = -24V, V_{GS} = 0V$	
		N-Ch	—	—	25		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$	
		P-Ch	—	—	-25		$V_{DS} = -24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$	
I_{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	± 100	nA	$V_{GS} = \pm 20V$	
Q_g	Total Gate Charge	N-Ch	—	7.8	12	nC	N-Channel	
		P-Ch	—	7.3	11		$I_D = 1.7A, V_{DS} = 24V, V_{GS} = 10V$ ③	
Q_{gs}	Gate-to-Source Charge	N-Ch	—	1.2	1.8	nC	P-Channel	
		P-Ch	—	1.1	1.6		$I_D = -1.2A, V_{DS} = -24V, V_{GS} = -10V$ ③	
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	2.5	3.8	nC	P-Channel	
		P-Ch	—	2.4	3.7		$I_D = -1.2A, V_{DS} = -24V, V_{GS} = -10V$ ③	
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	4.7	—	ns	N-Channel	
t_r	Rise Time	P-Ch	—	11	—		$V_{DD} = 15V, I_D = 1.7A, R_G = 6.1\Omega, R_D = 8.7\Omega$ ③	
		N-Ch	—	10	—		P-Channel	
$t_{d(off)}$	Turn-Off Delay Time	P-Ch	—	15	—		$V_{DD} = -15V, I_D = -1.2A, R_G = 6.2\Omega, R_D = 12\Omega$ ③	
		N-Ch	—	12	—	P-Channel		
t_f	Fall Time	P-Ch	—	36	—	N-Channel		
		N-Ch	—	5.3	—	P-Channel		
C_{iss}	Input Capacitance	P-Ch	—	28	—	pF	N-Channel	
		N-Ch	—	210	—		$V_{GS} = 0V, V_{DS} = 25V, f = 1.0\text{MHz}$ ③	
C_{oss}	Output Capacitance	P-Ch	—	180	—		P-Channel	
		N-Ch	—	80	—		$V_{GS} = 0V, V_{DS} = -25V, f = 1.0\text{MHz}$ ③	
C_{riss}	Reverse Transfer Capacitance	P-Ch	—	88	—	N-Channel		
		N-Ch	—	32	—	P-Channel		
C_{riss}	Reverse Transfer Capacitance	P-Ch	—	40	—	N-Channel		
		N-Ch	—	40	—	P-Channel		

Source-Drain Ratings and Characteristics

Parameter	Description		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	—	—	1.25	A	
		P-Ch	—	—	-1.25		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	14	A	
		P-Ch	—	—	-9.6		
V_{SD}	Diode Forward Voltage	N-Ch	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 1.7A, V_{GS} = 0V$ ③
		P-Ch	—	—	-1.2		$T_J = 25^\circ\text{C}, I_S = -1.2A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	N-Ch	—	40	60	ns	N-Channel
		P-Ch	—	40	60		$T_J = 25^\circ\text{C}, I_F = 1.7A, di/dt = 100A/\mu s$ ③
Q_{rr}	Reverse Recovery Charge	N-Ch	—	48	72	nC	P-Channel
		P-Ch	—	45	67		$T_J = 25^\circ\text{C}, I_F = -1.2A, di/dt = 100A/\mu s$ ③

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 21)
- ② N-Channel $I_{SD} \leq 1.7A, di/dt \leq 120A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
P-Channel $I_{SD} \leq -1.2A, di/dt \leq 160A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
- ③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ④ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.

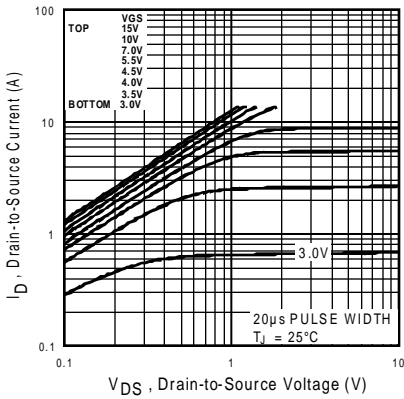


Fig 1. Typical Output Characteristics

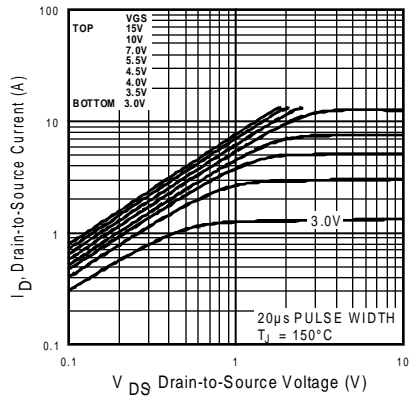


Fig 2. Typical Output Characteristics

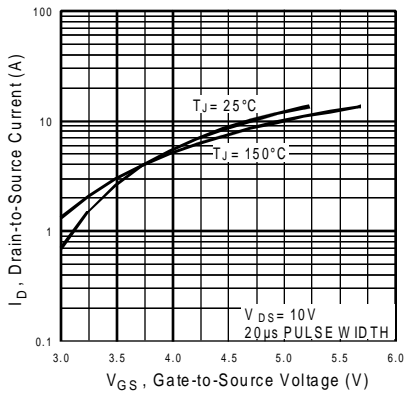


Fig 3. Typical Transfer Characteristics

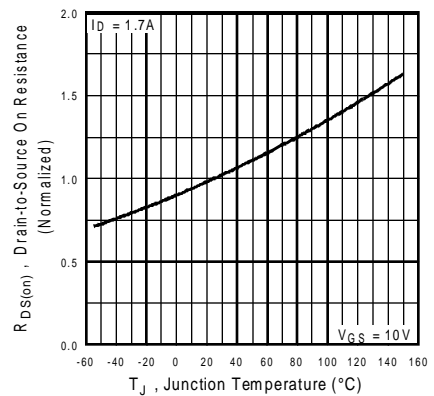


Fig 4. Normalized On-Resistance Vs. Temperature

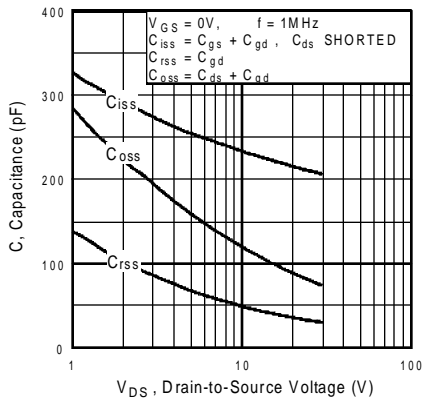


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

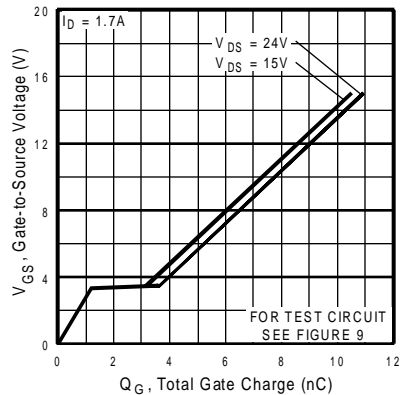


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

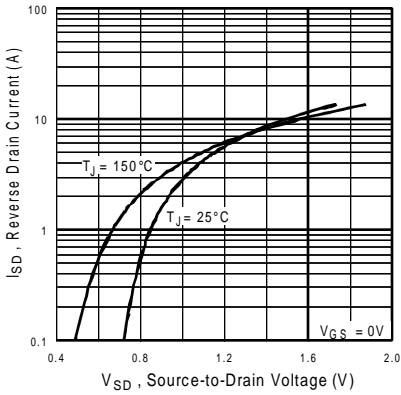


Fig 7. Typical Source-Drain Diode Forward Voltage

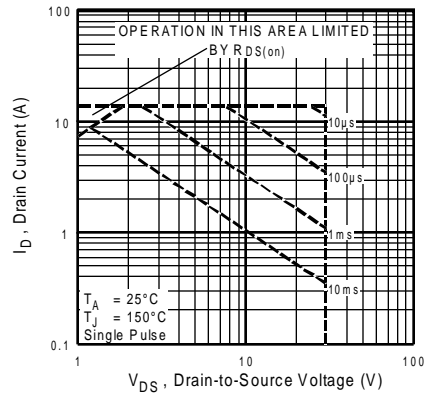


Fig 8. Maximum Safe Operating Area

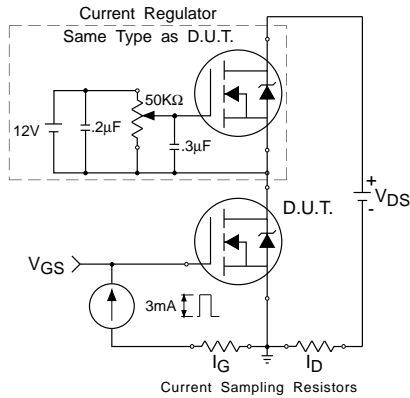


Fig 9a. Gate Charge Test Circuit

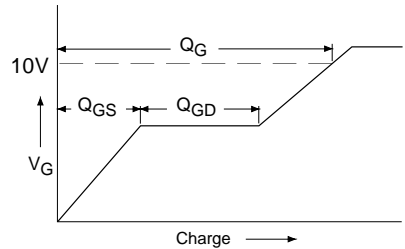


Fig 9b. Basic Gate Charge Waveform

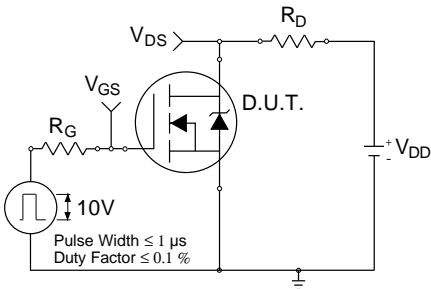


Fig 10a. Switching Time Test Circuit

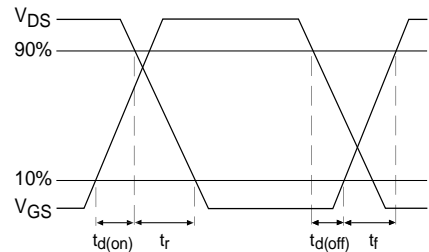


Fig 10b. Switching Time Waveforms

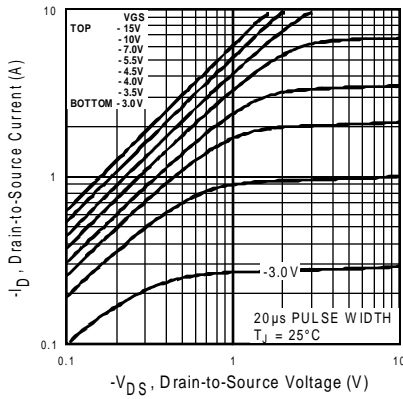


Fig 11. Typical Output Characteristics

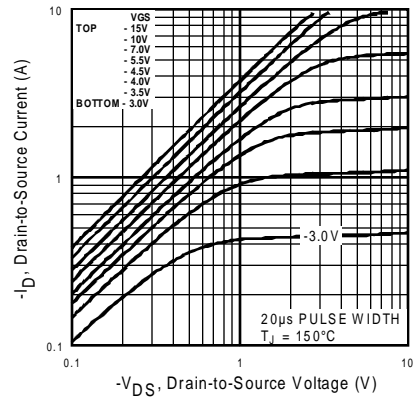


Fig 12. Typical Output Characteristics

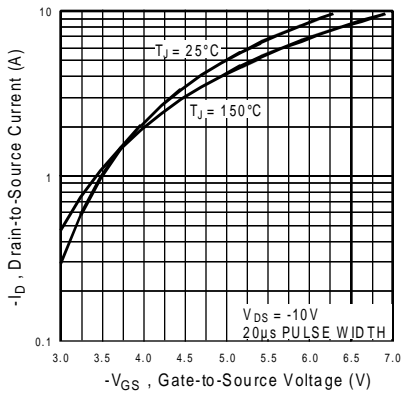


Fig 13. Typical Transfer Characteristics

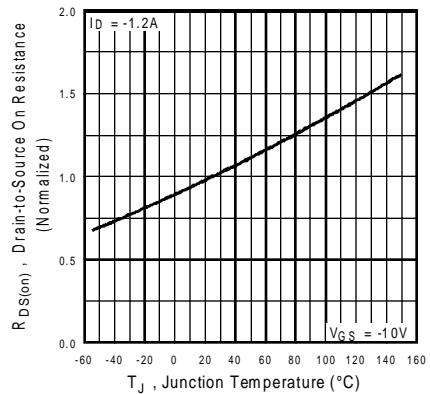


Fig 14. Normalized On-Resistance Vs. Temperature

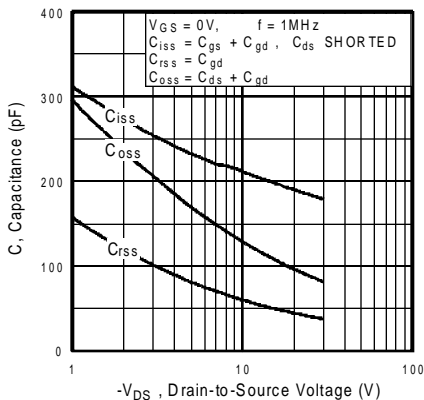


Fig 15. Typical Capacitance Vs. Drain-to-Source Voltage

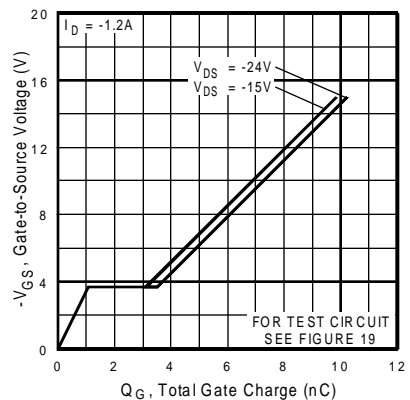


Fig 16. Typical Gate Charge Vs. Gate-to-Source Voltage

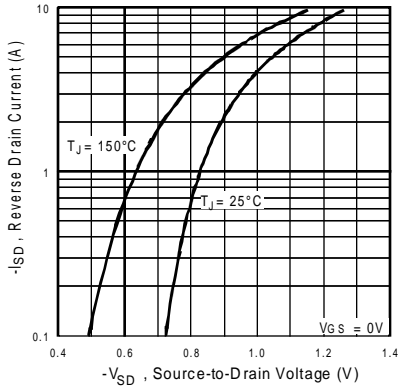


Fig 17. Typical Source-Drain Diode Forward Voltage

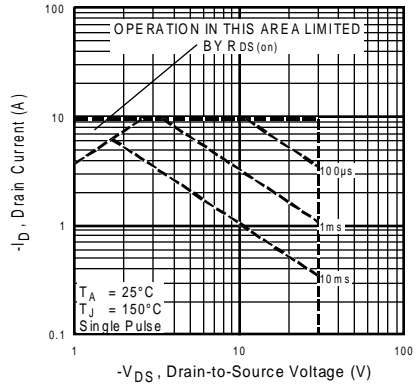


Fig 18. Maximum Safe Operating Area

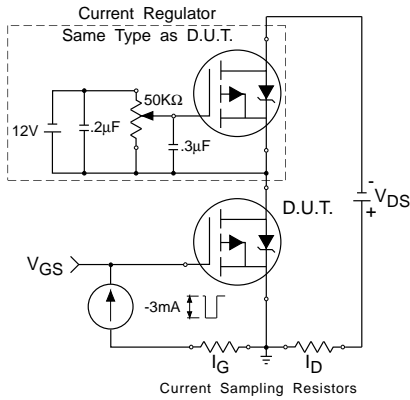


Fig 19a. Gate Charge Test Circuit

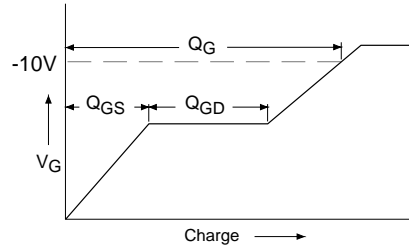


Fig 19b. Basic Gate Charge Waveform

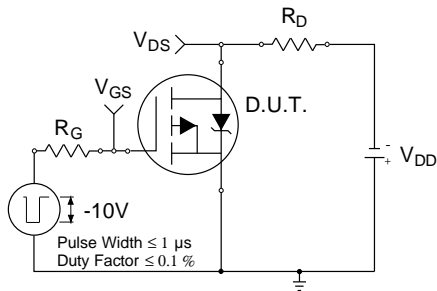


Fig 20a. Switching Time Test Circuit

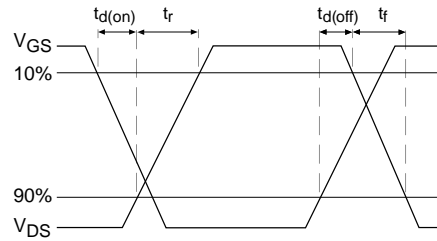


Fig 20b. Switching Time Waveforms

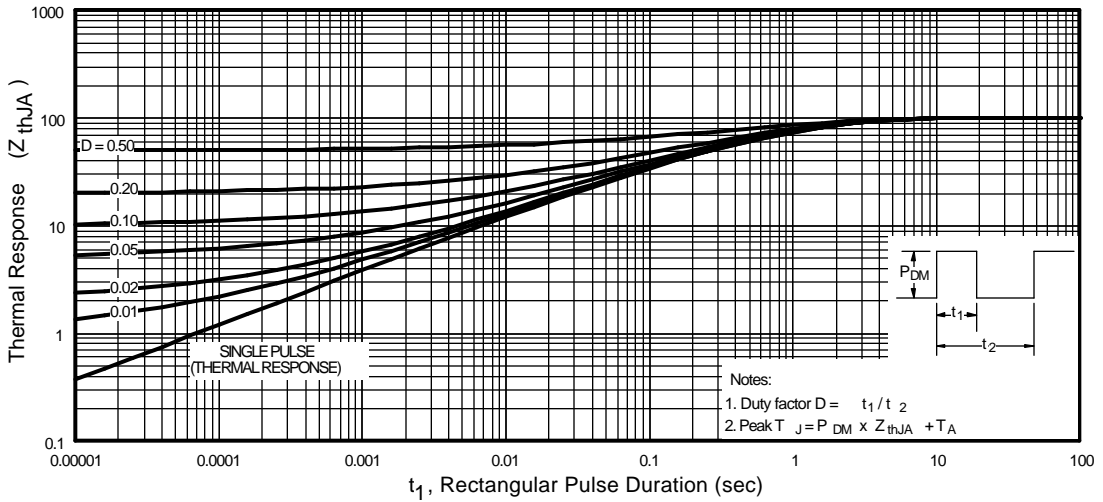
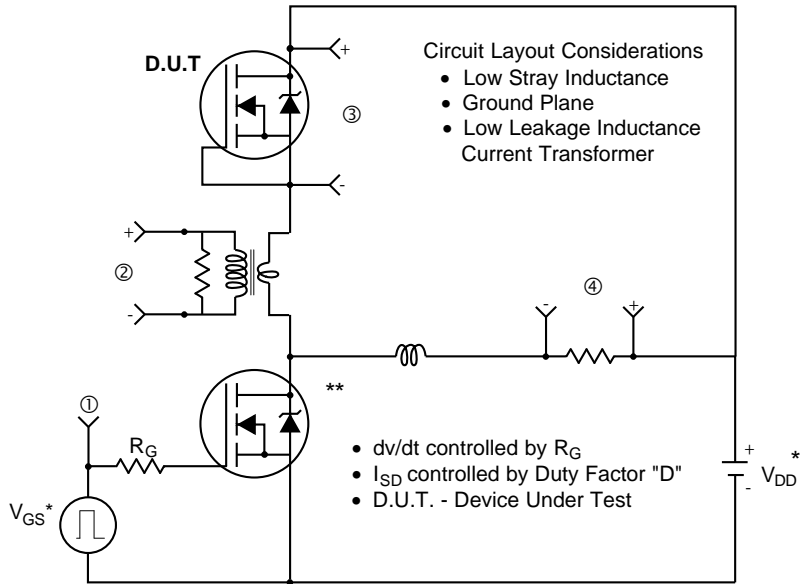


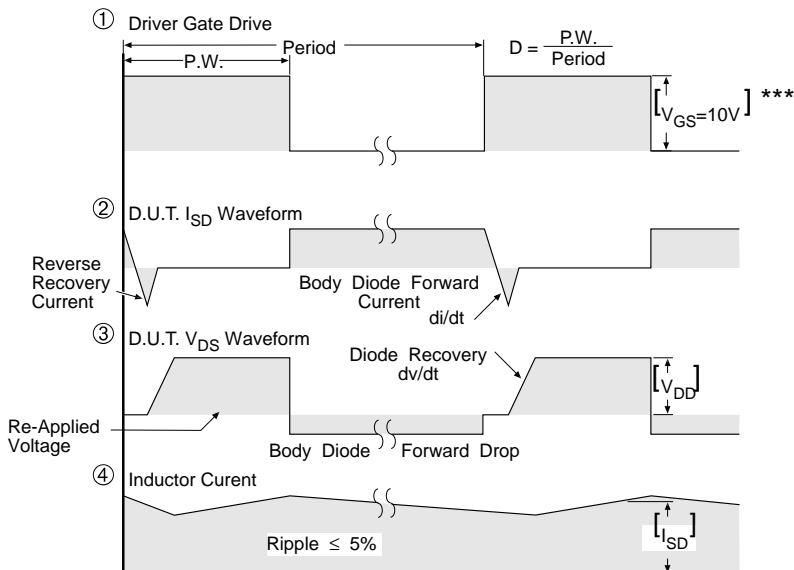
Fig 21. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements



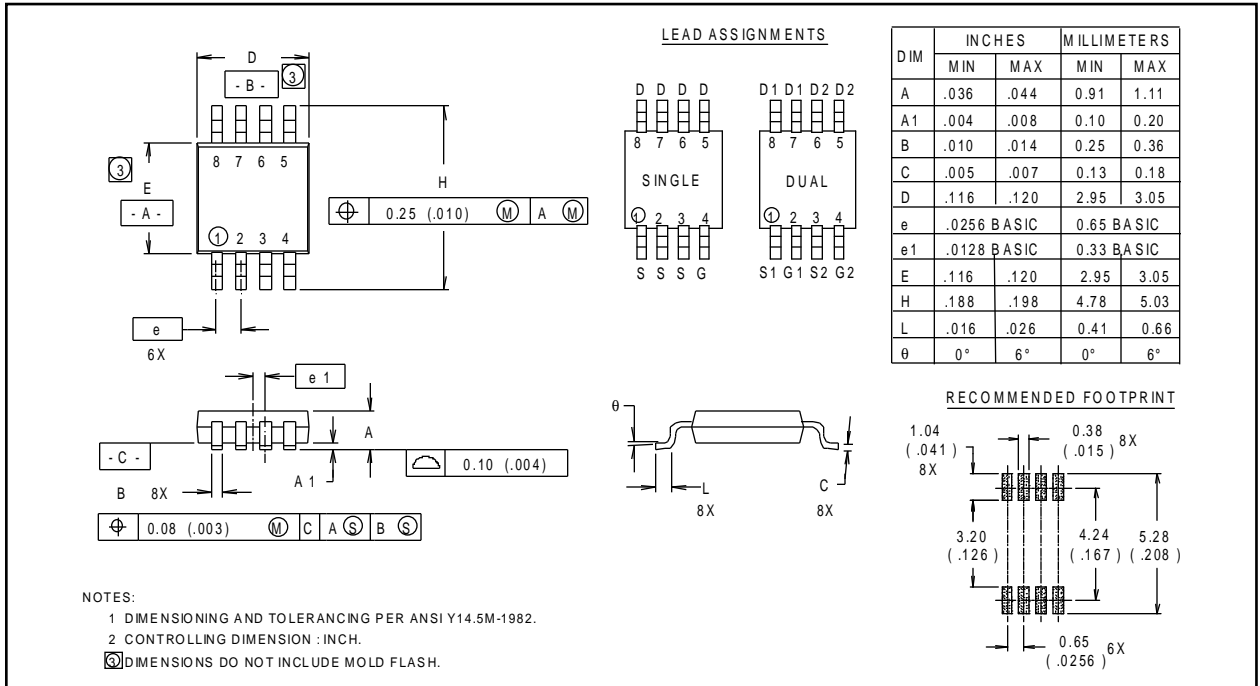
*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 22. For N and P Channel HEXFETS

Package Outline

Micro8 Outline

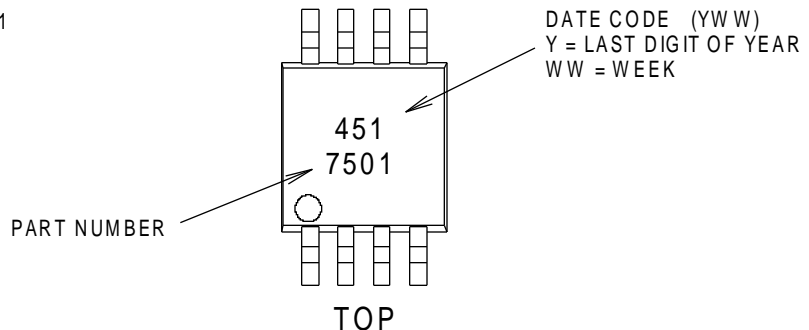
Dimensions are shown in millimeters (inches)



Part Marking Information

Micro8

EXAMPLE : THIS IS AN IRF7501



Tape & Reel Information

Micro8

Dimensions are shown in millimeters (inches)

