

SMPS MOSFET

IRF740AS/L

HEXFET® Power MOSFET

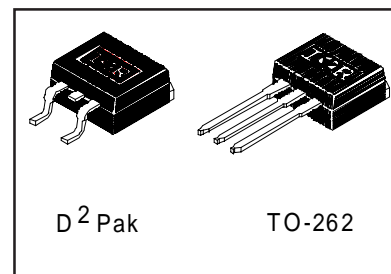
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High speed power switching

V _{DSS}	R _{ds(on)} max	I _D
400V	0.55Ω	10A

Benefits

- Low Gate Charge Q_g results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss specified (See AN 1001)



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V ^⑥	10	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V ^⑥	6.3	
I _{DM}	Pulsed Drain Current ^① ⑥	40	
P _D @ T _A = 25°C	Power Dissipation	3.1	W
P _D @ T _C = 25°C	Power Dissipation	125	
	Linear Derating Factor	1.0	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ^③ ⑥	5.9	V/ns
T _J	Operating Junction and	-55 to + 150	
T _{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Typical SMPS Topologies:

- Single transistor Flyback Xfmr. Reset
- Single Transistor Forward Xfmr. Reset
(Both for US Line Input only)

Notes ^① through ^⑤ are on page 10

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	400	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.48	—		$V/^\circ\text{C}$ Reference to $25^\circ\text{C}, I_D = 1mA$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.55	Ω	$V_{GS} = 10V, I_D = 6.0A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 400V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 320V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	4.9	—	—	S	$V_{DS} = 50V, I_D = 6.0A$ ⑥
Q_g	Total Gate Charge	—	—	36	nC	$I_D = 10A$ $V_{DS} = 320V$ $V_{GS} = 10V$, See Fig. 6 and 13 ④ ⑥
Q_{gs}	Gate-to-Source Charge	—	—	9.9		
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	16		
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	$V_{DD} = 200V$ $I_D = 10A$ $R_G = 10\Omega$ $R_D = 19.5\Omega$, See Fig. 10 ④ ⑥
t_r	Rise Time	—	35	—		
$t_{d(off)}$	Turn-Off Delay Time	—	24	—		
t_f	Fall Time	—	22	—		
C_{iss}	Input Capacitance	—	1030	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0MHz$, See Fig. 5 ⑥
C_{oss}	Output Capacitance	—	170	—		
C_{riss}	Reverse Transfer Capacitance	—	7.7	—		
C_{oss}	Output Capacitance	—	1490	—		
C_{oss}	Output Capacitance	—	52	—		
$C_{oss\ eff.}$	Effective Output Capacitance	—	61	—		

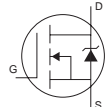
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ② ⑥	—	630	mJ
I_{AR}	Avalanche Current ①	—	10	A
E_{AR}	Repetitive Avalanche Energy ①	—	12.5	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.0	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)*	—	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	10	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	40		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	$T_J = 25^\circ\text{C}, I_S = 10A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	240	360	ns	$T_J = 25^\circ\text{C}, I_F = 10A$
Q_{rr}	Reverse Recovery Charge	—	1.9	2.9	μC	$di/dt = 100A/\mu\text{s}$ ④ ⑥
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

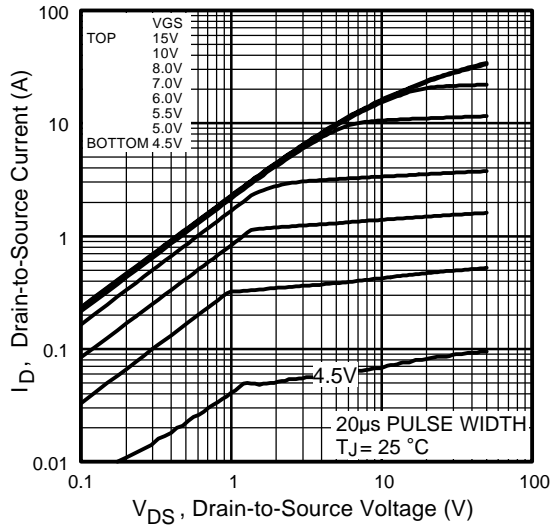


Fig 1. Typical Output Characteristics

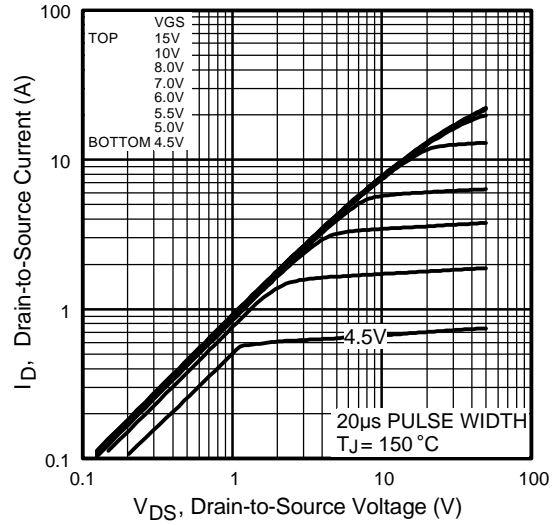


Fig 2. Typical Output Characteristics

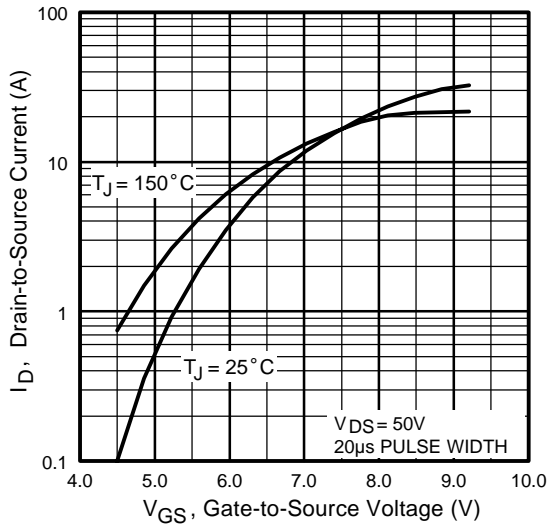


Fig 3. Typical Transfer Characteristics

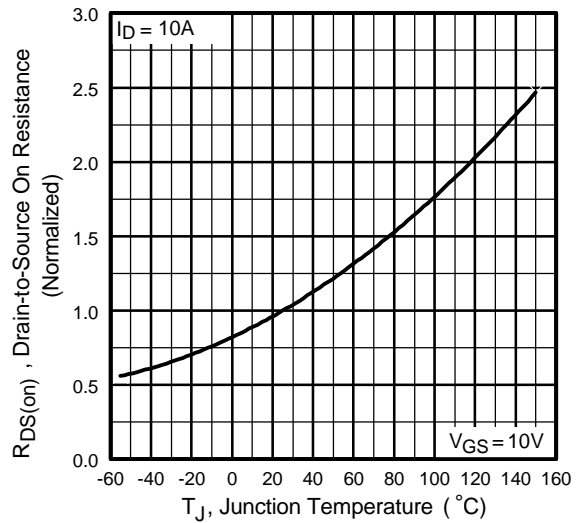


Fig 4. Normalized On-Resistance Vs. Temperature

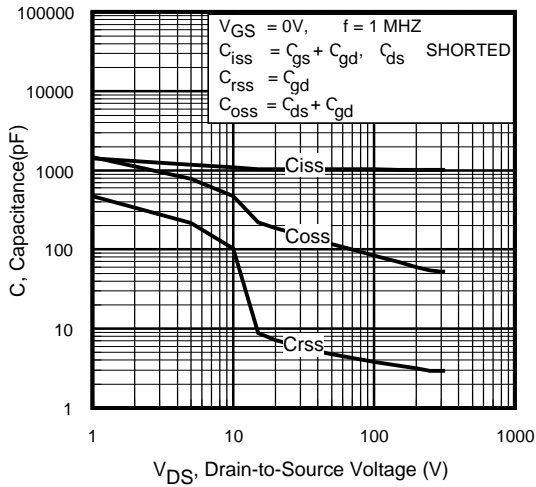


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

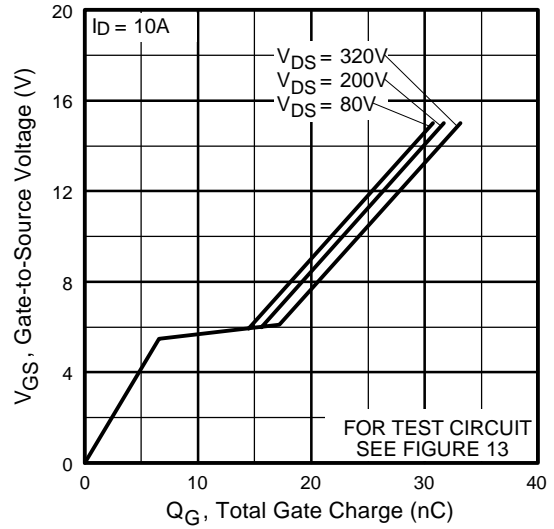


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

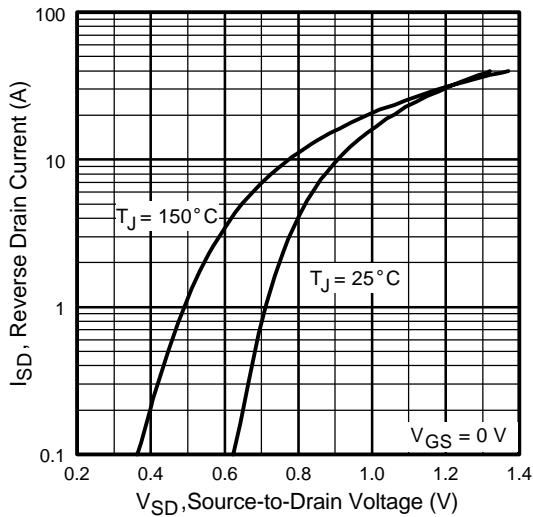


Fig 7. Typical Source-Drain Diode Forward Voltage

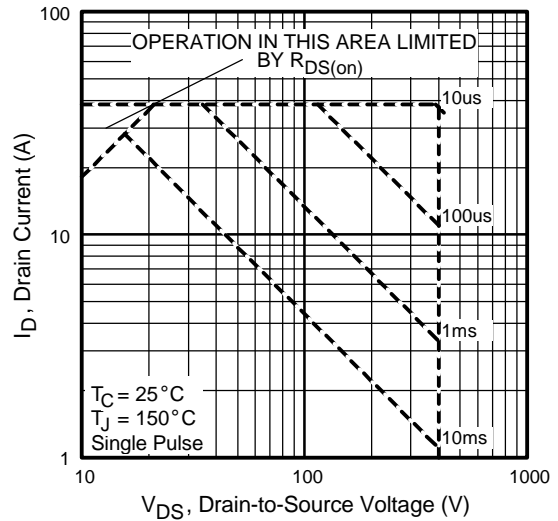


Fig 8. Maximum Safe Operating Area

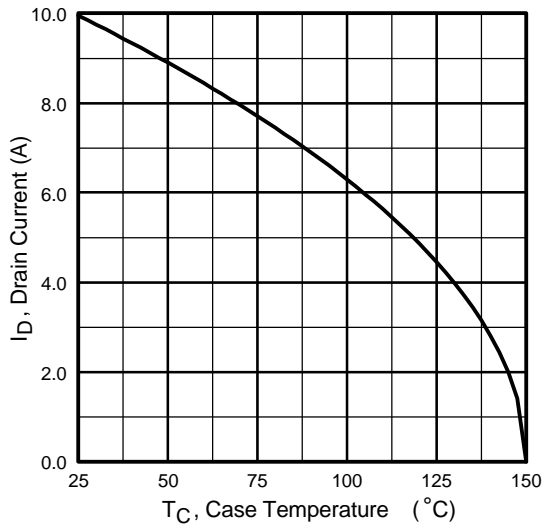


Fig 9. Maximum Drain Current Vs. Case Temperature



Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

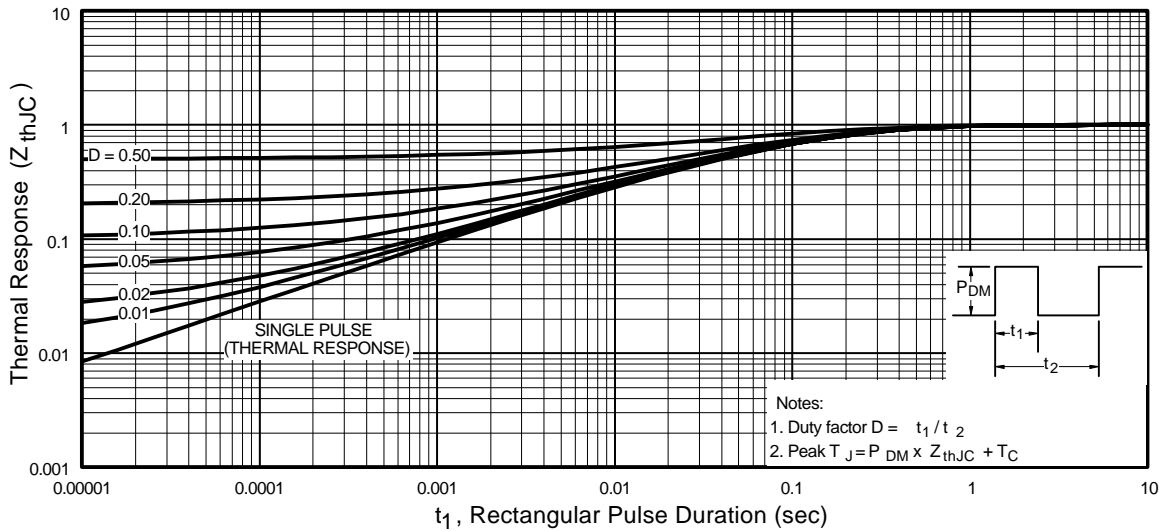


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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Fig 12a. Unclamped Inductive Test Circuit



Fig 12b. Unclamped Inductive Waveforms



Fig 13a. Basic Gate Charge Waveform



Fig 13b. Gate Charge Test Circuit

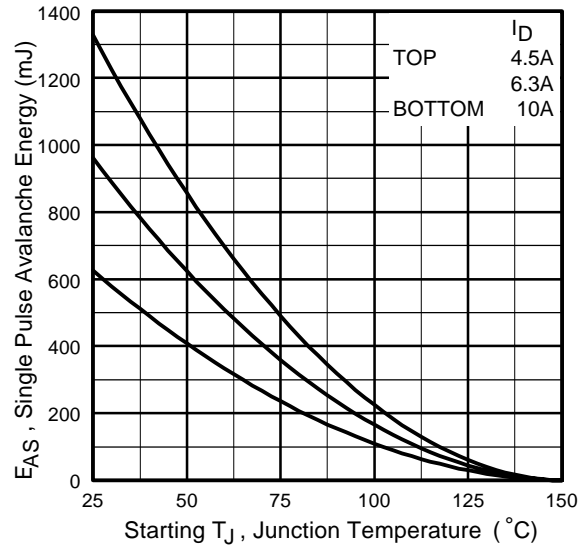


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

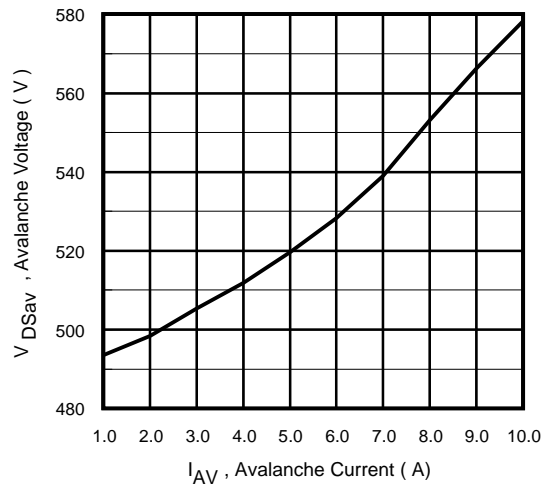


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

Peak Diode Recovery dv/dt Test Circuit



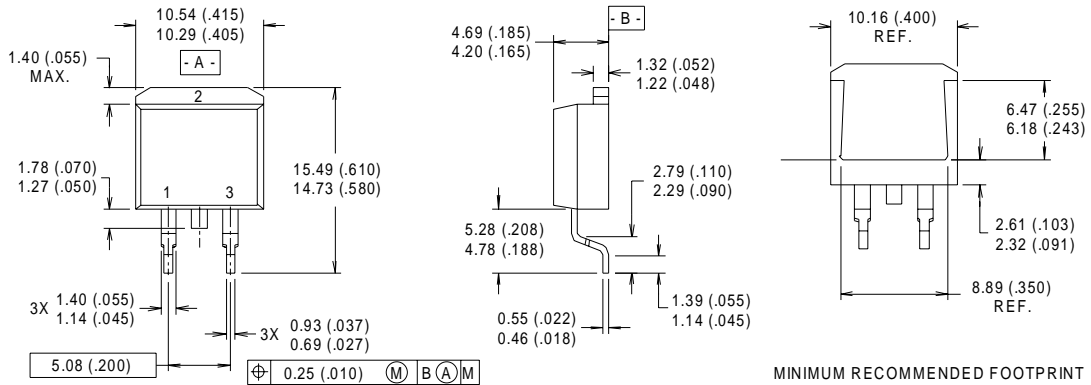
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

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D²Pak Package Outline



NOTES:

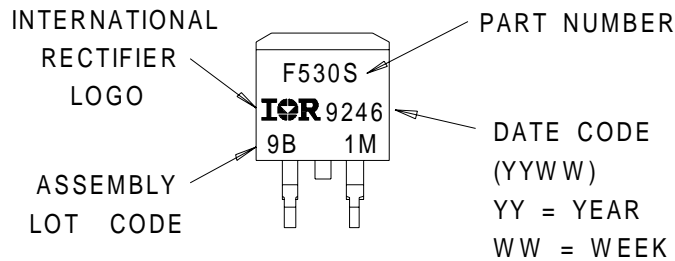
- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANS Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

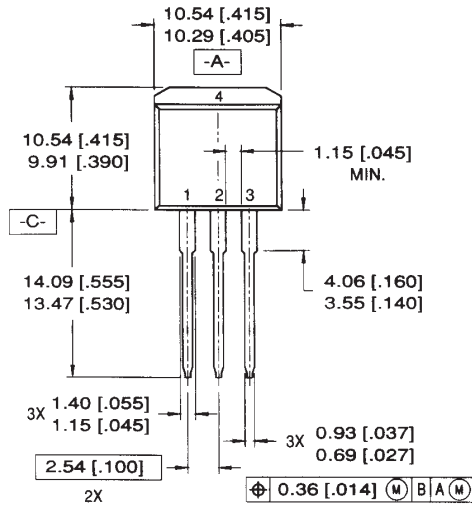
Part Marking Information

D²Pak



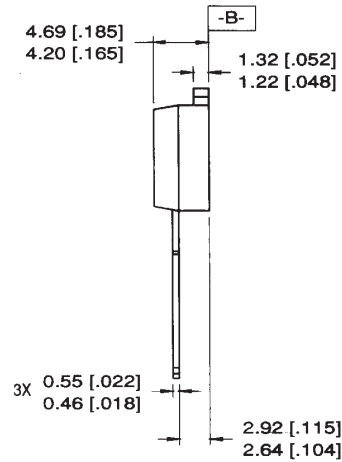
Package Outline

TO-262 Outline



LEAD ASSIGNMENTS

- 1 = GATE 3 = SOURCE
- 2 = DRAIN 4 = DRAIN



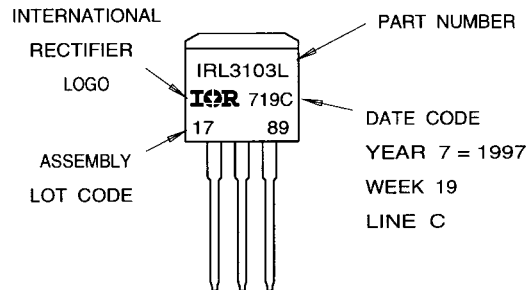
NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

Part Marking Information

TO-262

EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"

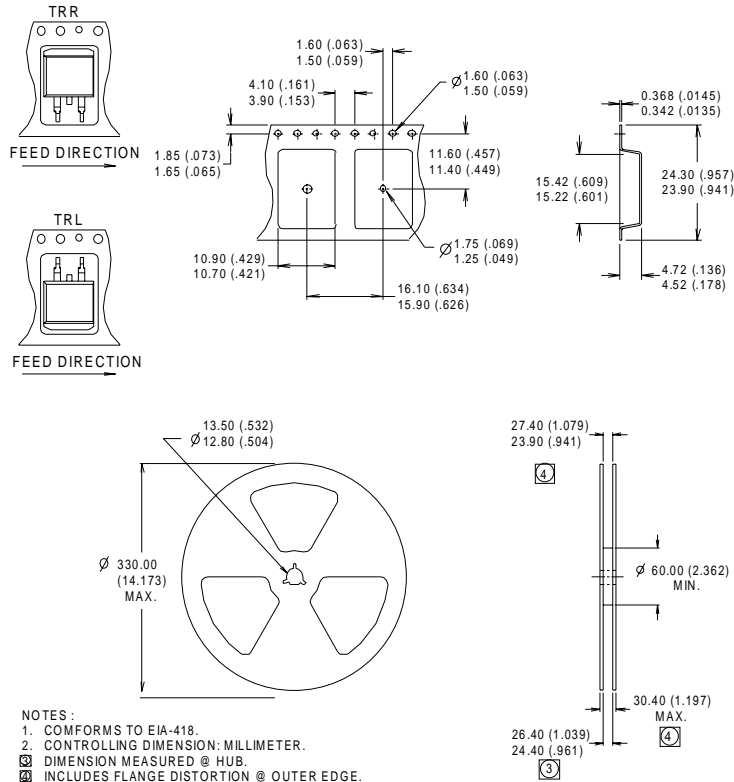


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Tape & Reel Information

D²Pak



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 12.6\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 10\text{A}$. (See Figure 12)
- ③ $I_{SD} \leq 10\text{A}$, $di/dt \leq 330\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ Uses IRF740A data and test conditions

* When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

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WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331

IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020

IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200

IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590

IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111

IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086

IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630

IR TAIWAN: 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936

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