FAIRCHILD SEMICONDUCTOR TM

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ADVANCE INFORMATION

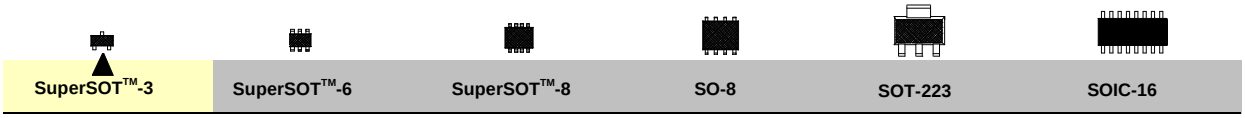
FDN337N
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

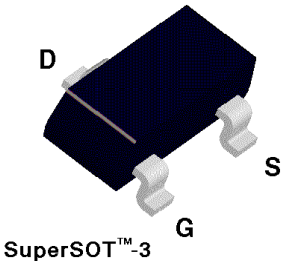
SuperSOT™-3 N-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

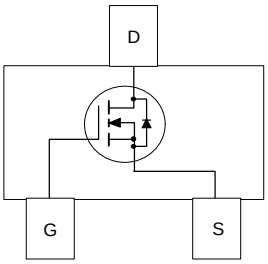
- 2.5 A, 20 V, $R_{DS(ON)}$ = 0.052 Ω @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 0.08 Ω @ V_{GS} = 2.5 V.
- Industry standard outline SOT-23 surface mount package using proprietary SuperSOT™-3 design for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-3 | SuperSOT™-6 | SuperSOT™-8 | SO-8 | SOT-223 | SOIC-16



SuperSOT™-3



Absolute Maximum Ratings T_A = 25°C unless other wise noted

Symbol	Parameter	FDN337N	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage - Continuous	±8	V
I_D	Maximum Drain Current - Continuous (Note 1a)	2.5	A
	- Pulsed	10	
P_D	Maximum Power Dissipation (Note 1a)	0.5	W
	(Note 1b)	0.46	
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	°C/W

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Symbol	Parameter	Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA		20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V				1	µA
			T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V_{DS} = 0 V				100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V				-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA		0.5		1	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 2.5 A				0.052	Ω
		V_{GS} = 2.5 V, I_D = 2 A				0.08	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V		10			A
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current					0.42	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.42 A (Note 2)				1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

   Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

   a. 250°C/W when mounted on a 0.02 in^2 pad of 2oz Cu.

   b. 270°C/W when mounted on a 0.001 in^2 pad of 2oz Cu.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.