

FAN8039BD3

5-CH Motor Driver

Features

- 1 Phase, Full-wave, Linear DC Motor Driver
- Built-in 5-CH Balanced Transformerless (BTL) Driver
- Built-in thermal shut down circuit (TSD)
- Built-in Variable Regulator With Power Tr.
- Built-in Power Save Circuit
- Built-in stand by mode circuit
- Wide Operating Supply Voltage : 4.5 ~ 13.2V

Description

The FAN8039BD3 is a monolithic integrated circuit suitable for a 5-ch motor driver which drives the tracking actuator, focus actuator, sled motor, tray motor, spindle motor of the DVDP/CAR-CD systems.

28-SSOPH-375SG2



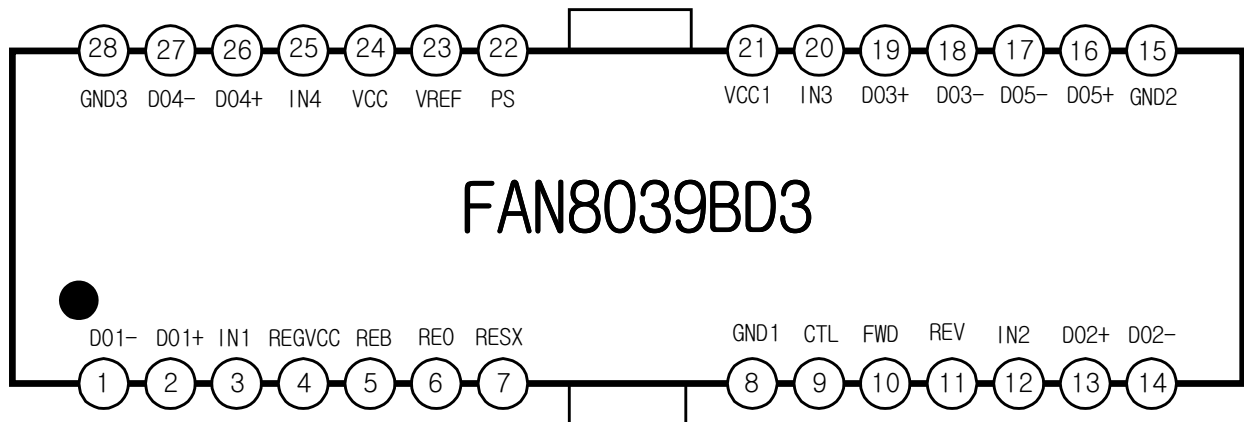
Typical Applications

- Compact disk player
- Video compact disk player
- Car compact disk player
- Mixing with compact disk player and mini disk player
- DVDP

Ordering Information

Device	Package	Operating Temp
FAN8039BD3	28-SSOPH-375SG2	-35°C ~ 85°C
FAN8039BD3T F	28-SSOPH-375SG2	-35°C ~ 85°C

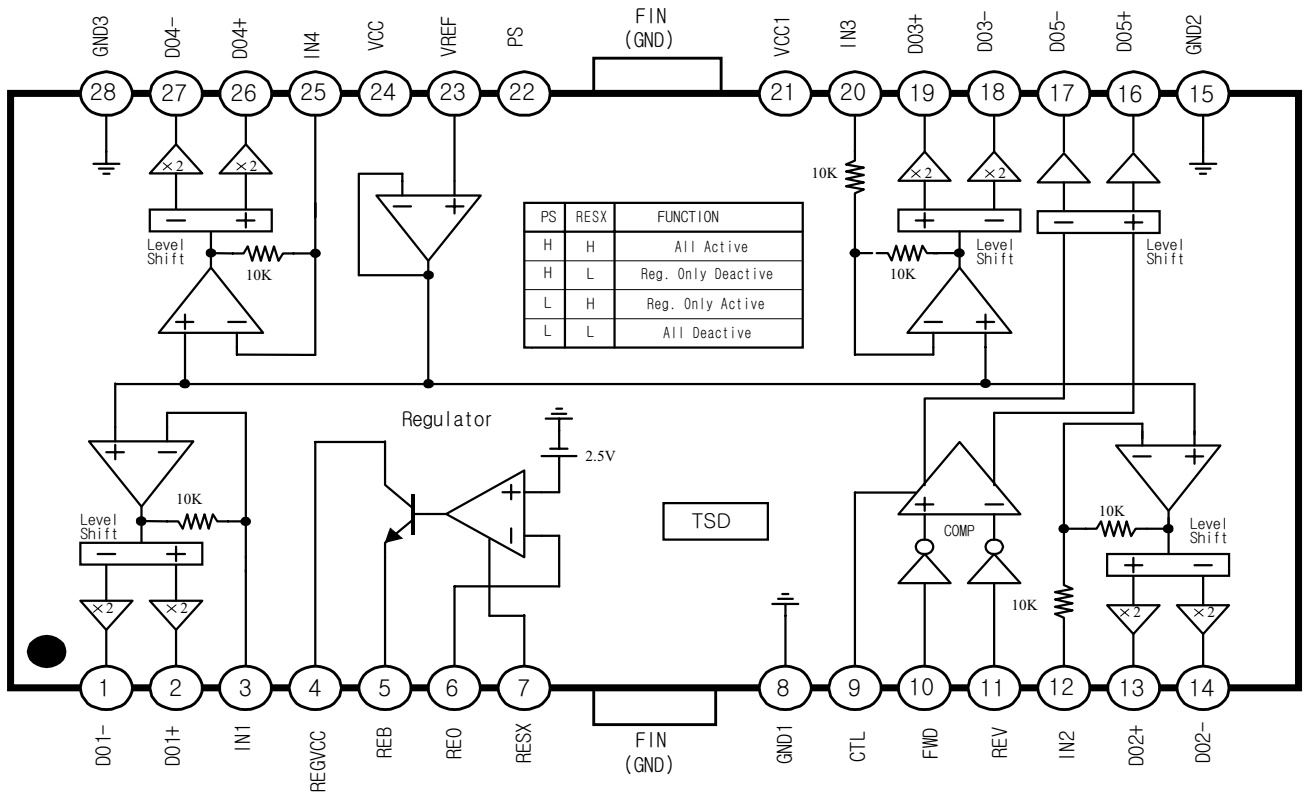
Pin Assignments



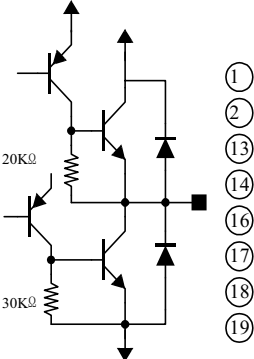
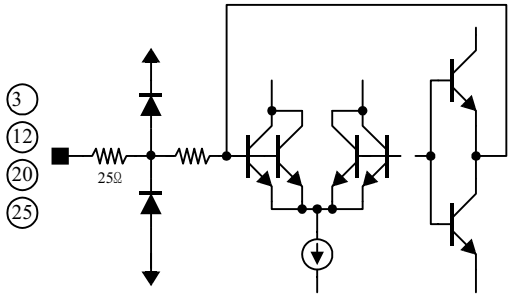
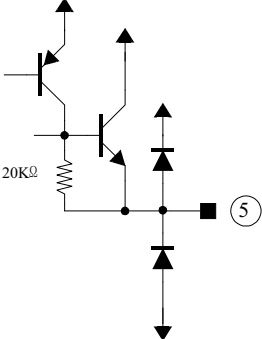
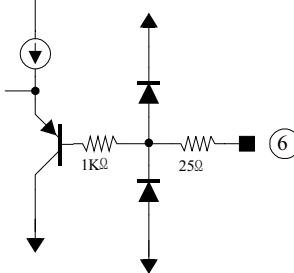
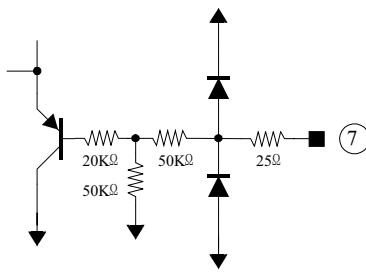
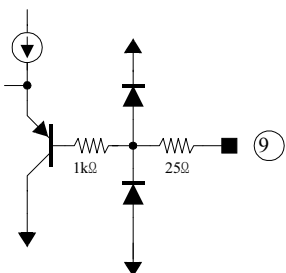
Pin Definitions

NO	Symbol	Description	NO	Symbol	Description
1	DO1-	CH1 Drive Output (-)	15	GND2	Power Ground1 (CH 2,3,5)
2	DO1+	CH1 Drive Output (+)	16	DO5+	CH5 Drive Output (+)
3	IN1	CH1 Drive Input	17	DO5-	CH5 Drive Output(-)
4	REGVCC	Regulator Supply Voltage	18	DO3-	CH3 Drive Output(-)
5	REB	Regulator Output	19	DO3+	CH3 Drive Output (+)
6	REO	Regulator Feedback Input	20	IN3	CH3 Drive Input
7	RESX	Regulator Reset	21	VCC1	Supply Voltage1(CH2,CH3,CH5)
8	GND1	Signal Ground	22	PS	Power Save
9	CTL	CH5 Motor Speed Control	23	VREF	Bias Voltage
10	FWD	CH5 Forward Input	24	VCC	Supply Voltage(CH1,CH4)
11	REV	CH5 Reverse Input	25	IN4	CH4 Drive Input
12	IN2	CH2 Drive Input	26	DO4+	CH4 Drive Output (+)
13	DO2+	CH2 Drive Output (+)	27	DO4-	CH4 Drive Output (-)
14	DO2-	CH2 Drive Output (-)	28	GND3	Power Ground2 (CH 1,4)

Internal Block Diagram



Equivalent Circuits

BTL DRIVER OUTPUT	BTL DRIVE INPUT
	
REGULATOR OUTPUT	REGULATOR FEEDBACK INPUT
	
REGULATOR RESET	MOTOR SPEED CONTROL
	

Equivalent Circuits (Continued)

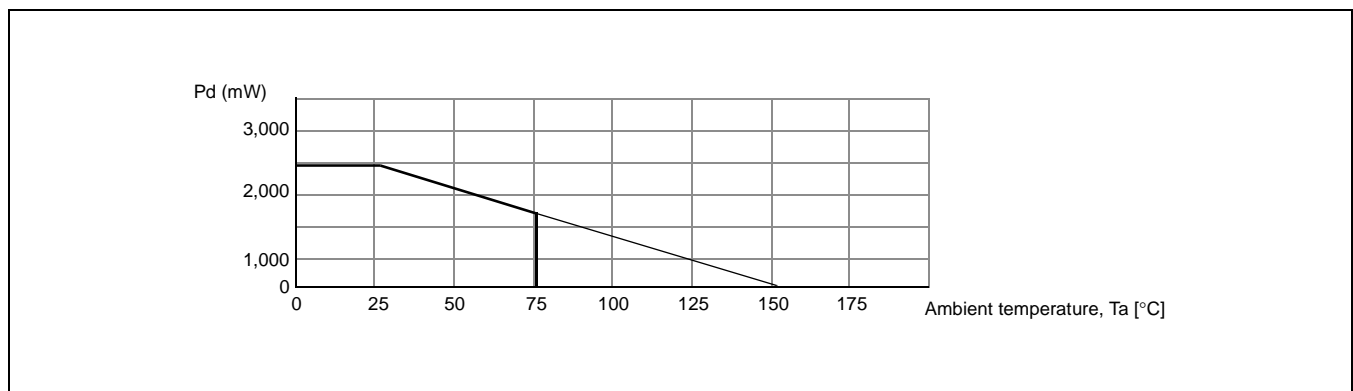
FOWARD INPUT	REVERSE INPUT
<p>Circuit diagram for Forward Input (10). It features two NPN transistors. The first transistor's base is connected to an input terminal through a 30KΩ resistor. Its emitter is grounded, and its collector is connected to the base of the second transistor through another 30KΩ resistor. The second transistor's emitter is also grounded, and its collector is connected to terminal 10 through a 25Ω resistor. A feedback loop is formed by a 30KΩ resistor connecting terminal 10 back to the base of the first transistor. Two diodes are connected in series between terminal 10 and ground, with their cathodes towards ground.</p>	<p>Circuit diagram for Reverse Input (11). It features two NPN transistors. The first transistor's base is connected to an input terminal through a 30KΩ resistor. Its emitter is grounded, and its collector is connected to the base of the second transistor through another 30KΩ resistor. The second transistor's emitter is also grounded, and its collector is connected to terminal 11 through a 25Ω resistor. A feedback loop is formed by a 30KΩ resistor connecting terminal 11 back to the base of the first transistor. Two diodes are connected in series between terminal 11 and ground, with their cathodes towards ground.</p>
POWER SAVE	BIAS VOLTAGE
<p>Circuit diagram for Power Save (22). It features a single NPN transistor. The base is connected to an input terminal through a 25Ω resistor. The emitter is grounded. The collector is connected to the base through a 20KΩ resistor. A 50KΩ resistor is connected between the base and ground. Two diodes are connected in series between the input terminal and ground, with their cathodes towards ground.</p>	<p>Circuit diagram for Bias Voltage (23). It features a differential pair of NPN transistors. The bases of both transistors are connected to a common input terminal through a 25Ω resistor. The emitters of both transistors are connected to a common emitter node, which is connected to ground through a 0.5KΩ resistor. The collectors of both transistors are connected to a common collector node, which is connected to a positive supply rail through two diodes in series, with their cathodes towards the collector node.</p>

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Value	Unit
Maximum Supply Voltage	VCC	18	V
Power Dissipation	PD	2.5 ^{note}	W
Operating Temperature	TOPR	-35 ~ +85	°C
Storage Temperature	TSTG	-55 ~ +150	°C
Maximum output current	IOMAX	1	A
Regulator Maximum output current	IROMAX	400	mA

Notes:

1. When mounted on 70mm × 70mm × 1.6mm PCB
2. Power dissipation reduces 20mW/°C for using above TA = 25°C
3. Do not exceed PD and SOA (Safe Operating Area)



Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Supply Voltage	VCC	4.5	-	13.2	V

Electrical Characteristics

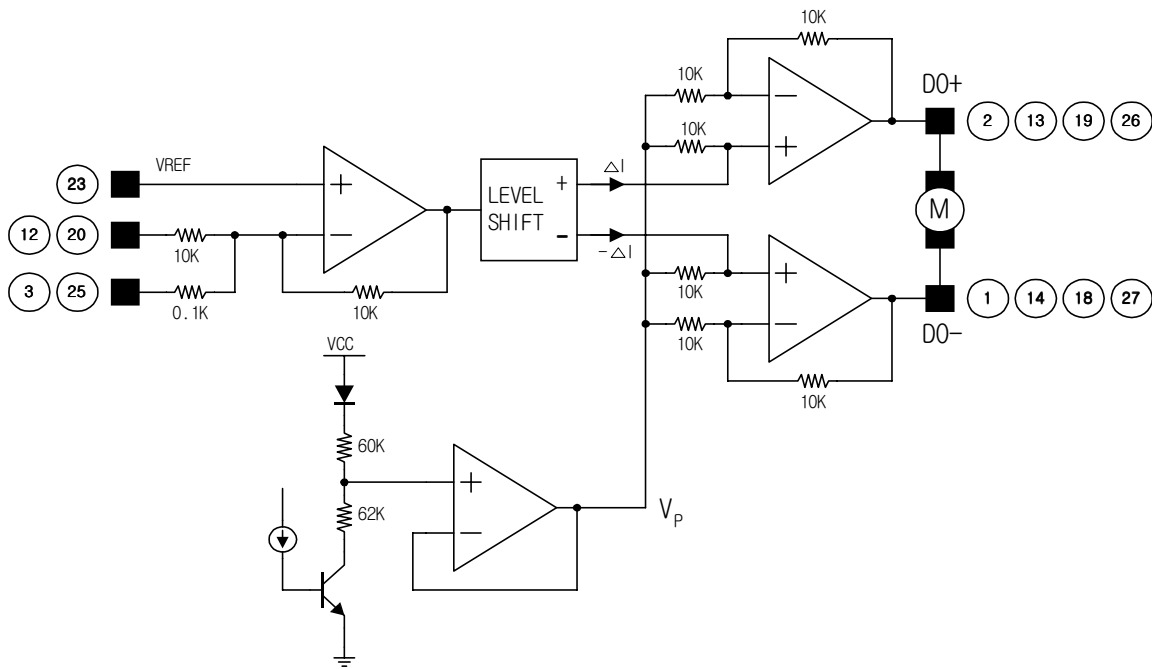
($V_{CC} = V_{CC1} = 8V$, $T_A = 25^\circ C$, unless otherwise specified)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
Quiescent Circuit Current	ICCQ	Under no - load	-	20	-	mA
Power Save On Current	IPS	Pin7=GND	-	1	2	mA
Power Save On Voltage	VPSON	Pin7=Variation	-	-	0.5	V
Power Save Off Voltage	VPSOFF	Pin7=Variation	2	-	-	V
VARIABLE REGULATOR PART						
Load Regulation	ΔV_{RL}	$I_L = 0mA \rightarrow 200mA$	-40	0	10	mV
Line Regulation	ΔV_{CC}	$I_L = 200mA, V_{CC}=6V \rightarrow 9V$	-20	0	30	mV
Regulator Output Voltage 1	VREG1	$I_L = 100mA$	4.75	5	5.25	V
Regulator Output Voltage 2	VREG2	$I_L = 100mA$	3.135	3.3	3.465	V
*Regulator Output Peak Current	IPK	$T_j = 25^\circ C$		700		mA
BLT DRIVER PART						
Output Offset Voltage	VOO	$V_{IN}=2.5V$	-40	0	40	mV
Maximum Output Voltage1	VOM1	$V_{CC}=V_{CC1}=8V, R_L = 12\Omega$	5.5	6.5	-	V
Maximum Output Voltage2	VOM2	$V_{CC}=V_{CC1}=13V, R_L = 24\Omega$	10.5	11.5	-	V
Close Loop Voltage Gain	AVF	$V_{IN}=0V, 1V_{rms}, f = 1KHz$	10.5	12	13.5	dB
Slew rate	SR	$V_{OUT}=4VP-P, f = 120KHz, Square$	-	2	-	V/ μs
LOADING MOTOR DRIVER PART						
Input High Level Voltage	V _{IH}	-	2	-	-	V
Input Low Level Voltage	V _{IL}	-	-	-	0.5	V
Output Voltage1	VO1	$V_{CC}=V_{CC1}=8V, V_{CTL}=OPEN, R_L=12\Omega$	5.5	6.5	-	V
Output Voltage2	VO2	$V_{CC}=V_{CC1}=12V, V_{CTL}=OPEN, R_L=24\Omega$	9.5	10.5	-	V
Output Offset Voltage1	VOO1	$V_{IN}=5V, 5V$	-40	-	40	mV
Output Offset Voltage2	VOO2	$V_{IN}=0V, 0V$	-40	-	40	mV

*.Pulse Testing with Low Duty.

Application Information

1. Driver (Except For Loading Motor Driver)



A voltage, V_{REF} is the reference voltage driven by the external bias voltage on pin#23. The input signal (V_{in}) on pin#12 and #20 is amplified by 10K/10K times and then fed to the level shift. The level shift provides a current as $+\Delta I$ and $-\Delta I$ due to the difference between the input signal and the arbitrary reference signal. The current can be fed into the driver Amp, so it drives the power TR on the output stage. The output can be shown 2 times as much as the input signal. (gain = $1 + 10K/10K$).

$$V_{IN} = V_{REF} + \Delta V \Delta I = \frac{\Delta V}{10K}$$

$$DO+ = V_P + \Delta I \cdot 10K \cdot \left(1 + \frac{10K}{10K}\right) = V_P + 2\Delta V$$

$$DO- = V_P - \Delta I \cdot 10K \cdot \left(1 + \frac{10K}{10K}\right) = V_P - 2\Delta V$$

$$V_{OUT} = (DO+) - (DO-) = 4\Delta V$$

$$GAIN = 20\log\left(\frac{V_{OUT}}{\Delta V}\right) = 12dB$$

Pin#3 or #25 can be used to modify the gain. The output stage is the balanced transformerless(BTL) driver. The bias voltage V_P is described as follows.

$$V_P = (VCC - V_{BE} - V_{CE(SAT)}) \times \frac{62K}{60K + 62K} + V_{CE(SAT)}$$

$$= \frac{VCC - V_{BE} - V_{CE(SAT)}}{1.97} + V_{CE(SAT)}$$

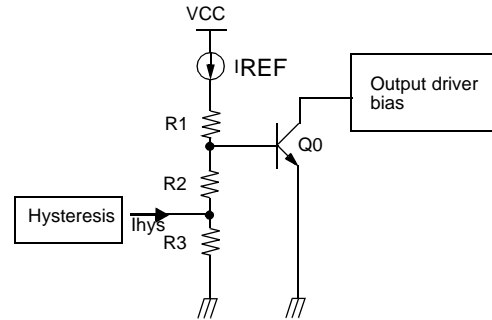
2. Thermal Shutdown

The TSD circuit turns activated when the junction temperature becomes over 175°C.

It cuts off the bias current on the output driver and keeps all the output drivers off. Meanwhile, the junction temperature begins to decrease.

The TSD circuit can be deactivated when the unction temperature falls under 150°C, so the output driver begins operating in normal condition

The TSD circuit has the hysteresis temperature of 25°C.

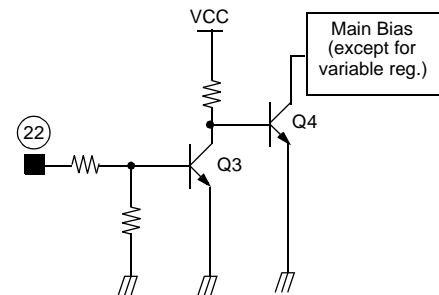


3. Power Save Function

When the pin22 is high, the TR Q3 is turned on and Q4 is off, so the bias circuit is enabled. On the other hand, when the pin22 is Low (GND), the TR Q3 is turned off and Q4 is on, so the bias circuit is disabled.

that is, it will make all the circuit blocks except for variable regulator off, so low power quiescent state can be established. Truth table is as follows.

Pin#22	FAN8039BD3
High	Power Save Off
Low	Power Save On



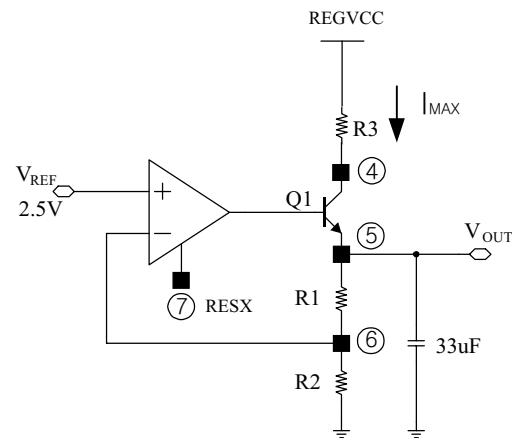
4. Variable Regulator

A 33uF capacitor is used as a ripple eliminator in the external circuit. Therefore, output voltage, Vout can be calculated as follows.

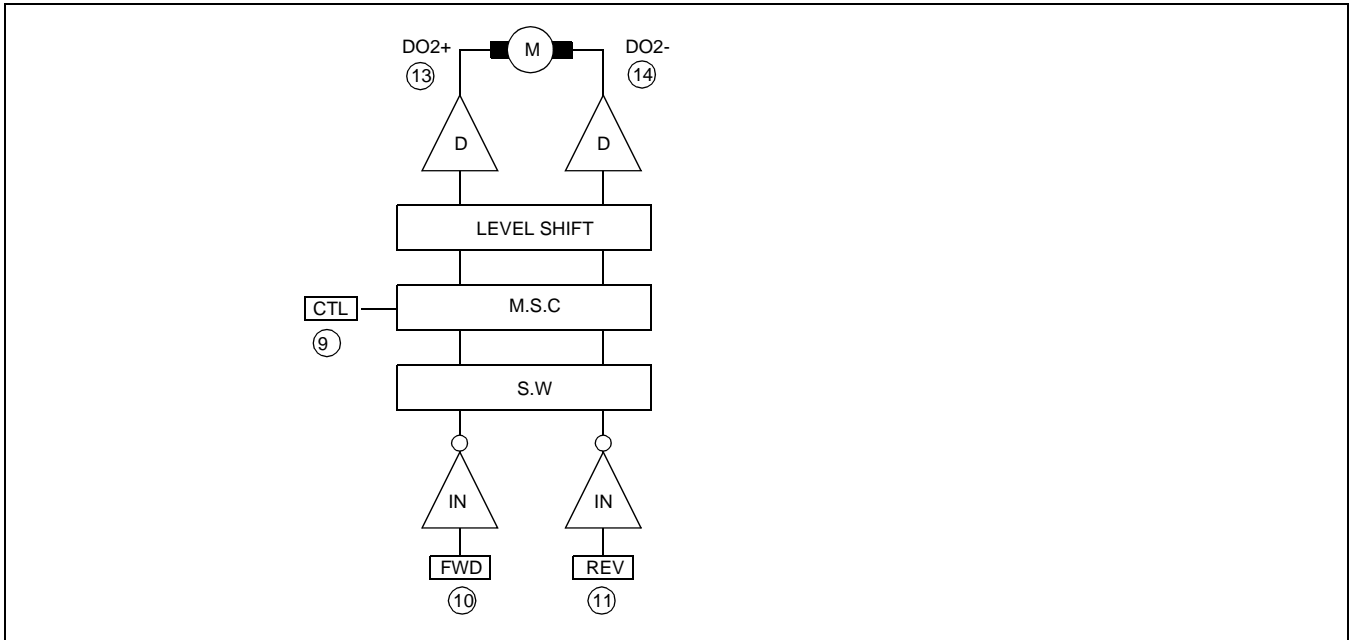
$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_1}{R_2}\right) = 2.5 \times 2 = 5V (R_1 = R_2)$$

In order to reduce the heating problem on regulator output TR, Q1, a resistor R3 can be used and calculated as follows.

$$R_3 = \frac{(REGVCC - (V_{out} + 1.5))}{I_{MAX}}$$



5. Loading Motor Driver



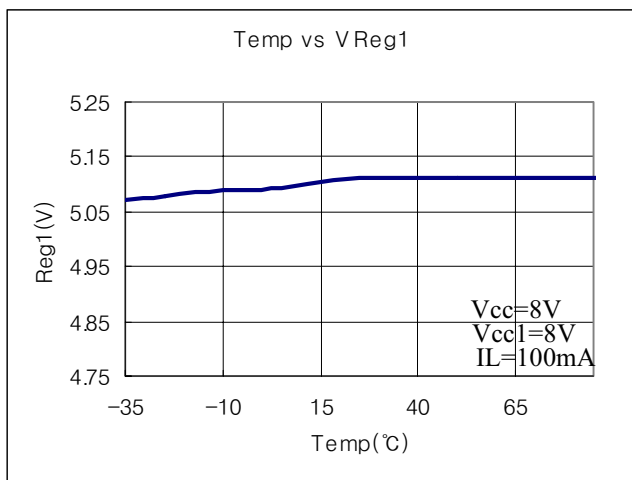
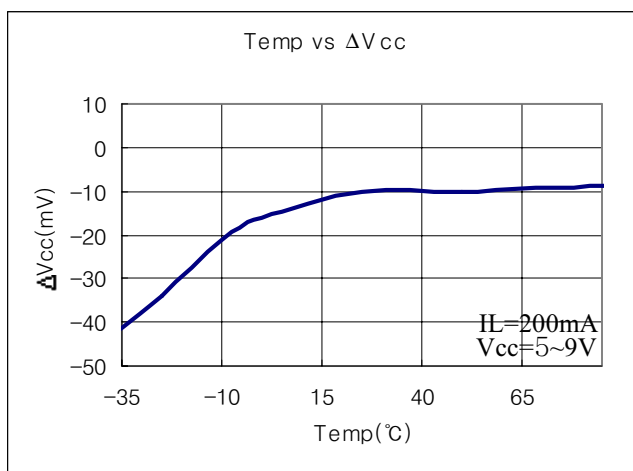
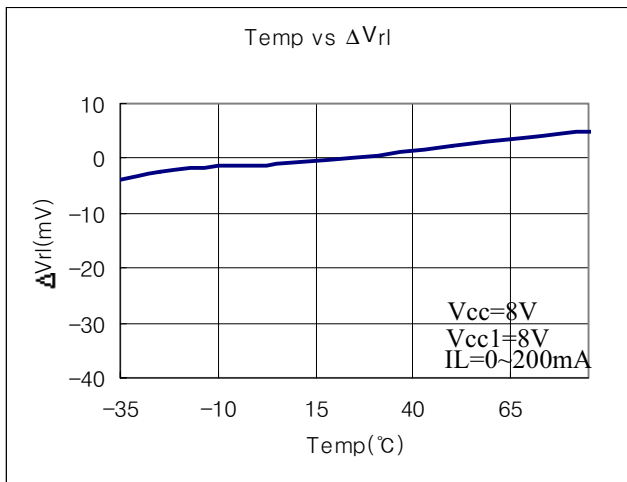
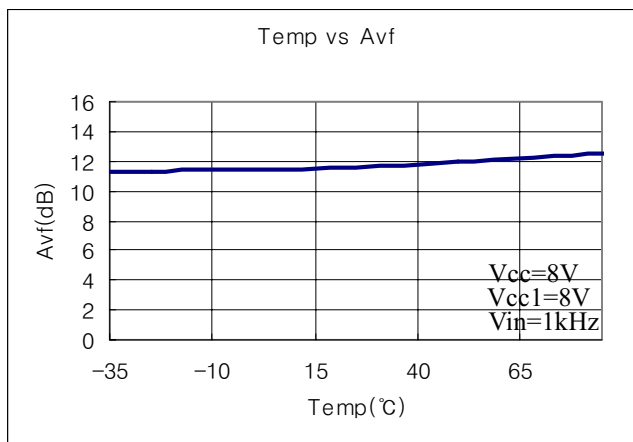
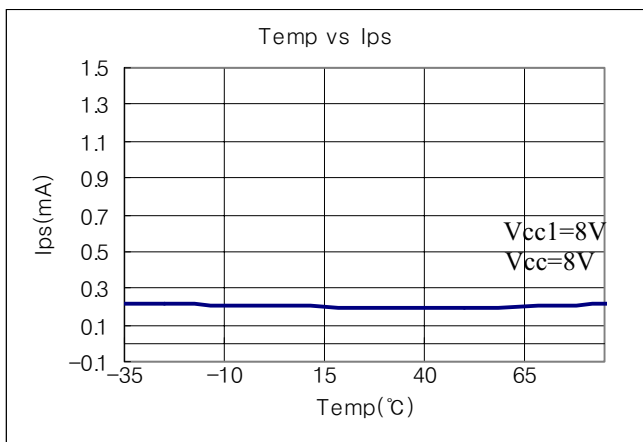
- Rotational direction control

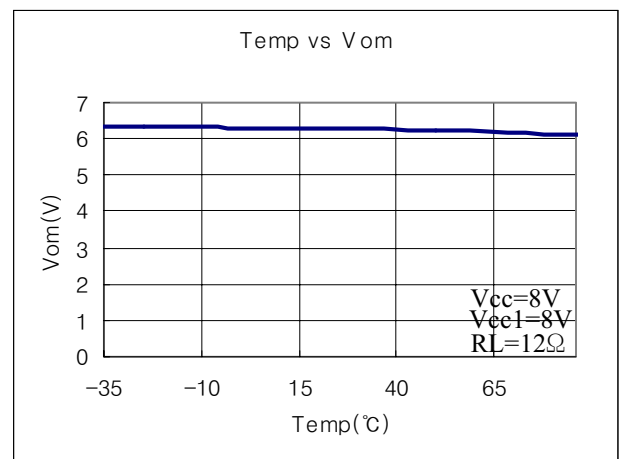
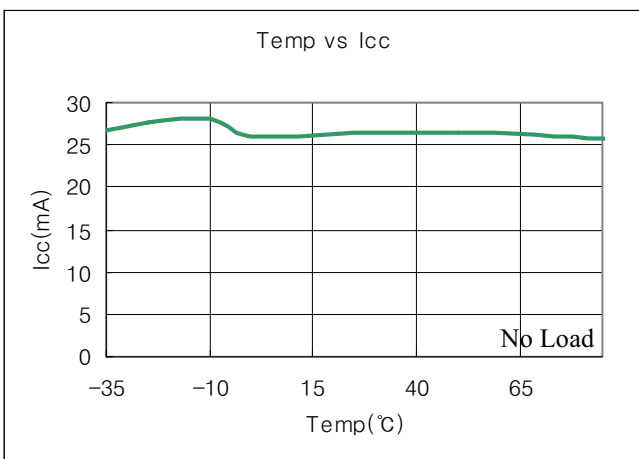
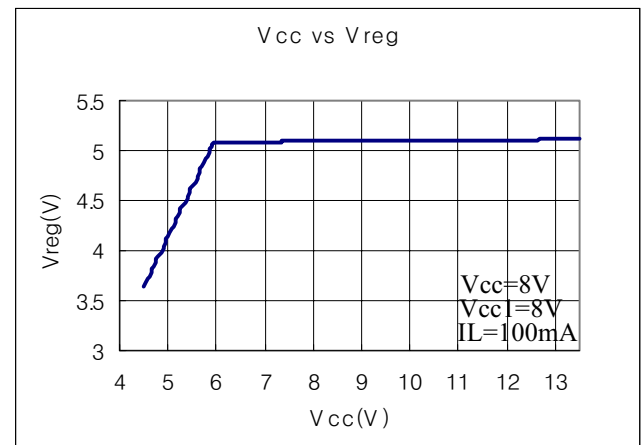
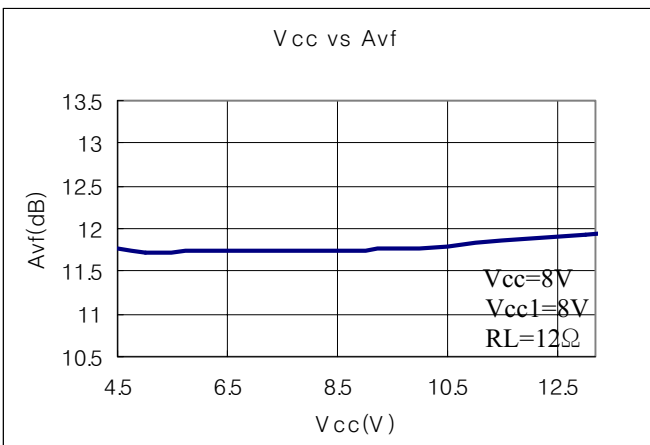
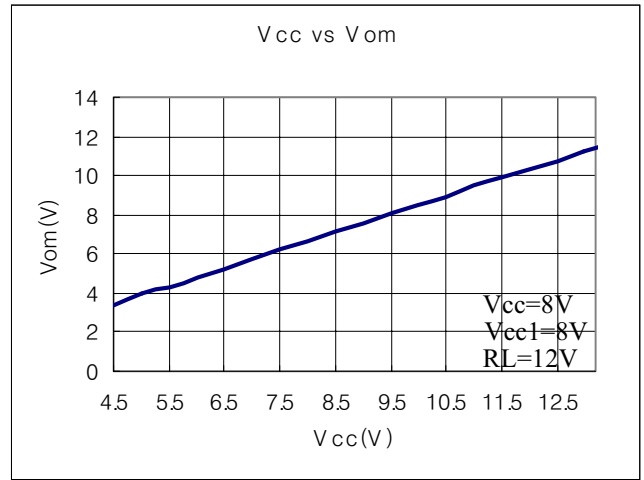
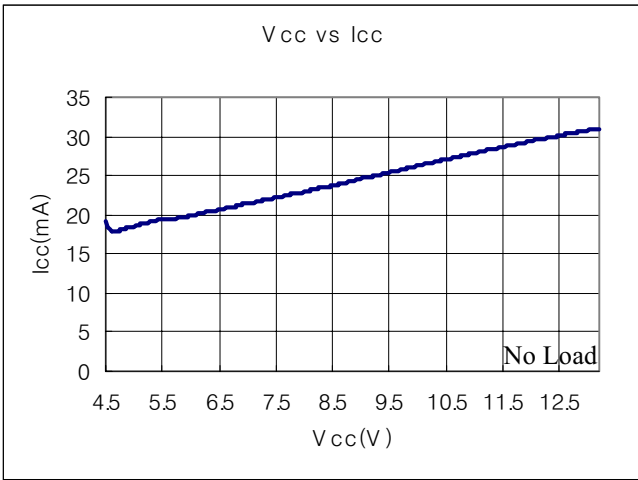
The forward and reverse rotational direction is controlled by FWD (pin10) and REV (pin11) , so the conditions are as follows.

INPUT		OUTPUT		
FWD	REV	OUT 1	OUT 2	State
H	H	Vp	Vp	High Impedence
H	L	H	L	Forward
L	H	L	H	Reverse
L	L	-	-	Short Brake

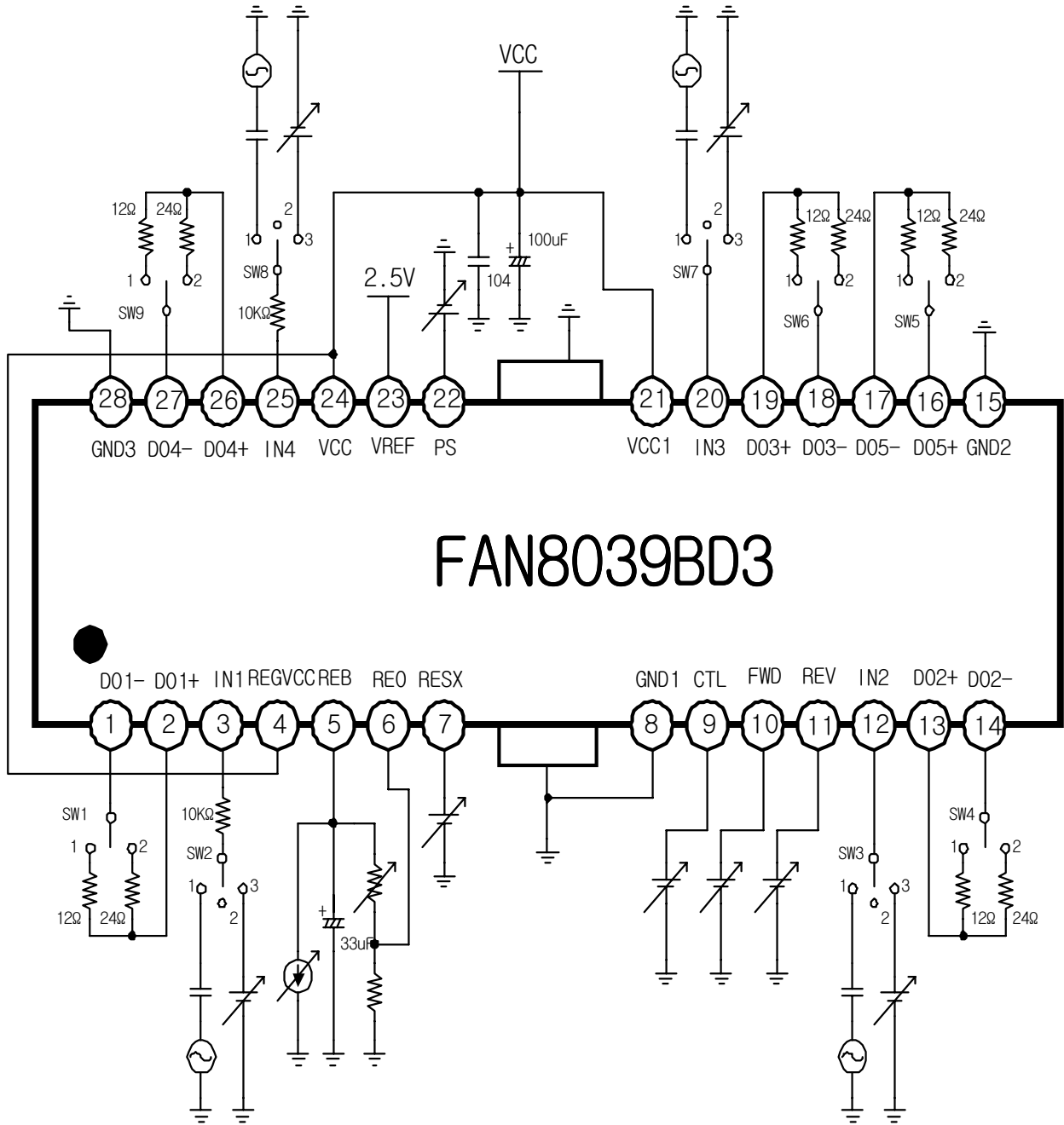
- Vp(Power Bias voltage) can be approximately 3.75V where Vcc1 and Vcc are 8V.
- Motor speed control (Where VCC=VCC1=8V)
 - The maximum torque can be obtained when the pin 9(CTL) is open.
 - If the voltage on pin 9(CTL) is 0V, the motor will not be operating.

Typical Performance Characteristics

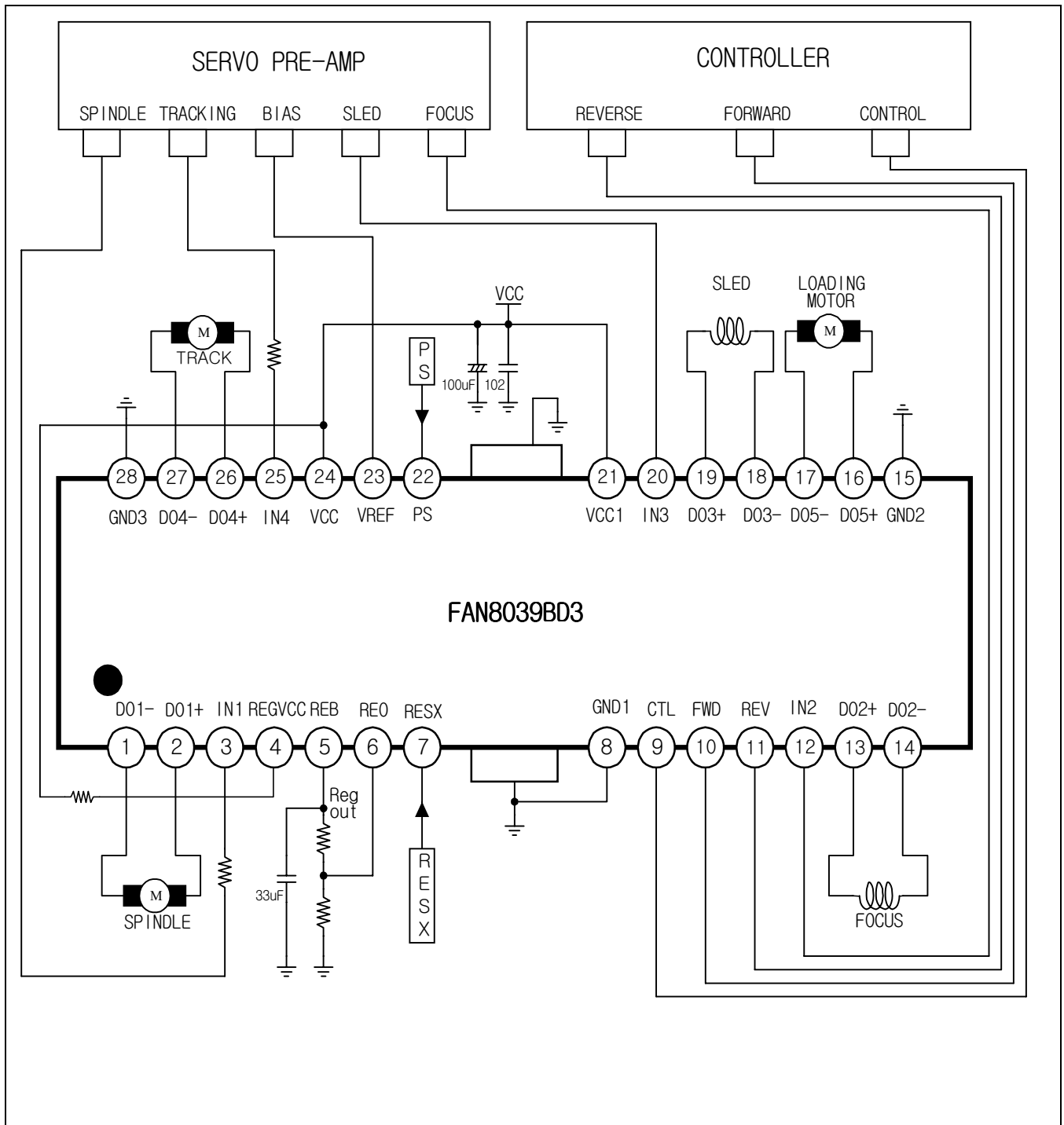




Test Circuit



Application Circuit



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