HARRIS SEMICONDUCTOR

DG211, DG212

December 1993

SPST 4 Channel Analog Switch

Features

- **Switches ±15V Analog Signals**
- **TTL Compatibility**
- **Logic Inputs Accept Negative Voltages**
- **R_{ON} ≤175Ω**

Ordering Information

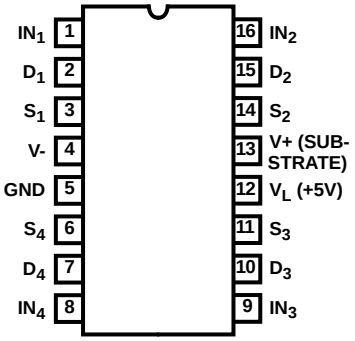
PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG211CJ	0°C to +70°C	16 Lead Plastic DIP
DG212CJ	0°C to +70°C	16 Lead Plastic DIP
DG211CY	0°C to +70°C	16 Lead SOIC (N)
DG212CY	0°C to +70°C	16 Lead SOIC (N)

Description

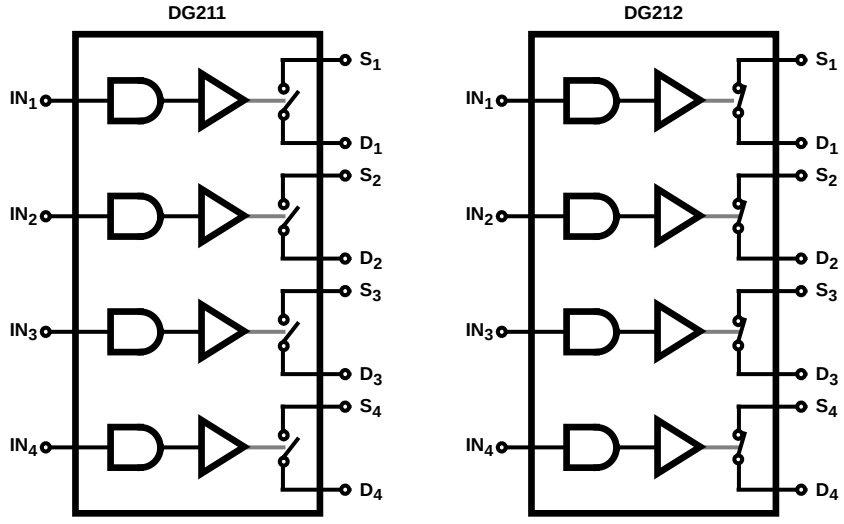
The DG211 and DG212 are low cost, CMOS monolithic, Quad SPST analog switches. These can be used in general purpose switching applications for communications, instrumentation, process control and computer peripheral equipment. Both devices provide true bidirectional performance in the ON condition and will block signals to 30V peak-to-peak in the OFF condition. The DG211 and DG212 differ only in that the digital control logic is inverted, as shown in the truth table.

Pinout

DG211, DG212
(PDIP, SOIC)
TOP VIEW



Functional Diagrams



NOTES:
1. Four SPST switches per package.
2. Switches shown for logic "1" input

TRUTH TABLE

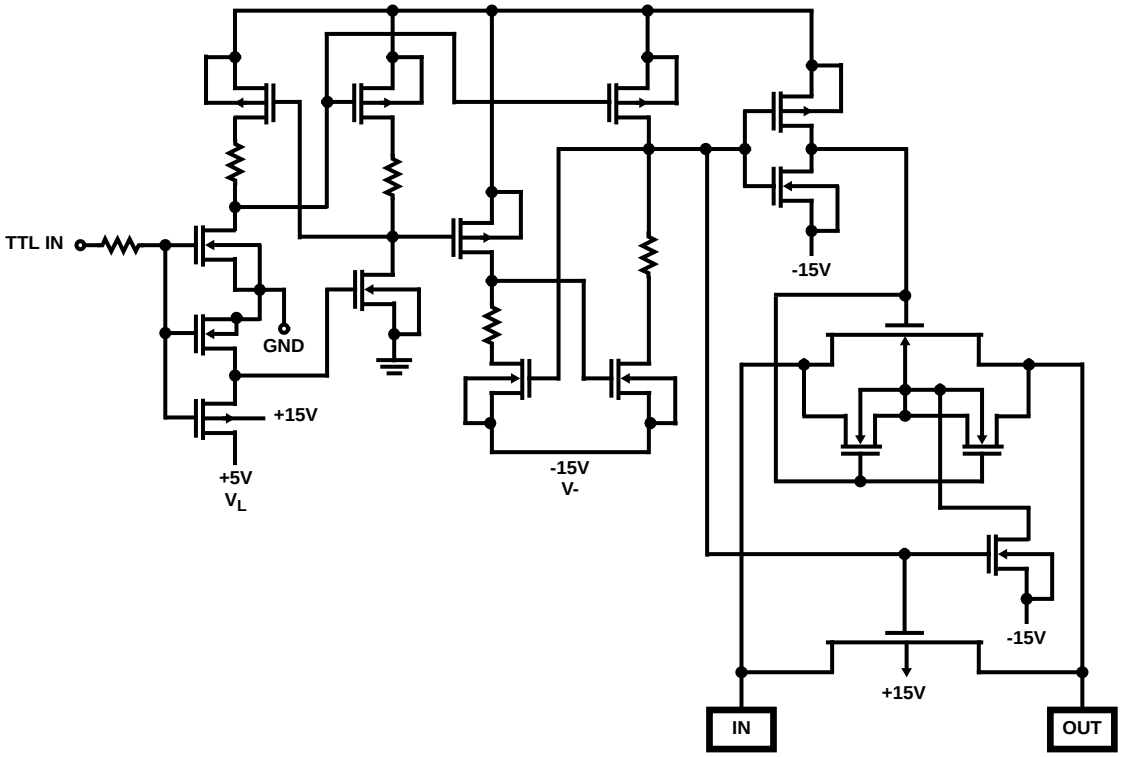
LOGIC	DG211	DG212
0	ON	OFF
1	OFF	ON

Logic "0" ≤0.8V, Logic "1" ≥ 2.4V

File Number **3118**

Schematic Diagram

DG211 ($^1/_4$ AS SHOWN)



Absolute Maximum Ratings

V+ to V- 44V
V_{IN} to Ground . . . . . V-, V+
V_L to Ground . . . . . -0.3V, 25V
V_S or V_D to V+ . . . . . 0, -36V
V_S or V_D to V- 0, 36V
V+ to Ground 25V
V- to Ground . . . . . -25V
Current, any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max) 70mA
Lead Temperature (Soldering 10s) . . . . . +300°C
Storage Temperature Range . . . . . -65°C to +125°C

Thermal Information

Thermal Resistance	θ_{JA}
Plastic DIP Package	100°C/W
SOIC Package	120°C/W
Junction Temperature	+150°C
Operating Temperature	0°C to +70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = +15V, V- = -15V, V_L = +5V, GND, T_A = +25°C

PARAMETERS	TEST CONDITIONS		(NOTE 1) MIN	(NOTE 2) TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-On Time, t_{ON}	See Figure 1 V_S = 10V, R_L = 1kΩ, C_L = 35pF		-	460	1000	ns
Turn-Off Time, t_{OFF1}			-	360	500	ns
t_{OFF2}			-	450	-	ns
Source OFF Capacitance, $C_{S(OFF)}$	V_S = 0V, V_{IN} = 5V, f = 1MHz (Note 2) V_D = 0V, V_{IN} = 5V, f = 1MHz (Note 2) V_D = V_S = 0V, V_{IN} = 0V, f = 1MHz (Note 2)		-	5	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$			-	5	-	pF
Channel ON Capacitance, $C_{D + S(ON)}$			-	16	-	pF
OFF Isolation, OIRR (Note 4)	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF, V_S = $1V_{RMS}$, f = 100kHz (Note 2)		-	70	-	dB
Crosstalk (Channel to Channel), CCRR			-	90	-	dB
INPUT						
Input Current with Voltage High, I_{INH}	V_{IN} = 2.4V		-1.0	-0.0004	-	µA
	V_{IN} = 15V		-	0.003	1.0	µA
Input Current with Voltage Low, I_{INL}	V_{IN} = 0V		-1.0	-0.0004	-	µA
SWITCH						
Analog Signal Range, V_{ANALOG}	V- = -15V, V_L = +5V		-15	-	15	V
Drain Source On Resistance, $R_{DS(ON)}$	V_D = ±10V, V_{IN} = 2.4V (DG212) I_S = 1mA, V_{IN} = 0.8V (DG211)		-	150	175	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{IN} = 2.4V (DG211) V_{IN} = 0.8V (DG212)	V_S = 14V, V_D = -14V	-	0.01	5.0	nA
		V_S = -14V, V_D = 14V	-5.0	-0.02	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		V_S = -14V, V_D = 14V	-	0.01	5.0	nA
		V_S = 14V, V_D = -14V	-5.0	-0.02	-	nA
Drain ON Leakage Current, $I_{D(ON)}$ (Note 3)	V_S = V_D = -14V, V_{IN} = 0.8V (DG211) V_{IN} = 2.4V (DG212)		-	0.1	5.0	nA
			-5.0	-0.15	-	nA

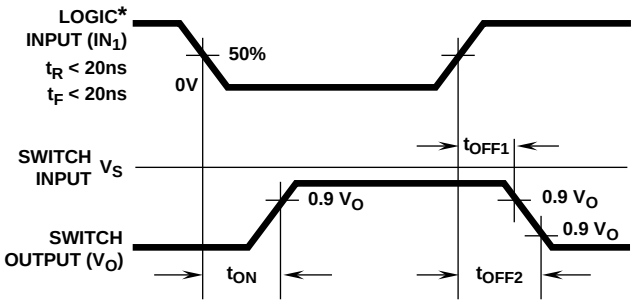
Electrical Specifications V+ = +15V, V- = -15V, V_L = +5V, GND, T_A = +25°C **(Continued)**

PARAMETERS	TEST CONDITIONS	(NOTE 1) MIN	(NOTE 2) TYP	MAX	UNITS
POWER SUPPLY CHARACTERISTICS					
Positive Supply Current, I+	V_{IN} = 0V and 2.4V	-	0.1	10	µA
Negative Supply Current, I-		-	0.1	10	µA
Logic Supply Current, I_L		-	0.1	10	µA

NOTES:
1. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
2. For design reference only, not 100% tested.
3. $I_{D(ON)}$ is leakage from driver into ON switch.
4. OFF Isolation $= 20\log\frac{V_S}{V_D}$, V_S = Input to OFF switch, V_D = output
5. Switching times only sampled.

Test Circuits

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note the V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



* Logic shown for DG211. Invert for DG212.

FIGURE 1. SWITCHING TIME TEST WAVEFORMS

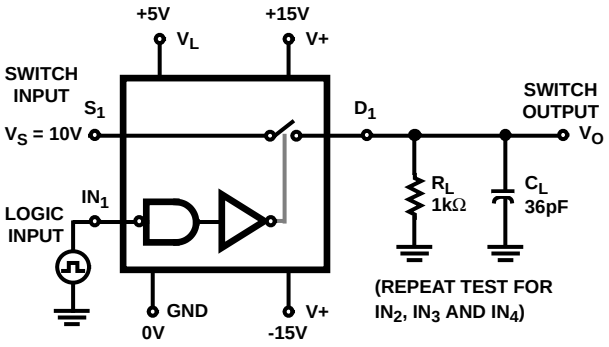


FIGURE 2. SWITCHING TIME TEST CIRCUIT

Metallization Topology

DIE DIMENSIONS:
2159µm x 2235µm

METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG/Nitride
PSG Thickness: 7kÅ ± 1.4kÅ
Nitride Thickness: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

DG211, DG212