
Chrontel CH7028B SDTV Encoder

Features

- TV encoder targets the handheld devices and other appropriate display devices used in consumer products. (i.e. automobile).
- Support TV output format (NTSC, PAL).
- Two on-chip 10-bit high speed DACs providing flexible output capabilities. Such as single, double CVBS outputs, and S-video output.
- Internal embedded 16Mbits SDRAM is used as frame buffer supporting for frame rate conversion.
- Flexible up and down scaling engine is embedded including de-flickering capability.
- Programmable 18-bit/16-bit/15-bit/12-bit/8-bit digital input interface supports various RGB (RGB666, RGB565 and etc), YCbCr (4:2:2 YCbCr, ITU656) and 2x or 3x multiplexed input. CPU/MEMORY interface is also supported.
- Support for flexible input resolution up to 800x800 and 1024x680. (i.e. 220x176, 320x240, 640x480 720x480, 720x576, 800x480, 800x600 480x800, 600x800 and etc)
- Pixel by pixel brightness, contrast, hue and saturation adjustment for each output is supported.
- Pixel by pixel horizontal position adjustment and line by line vertical position adjustment are supported.
- 90/180/270 degree image rotation and vertical or horizontal flip functions are supported.
- TV connection detection capability. DAC can be switched off based on detection result. (Driver support is required)
- Programmable power management.
- Flexible pixel clock frequency from graphics controller is supported (2.3MHz –120MHz).
- Flexible input clock from crystal or oscillator is supported (2.3MHz – 64MHz).
- Only slave mode supported.
- Offered in LQFP package and BGA package.
- Fully programmable through serial port.
- IO and SPC/SPD voltage supported is from 1.2V to 3.3V.

General Description

The CH7028B is a device targeting handheld and similar systems which accept digital input signal, and encodes and transmits data through 10-bit DACs. The device is able to encode the video signals and generate synchronization signals for NTSC and PAL standards. The device accepts different data formats including RGB and YCbCr (e.g. RGB565, RGB666, ITU656 like YCbCr, etc.). 16Mbit SDRAM is embedded in package. Frame rate conversion and Image rotation are possible.

Note: the above feature list is subject to change without notice. Please contact Chrontel for more information and current updates.

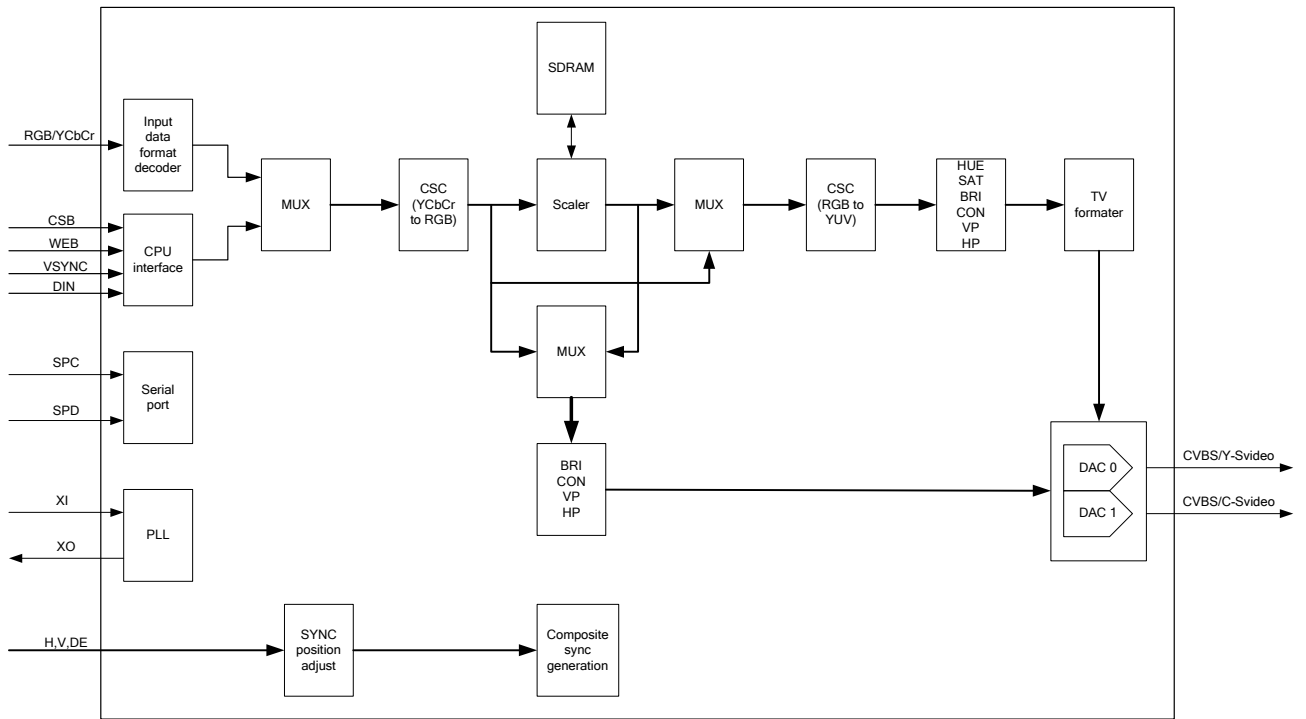


Figure 1: CH7028B Block Diagram

1.0 Pin-out

1.1 Package Diagram

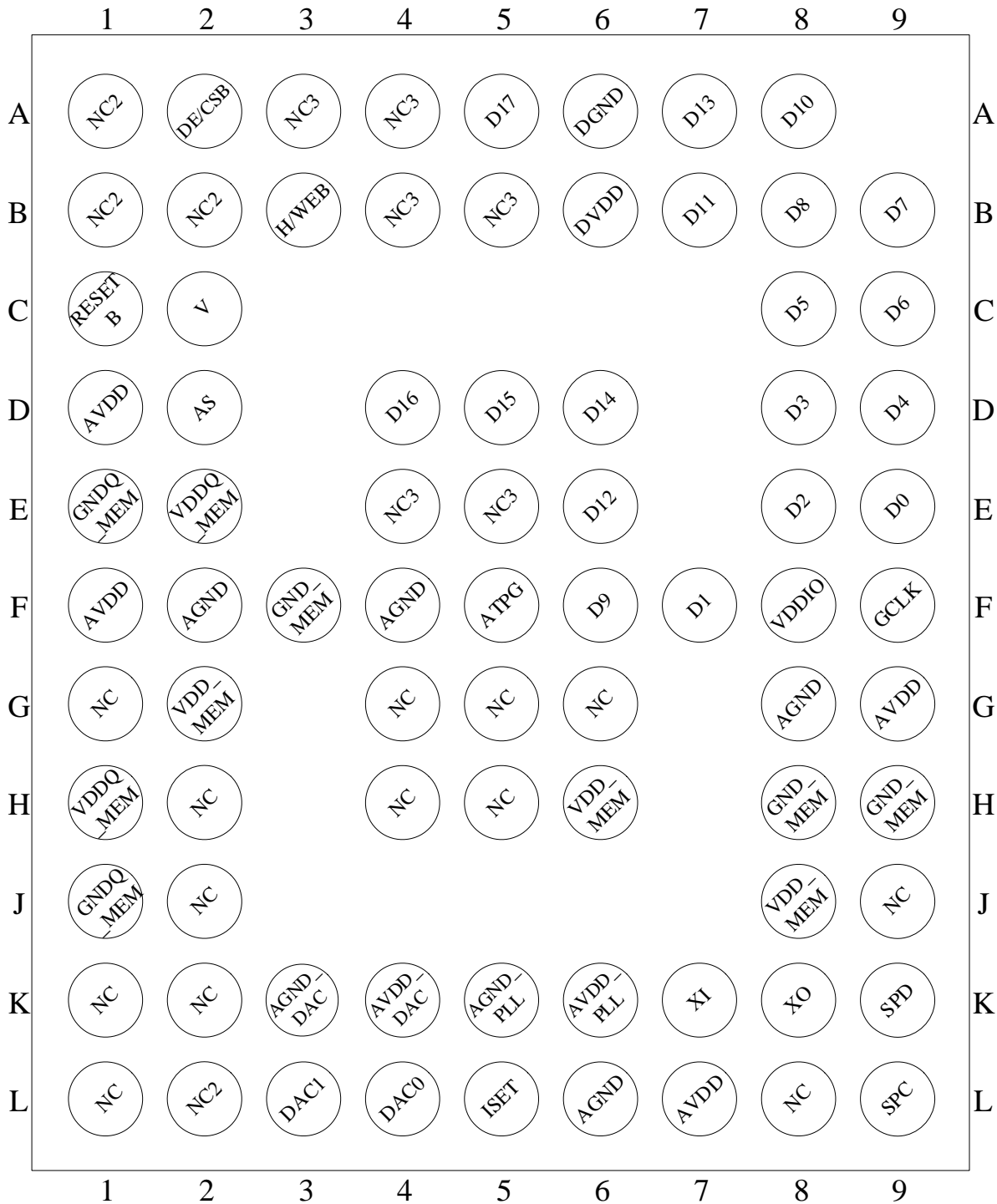


Figure 2: 80 pin BGA Package(Top view)

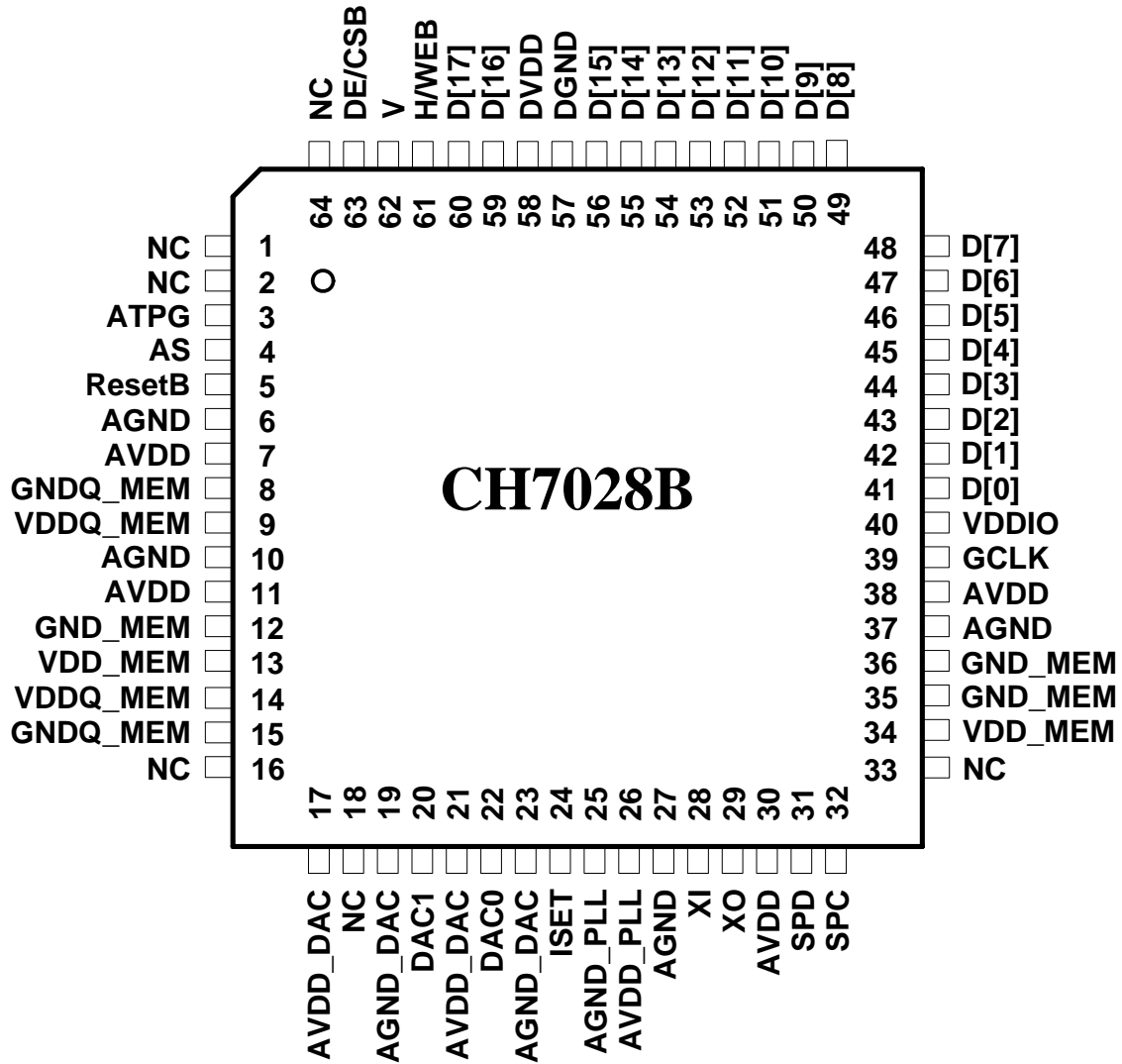


Figure 3: 64 pin LQFP Package

1.2 Pin Description

Table 1: Pin Name Description (BGA Package)

Pin #	Type	Symbol	Description
A5, D4, F7, E9, D5, D6, A7, E6, B7, A8, F6, B8, B9, C9, C8, D9, D8, E8	In	D[17:0] ^[1]	Data[0] through Data[17] Inputs These pins accept the 18 data inputs from a digital video port of a graphics controller. The swing is defined by VDDIO.
C2	In/Out	V	Vertical Sync Input / Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.
B3	In/Out	H/WEB	Horizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of CPU/MEMORY interface.
A2	In	DE/CSB	Data Input Indicator When the pin is high, the input data is active. When the pin is low, the input data is blanking. It is also the CSB signal of CPU/MEMORY interface.
D2	In	AS	Serial Port Device Address Select 0: 76h 1: 75h
F5	In	ATPG	ATPG Enable (Internally pull-low) This pin should be left open or pulled low with a 10k resistor in the application. This pin configures the pre-condition for scan chain and boundary scan test when high. Otherwise it should be pulled low. Voltage level is 0 to 3.3V.
C1	In	RESETB	Active low reset. When RESETB is low, the device is held in the hardware reset condition. When RESETB is high, reset is controlled through the serial port.
K9	In/Out	SPD	Serial Port Data Input / Output (open drain) This pin functions as the bi-directional data pin of the serial port. External pull-up resistor is required.
L9	In	SPC	Serial Port Clock Input (open drain) This pin functions as the clock pin of the serial port. External pull-up resistor is required.
L4	Out	DAC0	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3 V.
L3	Out	DAC1	CVBS, S-video, YPbPr or Analog RGB output Full swing is up to 1.3 V.
L5	In	ISET	Current Set This pin sets the DAC current. A 1.2k Ω , 1% tolerance resistor should be connected between this pin and AGND_DAC using short and wide trace.

Pin #	Type	Symbol	Description
K7	In	XI	Crystal Input / External Input For some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI input.
K8	Out	XO	Crystal Output For some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XI. However, if an external CMOS clock is attached to XI, XO should be left open.
F9	In	GCLK	Graphics Controller Clock Input
F8	Power	VDDIO	IO supply voltage (1.2-3.3V)
B6	Power	DVDD	Digital supply voltage (1.8V)
D1, F1, L7, G9	Power	AVDD	Analog supply voltage (2.5 – 3.3V)
K6	Power	AVDD_PLL	PLL supply voltage (1.8V)
K4	Power	AVDD_DAC	DAC power supply (2.5 – 3.3V)
E2, H1	Power	VDDQ_MEM	SDRAM output buffer supply voltage (2.5V)
G2, J8, H6	Power	VDD_MEM	SDRAM device supply voltage (2.5V)
A6	Power	DGND	Digital supply ground
F4, F2, L6, G8	Power	AGND	Analog supply ground
K5	Power	AGND_PLL	PLL supply ground
K3	Power	AGND_DAC	DAC supply ground
E1, J1	Power	GNDQ_MEM	SDRAM output buffer supply ground
F3, H9, H8	Power	GND_MEM	SDRAM device supply ground
		NC	All the NC pins should be left open.

Notes:

1. All the unused Data input pins should be pulled low with 10k Ω resistors or shorted to Ground directly.
2. All the NC pins should be left open.

Table 2: Pin Name Descriptions (LQFP64 Package)

Pin #	Type	Symbol	Description
41 - 56 59 - 60	In	D[17:0] ^[1]	Data[0] through Data[17] Inputs These pins accept the 18 data inputs from a digital video port of a graphics controller. The swing is defined by VDDIO.
62	I/O	V	Vertical Sync Input / Output When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply.
61	I/O	H/WEB	Horizontal Sync Input / Output When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. It is also the WEB signal of CPU/MEMERY interface.
63	In	DE/CSB	Data Input Indicator When the pin is high, the input data is active. When the pin is low, the input data is blanking. CSB signal input of CPU/MEMERY interface.
4	In	AS	Serial Port Device Address Select 0: 76h 1: 75h
3	In	ATPG	ATPG Enable (Internally pull-down) This pin should be left open or pulled low with a 10k resistor in the application. This pin configures the pre-condition for scan chain and boundary scan test when high. Otherwise it should be pulled low. Voltage level is 0 to 3.3V.
5	In	ResetB	Reset * Input When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port.
31	I/O	SPD	Serial Port Data Input / Output (open drain) This pin functions as the bi-directional data pin of the serial port. External pull-up resistor is required.
32	In	SPC	Serial Port Clock Input (open drain) This pin functions as the clock pin of the serial port. External pull-up resistor is required.
22	Out	DAC0	CVBS or S-video output Full swing is up to 1.3v.
20	Out	DAC1	CVBS or S-video output Full swing is up to 1.3v.
24	In	ISET	Current Set Resistor Input This pin sets the DAC current. A 1.2k Ω , 1% tolerance resistor should be connected between this pin and AGND_DAC using short and wide traces.
28	In	XI	Crystal Input / External Input For some situation of the slave mode, a parallel resonance crystal (± 20 ppm) should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI/FIN input.
29	Out	XO	Crystal Output For some situation of the slave mode, a parallel resonance crystal (± 20

Pin #	Type	Symbol	Description
			ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
39	In	GCLK	Graphics Controller Clock Input
40	Power	VDDIO	IO supply voltage (1.2-3.3V).
58	Power	DVDD	Digital supply voltage (1.8V).
7,11,30,38	Power	AVDD	Analog supply voltage (2.5-3.3V).
26	Power	AVDD_PLL	PLL supply voltage (1.8V).
17,21	Power	AVDD_DAC	DAC power supply (2.5-3.3V).
9,14	Power	VDDQ_MEM	SDRAM output buffer supply voltage (2.5V).
13,34	Power	VDD_MEM	SDRAM device supply voltage (2.5V).
57	Power	DGND	Digital supply ground.
6,10,27,37	Power	AGND	Analog supply ground.
25	Power	AGND_PLL	PLL supply ground.
19,23	Power	AGND_DAC	DAC supply ground.
8,15	Power	GNDQ_MEM	SDRAM output buffer supply ground.
12,35,36	Power	GND_MEM	SDRAM device supply ground.

Notes:

1. All the unused Data input pins should be pulled low with 10kΩ resistors or shorted to Ground directly.

2.0 Package Dimensions

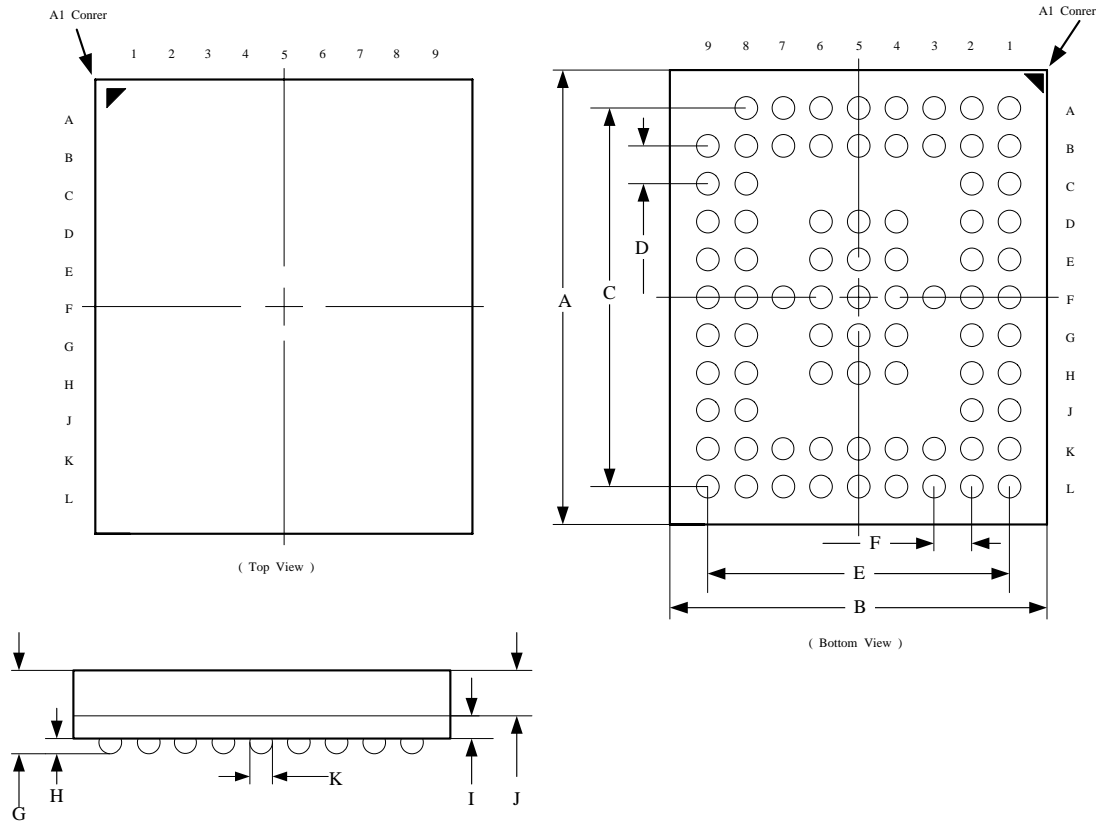


Figure 4: 80 Pin BGA Package

Table of Dimensions

No. of Leads		SYMBOL										
80 (5 X 6 mm)		A	B	C	D	E	F	G	H	I	J	K
Milli-meters	Min	6.00	5.00	5.00	0.50	4.00	0.50		0.22	0.30	0.60	0.30
	Max							1.20	0.30			

Notes:

All dimensions conform to JEDEC standard MO-216.

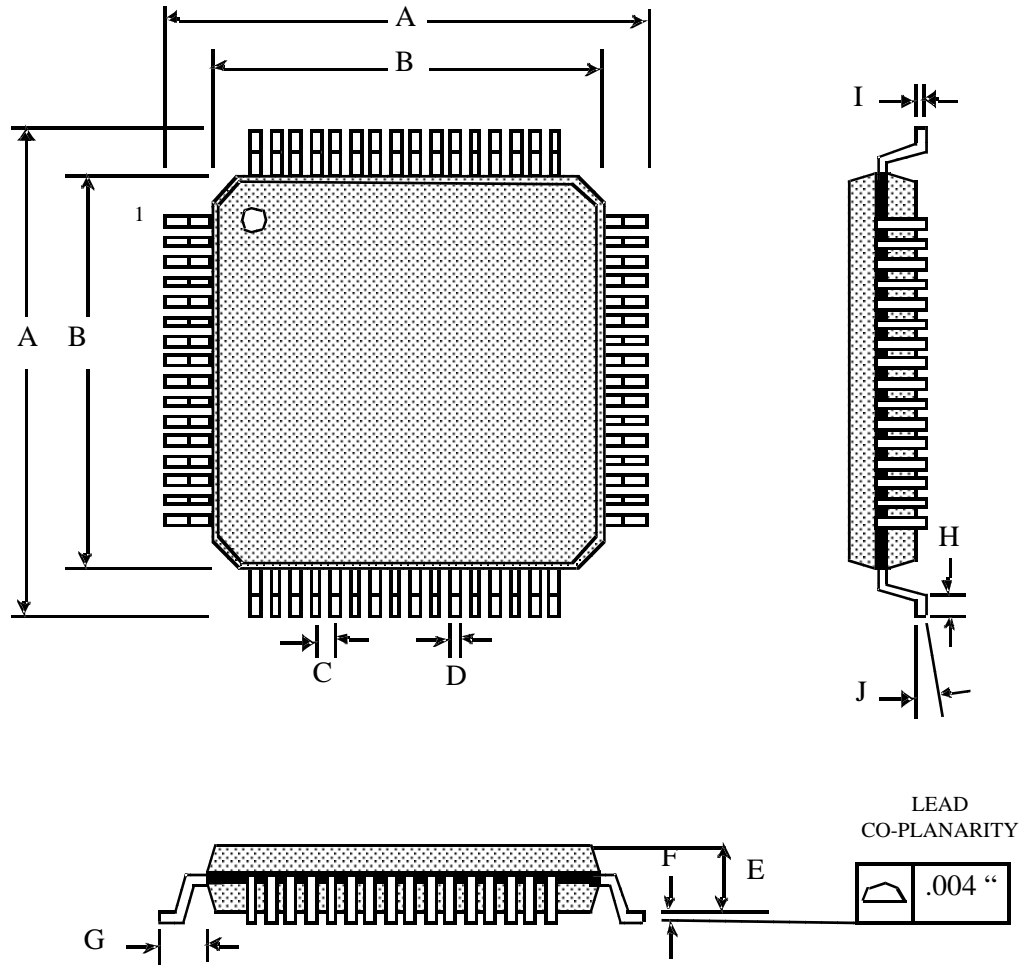


Figure 5: 64 Pin LQFP Package

Table of Dimensions

No. of Leads		SYMBOL									
64 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	K
Milli-meters	Min	12	10	0.50	0.17	1.35	0.05	1.00	0.45	0.09	0°
	Max				0.27	1.45	0.15		0.75	0.20	7°

Notes:

1. Conforms to JEDEC standard JESD-30 MS-026D.
2. Dimension B: Top Package body size may be smaller than bottom package size by as much as 0.15 mm.
3. Dimension B does not include allowable mold protrusions up to 0.25 mm per side.

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ORDERING INFORMATION			
Part Number	Package Type	Copy Protection	Operating Temperature Range
CH7028B-TF	64 LQFP, Lead-free	None	Commercial : -20 to 70°C
CH7028B-TF-TR	64 LQFP, Lead-free, Tape & reel	None	Commercial : -20 to 70°C
CH7028B-TFI	64 LQFP, Lead-free	None	Industrial : -40 to 85°C
CH7028B-TFI-TR	64 LQFP, Lead-free, Tape & reel	None	Industrial : -40 to 85°C
CH7028B-GF	80BGA, Lead-free	None	Commercial : -20 to 70°C
CH7028B-GF-TR	80BGA, Lead-free, Tape & reel	None	Commercial : -20 to 70°C

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