

# CD74HC40103, CD74HCT40103

## High Speed CMOS Logic 8-Stage Synchronous Down Counters

### Features

- Synchronous or Asynchronous Preset
- Cascadable in Synchronous or Ripple Mode
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC40103E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT40103E	-55 to 125	16 Ld PDIP	E16.3
CD74HC40103M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT40103M	-55 to 125	16 Ld SOIC	M16.15

#### NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

### Description

The Harris CD74HC40103 and CD74HCT40103 are manufactured with high speed silicon gate technology and consist of an 8-stage synchronous down counter with a single output which is active when the internal count is zero. The 40103 contains a single 8-bit binary counter. Each has control inputs for enabling or disabling the clock, for clearing the counter to its maximum count, and for presetting the counter either synchronously or asynchronously. All control inputs and the  $\overline{TC}$  output are active-low logic.

In normal operation, the counter is decremented by one count on each positive transition of the CLOCK (CP). Counting is inhibited when the  $\overline{TE}$  input is high. The  $\overline{TC}$  output goes low when the count reaches zero if the  $\overline{TE}$  input is low, and remains low for one full clock period.

When the  $\overline{PE}$  input is low, data at the P0-P7 inputs are clocked into the counter on the next positive clock transition regardless of the state of the  $\overline{TE}$  input. When the  $\overline{PL}$  input is low, data at the P0-P7 inputs are asynchronously forced into the counter regardless of the state of the  $\overline{PE}$ ,  $\overline{TE}$ , or CLOCK inputs. Input P0-P7 represent a single 8-bit binary word for the 40103. When the MR input is low, the counter is asynchronously cleared to its maximum count of 255<sub>10</sub>, regardless of the state of any other input. The precedence relationship between control inputs is indicated in the truth table.

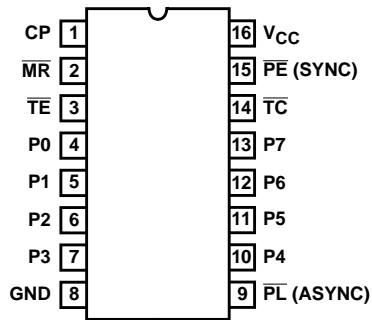
If all control inputs except  $\overline{TE}$  are high at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 100 or 256 clock pulses long.

The 40103 may be cascaded using the  $\overline{TE}$  input and the  $\overline{TC}$  output, in either a synchronous or ripple mode. These circuits possess the the low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits and can drive up to 10 LSTTL loads.

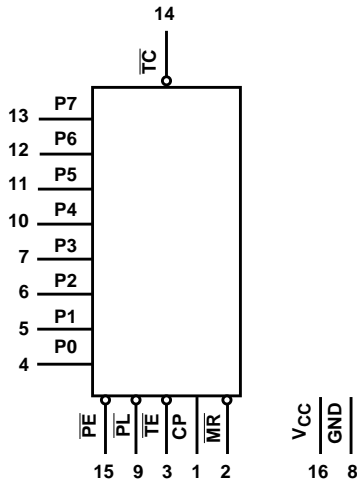
# CD74HC40103, CD74HCT40103

## Pinout

CD74HC40103, CD74HCT40103  
(PDIP, SOIC)  
TOP VIEW



## Functional Diagram



TRUTH TABLE

CONTROL INPUTS				PRESET MODE	ACTION
MR	PL	PE	TE		
1	1	1	1	Synchronous	Inhibit Counter
1	1	1	0		Count Down
1	1	0	X		Preset On Next Positive Clock Transition
1	0	X	X	Asynchronously	Preset Asynchronously
0	X	X	X		Clear to Maximum Count

**NOTE:**

1 = High Level.

0 = Low Level.

X = Don't Care.

Clock connected to clock input.

Synchronous Operation: changes occur on negative-to-positive clock transitions.

Load Inputs: MSB = P7, LSB = P0.

## CD74HC40103, CD74HCT40103

### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

### Thermal Information

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package .....	90
SOIC Package .....	160
Maximum Junction Temperature .....	$150^{\circ}C$
Maximum Storage Temperature Range .....	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	$300^{\circ}C$ (SOIC - Lead Tips Only)

### Operating Conditions

Temperature Range, $T_A$ .....	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	-	-	-	-	-	-	-	-	-	V
			4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	6	-	-	8	-	80	-	160	$\mu A$

**CD74HC40103, CD74HCT40103**

**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> and GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE: For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

INPUT	UNIT LOADS (NOTE)
P0-P7	0.20
$\overline{TE}$ , $\overline{MR}$	0.40
CP	0.60
$\overline{PE}$	0.80
$\overline{PL}$	1.35

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

**Prerequisite for Switching Specifications**

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>										
CP Pulse Width	t <sub>W</sub>	2	165	-	-	205	-	250	-	ns
		4.5	33	-	-	41	-	50	-	ns
		6	28	-	-	35	-	43	-	ns
$\overline{PL}$ Pulse Width	t <sub>W</sub>	2	125	-	-	155	-	190	-	ns
		4.5	25	-	-	31	-	38	-	ns
		6	21	-	-	26	-	32	-	ns

**CD74HC40103, CD74HCT40103**

**Prerequisite for Switching Specifications (Continued)**

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
MR Pulse Width	t <sub>W</sub>	2	125	-	-	135	-	190	-	ns
		4.5	25	-	-	31	-	38	-	ns
		6	21	-	-	26	-	32	-	ns
CP Max. Frequency (Note 4)	f <sub>CP(MAX)</sub>	2	3	-	-	2	-	2	-	MHz
		4.5	15	-	-	12	-	10	-	MHz
		6	18	-	-	14	-	12	-	MHz
P to CP Set-up Time	t <sub>SU</sub>	2	100	-	-	125	-	150	-	ns
		4.5	20	-	-	25	-	30	-	ns
		6	17	-	-	21	-	26	-	ns
PE to CP Set-up Time	t <sub>SU</sub>	2	75	-	-	95	-	110	-	ns
		4.5	15	-	-	19	-	22	-	ns
		6	13	-	-	16	-	19	-	ns
TE to CP Set-up Time	t <sub>SU</sub>	2	150	-	-	190	-	225	-	ns
		4.5	30	-	-	38	-	45	-	ns
		6	26	-	-	33	-	38	-	ns
P to CP Hold Time	t <sub>H</sub>	2	5	-	-	5	-	5	-	ns
		4.5	5	-	-	5	-	5	-	ns
		6	5	-	-	5	-	5	-	ns
TE to CP Hold Time	t <sub>H</sub>	2	0	-	-	0	-	0	-	ns
		4.5	0	-	-	0	-	0	-	ns
		6	0	-	-	0	-	0	-	ns
MR to CP Removal Time	t <sub>REM</sub>	2	50	-	-	65	-	75	-	ns
		4.5	10	-	-	13	-	15	-	ns
		6	9	-	-	11	-	13	-	ns
PE to CP Hold Time	t <sub>H</sub>	2	2	-	-	2	-	2	-	ns
		4.5	2	-	-	2	-	2	-	ns
		6	2	-	-	2	-	2	-	ns
<b>HCT TYPES</b>										
CP Pulse Width	t <sub>W</sub>	4.5	35	-	-	44	-	53	-	ns
PL Pulse Width	t <sub>W</sub>	4.5	43	-	-	54	-	65	-	ns
MR Pulse Width	t <sub>W</sub>	4.5	35	-	-	44	-	53	-	ns
CP Max. Frequency (Note 4)	f <sub>CP(MAX)</sub>	4.5	14	-	-	11	-	9	-	MHz
P to CP Set-up Time	t <sub>SU</sub>	4.5	24	-	-	30	-	36	-	ns
PE to CP Set-up Time	t <sub>SU</sub>	4.5	20	-	-	25	-	30	-	ns
TE to CP Set-up Time	t <sub>SU</sub>	4.5	40	-	-	50	-	60	-	ns
P to CP Hold Time	t <sub>H</sub>	4.5	5	-	-	5	-	5	-	ns
TE to CP Hold Time	t <sub>H</sub>	4.5	0	-	-	0	-	0	-	ns
MR to CP Removal Time	t <sub>REM</sub>	4.5	10	-	-	13	-	15	-	ns
PE to CP Hold Time	t <sub>H</sub>	4.5	2	-	-	2	-	2	-	ns

**CD74HC40103, CD74HCT40103**

**Switching Specifications** Input  $t_r, t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay CP to any $\overline{TC}$ (Async Preset)	$t_{PLH},$ $t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	300	-	375	-	450	ns
		$C_L = 50\text{pF}$	4.5	-	-	60	-	75	-	90	ns
		$C_L = 15\text{pF}$	5	-	25	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	51	-	64	-	77	ns
CP to $\overline{TC}$ (Sync Preset)	$t_{PLH},$ $t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	300	-	375	-	450	ns
		$C_L = 50\text{pF}$	4.5	-	-	60	-	75	-	90	ns
		$C_L = 15\text{pF}$	5	-	25	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	51	-	64	-	77	ns
$\overline{TE}$ to $\overline{TC}$	$t_{PLH},$ $t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	200	-	250	-	300	ns
		$C_L = 50\text{pF}$	4.5	-	-	40	-	50	-	60	ns
		$C_L = 15\text{pF}$	5	-	17	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	34	-	43	-	51	ns
$\overline{PL}$ to $\overline{TC}$	$t_{PLH},$ $t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	275	-	345	-	415	ns
		$C_L = 50\text{pF}$	4.5	-	-	55	-	69	-	83	ns
		$C_L = 15\text{pF}$	5	-	23	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	47	-	59	-	71	ns
$\overline{MR}$ to $\overline{TC}$	$t_{PLH},$ $t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	275	-	345	-	415	ns
		$C_L = 50\text{pF}$	4.5	-	-	55	-	69	-	83	ns
		$C_L = 15\text{pF}$	5	-	23	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	47	-	59	-	71	ns
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
		$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
		$C_L = 50\text{pF}$	6	-	-	13	-	16	-	19	ns
Input Capacitance	$C_I$	$C_L = 50\text{pF}$	-	-	-	10	-	10	-	10	pF
CP Maximum Frequency	$f_{MAX}$	$C_L = 15\text{pF}$	5	-	25	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 5, 6)	$C_{PD}$	-	5	-	25	-	-	-	-	-	pF
<b>HCT TYPES</b>											
Propagation Delay CP to $\overline{TC}$ (Async Preset)	$t_{PLH},$ $t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	60	-	75	-	90	ns
		$C_L = 15\text{pF}$	5	-	25	-	-	-	-	-	ns
$\overline{CE}$ to $\overline{TC}$ (Sync Preset)	$t_{PLH},$ $t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	63	-	79	-	95	ns
		$C_L = 15\text{pF}$	5	-	26	-	-	-	-	-	ns
$\overline{TE}$ to $\overline{TC}$	$t_{PLH},$ $t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	50	-	63	-	75	ns
		$C_L = 15\text{pF}$	5	-	21	-	-	-	-	-	ns
$\overline{PL}$ to $\overline{TC}$	$t_{PLH},$ $t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	68	-	85	-	102	ns
		$C_L = 15\text{pF}$	5	-	28	-	-	-	-	-	ns

## CD74HC40103, CD74HCT40103

### Switching Specifications Input $t_r$ , $t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{MR}$ to $\overline{TC}$	$t_{PLH}$ , $t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	55	-	69	-	83	ns
		$C_L = 15\text{pF}$	5	-	23	-	-	-	-	-	ns
Output Transition Time	$t_{THL}$ , $t_{TLH}$	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	$C_{IN}$	$C_L = 50\text{pF}$	-	-	-	10	-	10	-	10	pF
CP Maximum Frequency	$f_{MAX}$	$C_L = 15\text{pF}$	5	-	25	-	-	-	-	-	MHz
Power Dissipation Capacitance (Notes 5, 6)	$C_{PD}$	-	5	-	27	-	-	-	-	-	pF

#### NOTES:

- Noncascaded operation only. With cascaded counters clock-to-terminal count propagation delays, count enables ( $\overline{PE}$  or  $\overline{TE}$ )-to-clock SET UP TIMES, and count enables ( $\overline{PE}$  or  $\overline{TE}$ )-to-clock HOLD TIMES determine maximum clock frequency. For example, with these HC devices:

$$C_P f_{MAX} = \frac{1}{\text{CP-to-}\overline{TC} \text{ prop delay} + \overline{TE}\text{-to-CP Setup Time} + \overline{TE}\text{-to-CP Hold Time}} = \frac{1}{60 + 30 + 0} \approx 11\text{MHz}$$

- $C_{PD}$  is used to determine the dynamic power consumption, per package.
- $P_D = V_{CC}^2 f_i + C_L V_{CC}^2 f_o$  where  $f_i$  = Input Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage,  $f_o$  = Output Frequency.

### Timing Diagrams

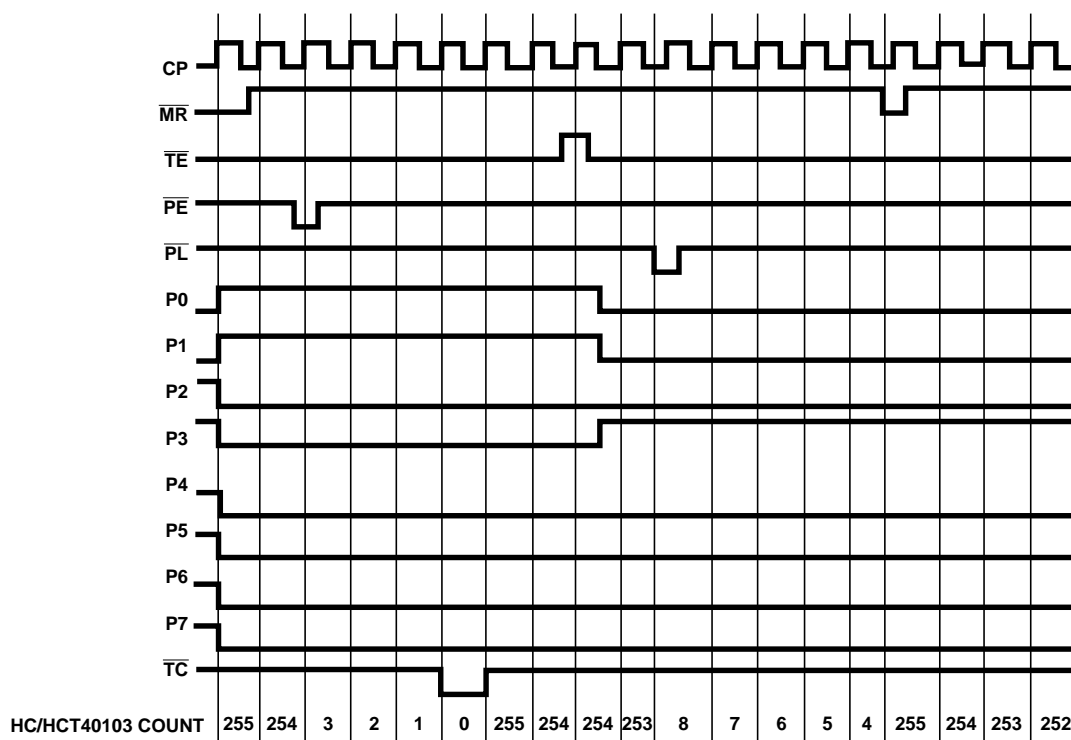


FIGURE 2.

Test Circuits and Waveforms

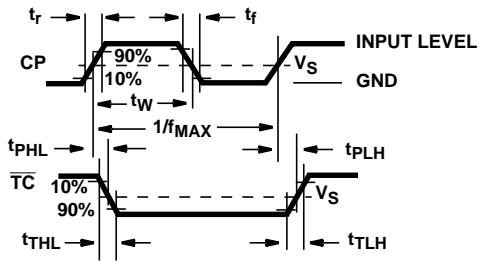


FIGURE 3.

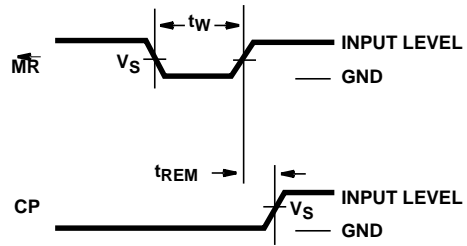


FIGURE 4.

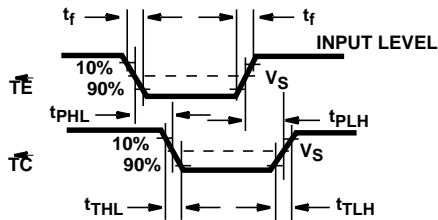


FIGURE 5.

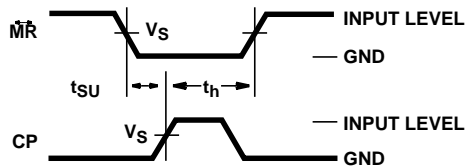


FIGURE 6.

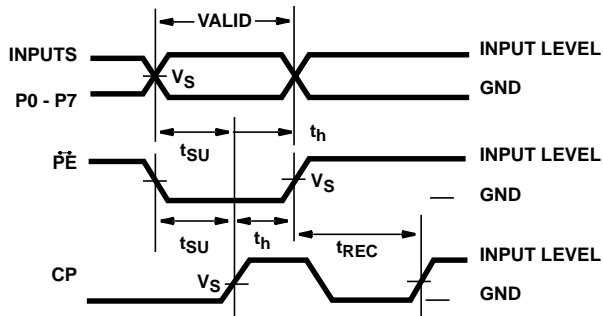


FIGURE 7.

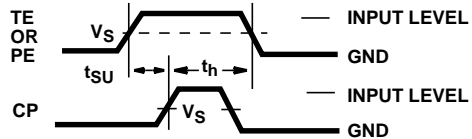
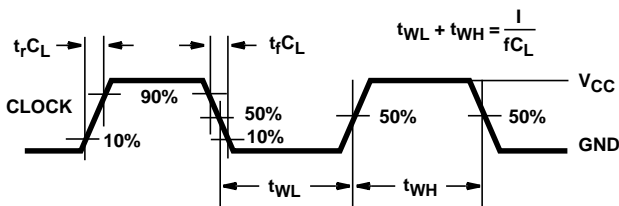
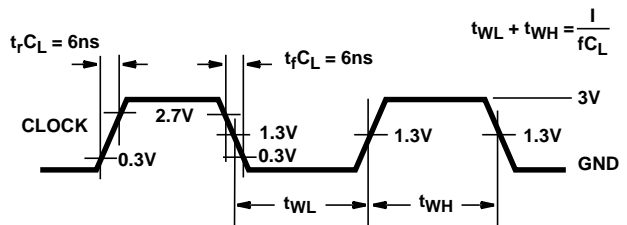


FIGURE 8.



NOTE: Outputs should be switching from 10% VCC to 90% VCC in accordance with device truth table. For fMAX, input duty cycle = 50%.

FIGURE 9. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10% VCC to 90% VCC in accordance with device truth table. For fMAX, input duty cycle = 50%.

FIGURE 10. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



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