



BT131 series

Triacs logic level

Rev. 08 — 9 September 2005

Product data sheet

1. Product profile

1.1 General description

Passivated, sensitive gate triacs in a SOT54 plastic package

1.2 Features

- Designed to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

1.3 Applications

- General purpose switching and phase control

1.4 Quick reference data

- $V_{\text{DRM}} \leq 600 \text{ V}$ (BT131-600)
- $V_{\text{DRM}} \leq 800 \text{ V}$ (BT131-800)
- $I_{\text{T(RMS)}} \leq 1 \text{ A}$
- $I_{\text{TSM}} \leq 12.5 \text{ A}$

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	main terminal 2 (T2)	 SOT54 (TO-92)	 sym051
2	gate (G)		
3	main terminal 1 (T1)		

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
BT131-600	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54
BT131-800			

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage				
	BT131-600		[1] -	600	V
	BT131-800		-	800	V
$I_{\text{T(RMS)}}$	RMS on-state current	all conduction angles; $T_{\text{lead}} = 51.2\text{ °C}$; see Figure 1 , 4 and 5	-	1	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_j = 25\text{ °C}$ prior to surge; see Figure 2 and 3			
		$t = 20\text{ ms}$	-	12.5	A
		$t = 16.7\text{ ms}$	-	13.8	A
I^2t	I^2t for fusing	$t = 10\text{ ms}$	-	1.28	A^2s
dl_{T}/dt	rate of rise of on-state current	$I_{\text{TM}} = 1.5\text{ A}$; $I_{\text{G}} = 20\text{ mA}$; $dl_{\text{G}}/dt = 200\text{ mA}/\mu\text{s}$			
		T2+ G+	-	50	$\text{A}/\mu\text{s}$
		T2+ G-	-	50	$\text{A}/\mu\text{s}$
		T2- G-	-	50	$\text{A}/\mu\text{s}$
		T2- G+	-	10	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	+150	$^{\circ}\text{C}$
T_j	junction temperature		-	125	$^{\circ}\text{C}$

[1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/ μs .

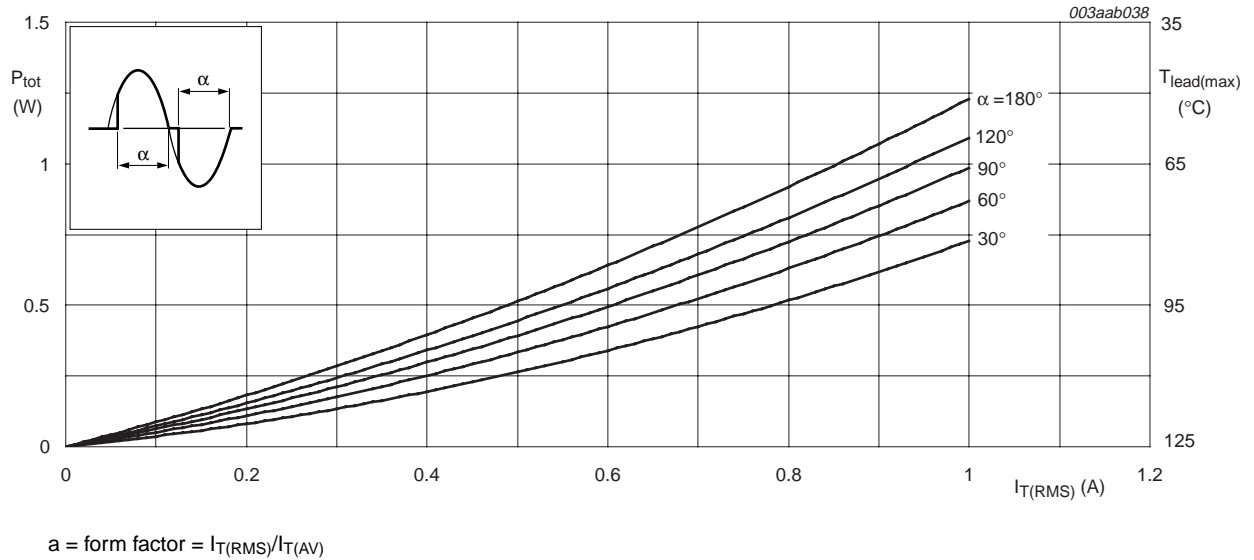


Fig 1. Total power dissipation as a function of average on-state current; maximum values

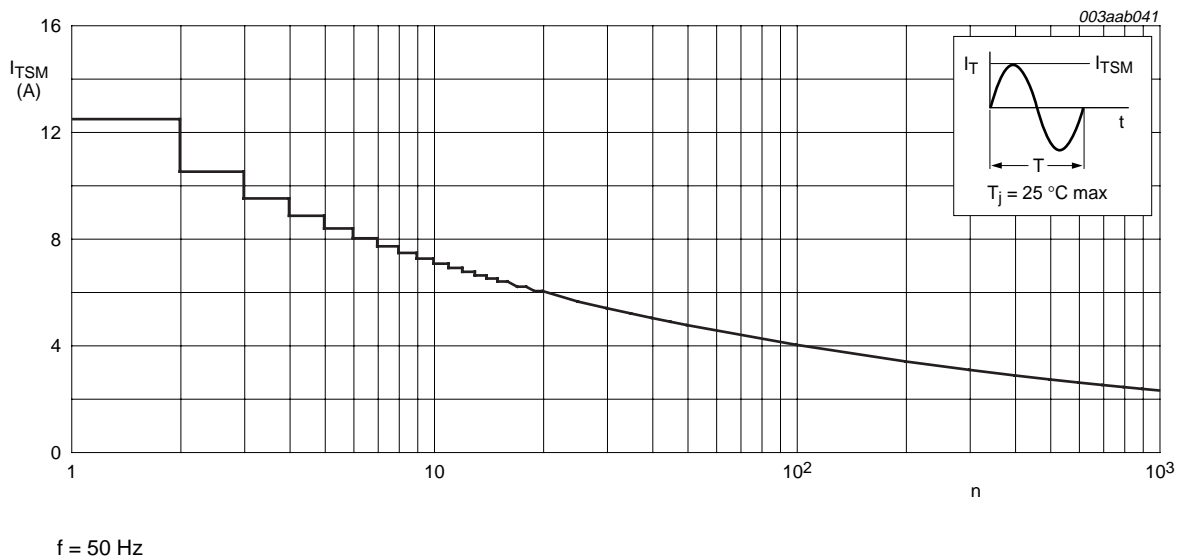
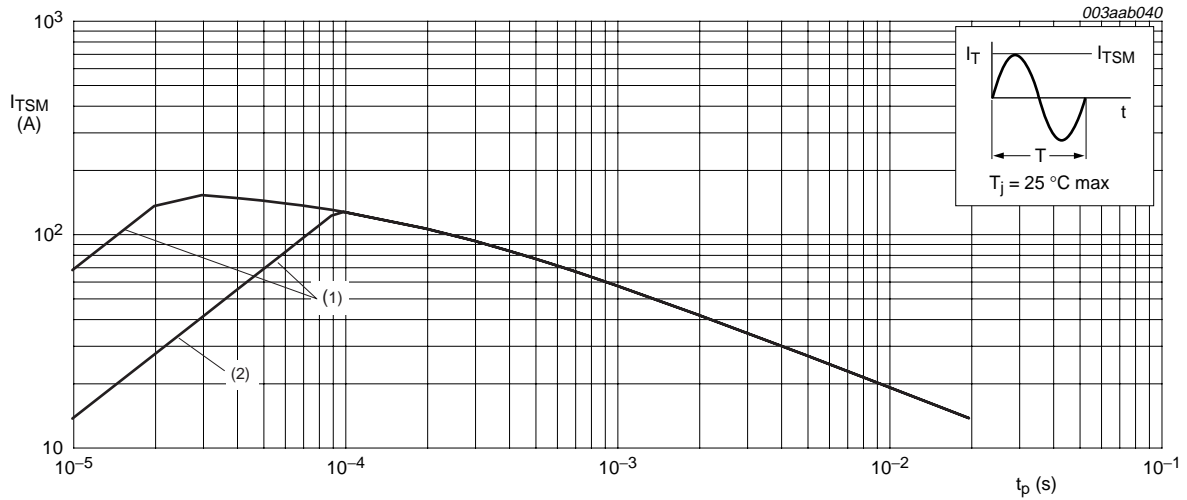


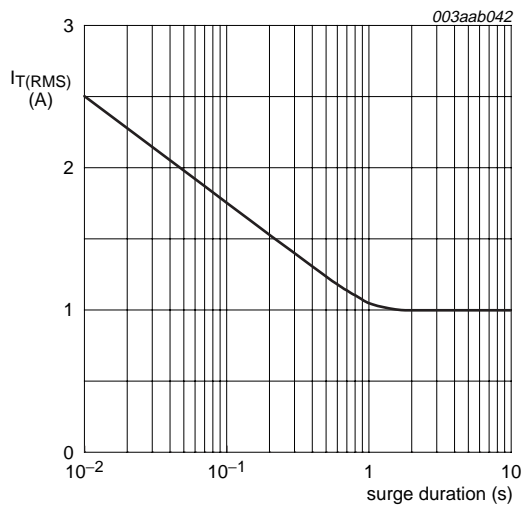
Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20\text{ ms}$

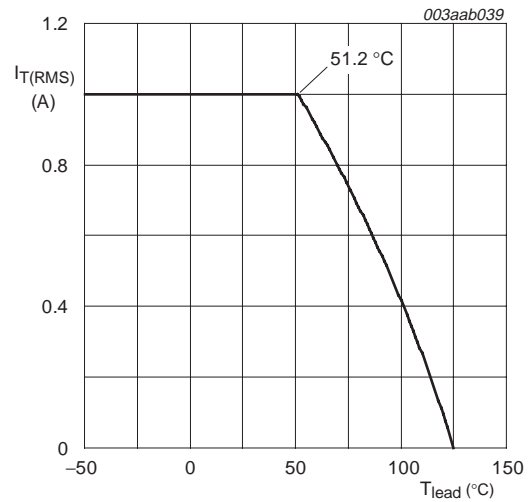
- (1) dI_T/dt limit
- (2) T2- G+ quadrant

Fig 3. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values



$f = 50\text{ Hz}; T_{lead} \leq 51.2\text{ °C}$

Fig 4. RMS on-state current as a function of surge duration, for sinusoidal currents; maximum values



(1) $T_{lead} = 51.2\text{ °C}$

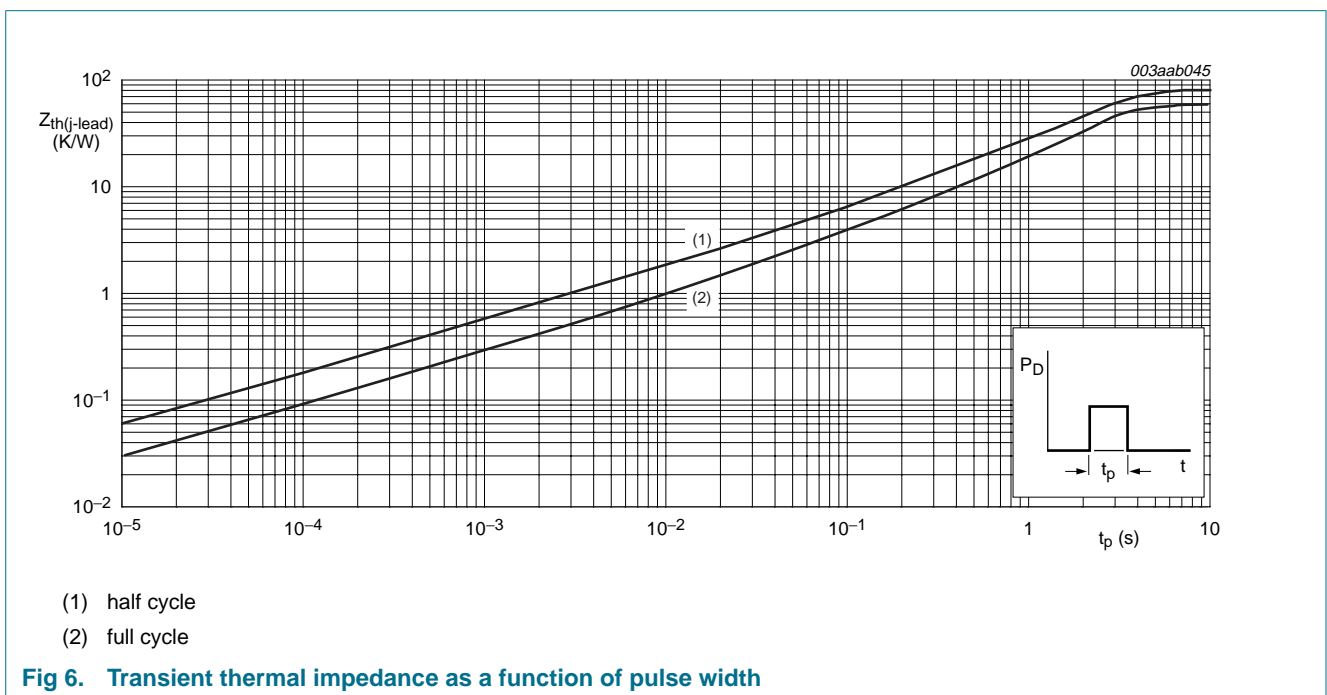
Fig 5. RMS on-state current as a function of lead temperature; maximum values

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle	-	-	60	K/W
		half cycle	-	-	80	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	see Figure 6	[1] -	150	-	K/W

[1] Mounted on a printed-circuit board; lead length = 4 mm



6. Characteristics

Table 5: Characteristics

$T_j = 25\text{ °C}$ unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; see Figure 8				
		T2+ G+	-	0.4	3	mA
		T2+ G-	-	1.3	3	mA
		T2- G-	-	1.4	3	mA
		T2- G+	-	3.8	7	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_{GT} = 100\text{ mA}$; see Figure 10				
		T2+ G+	-	1.2	5	mA
		T2+ G-	-	4	8	mA
		T2- G-	-	1	5	mA
		T2- G+	-	2.5	8	mA
I_H	holding current	$V_D = 12\text{ V}$; $I_{GT} = 100\text{ mA}$; see Figure 11	-	1.3	5	mA
V_T	on-state voltage	$I_T = 1.4\text{ A}$; see Figure 9	-	1.2	1.5	V
V_{GT}	gate trigger voltage	$I_T = 10\text{ mA}$; gate open circuit; see Figure 7				
		$V_D = 12\text{ V}$; $I_{GT} = 100\text{ mA}$	-	0.7	1.5	V
		$V_D = 400\text{ V}$; $I_{GT} = 100\text{ mA}$; $T_j = 125\text{ °C}$	0.2	0.3	-	V
I_D	off-state current	$V_D = V_{DRM(max)}$; $T_j = 125\text{ °C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}$; $T_j = 125\text{ °C}$; exponential waveform; $R_{GK} = 1\text{ k}\Omega$; see Figure 12	10	20	-	V/ μ s
dV_{com}/dt	rate of change of commutating current	$V_{DM} = 400\text{ V}$; $T_j = 125\text{ °C}$; $dl_{com}/dt = 0.5\text{ A/ms}$	2	-	-	V/ μ s
t_{gt}	gate-controlled turn-on time	$I_{TM} = 1.5\text{ A}$; $V_D = V_{DRM(max)}$; $I_G = 100\text{ mA}$; $dl_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	μ s

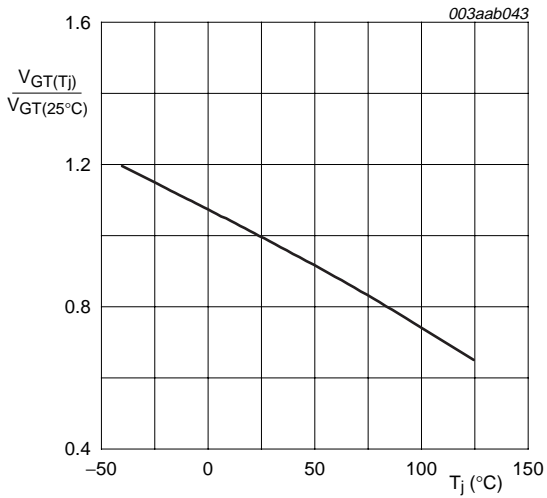
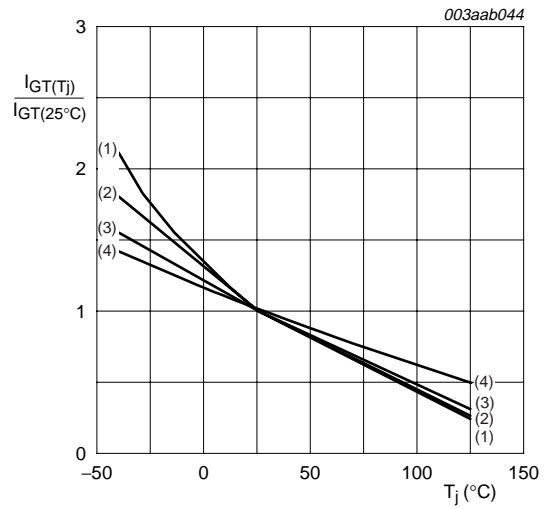
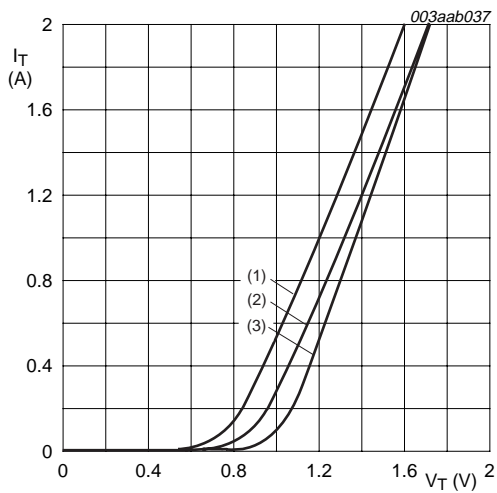


Fig 7. Normalized gate trigger voltage as a function of junction temperature



- (1) T2- G+
- (2) T2- G-
- (3) T2+ G-
- (4) T2+ G+

Fig 8. Normalized gate trigger current as a function of junction temperature



$V_o = 0.92 \text{ V}$
 $R_s = 0.4 \text{ } \Omega$.

- (1) $T_j = 125 \text{ }^\circ\text{C}$; typical values
- (2) $T_j = 125 \text{ }^\circ\text{C}$; maximum values
- (3) $T_j = 25 \text{ }^\circ\text{C}$; maximum values

Fig 9. On-state current characteristics

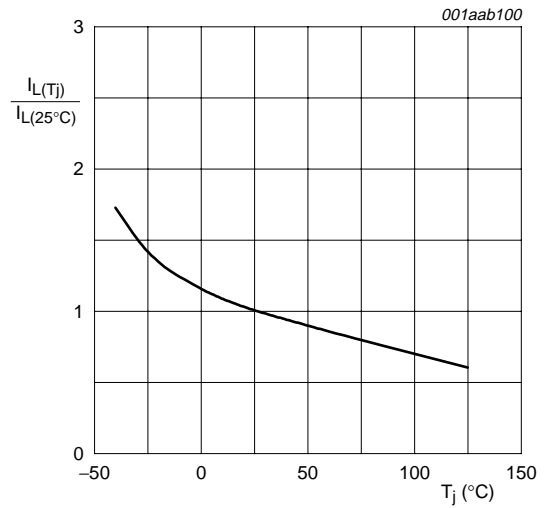
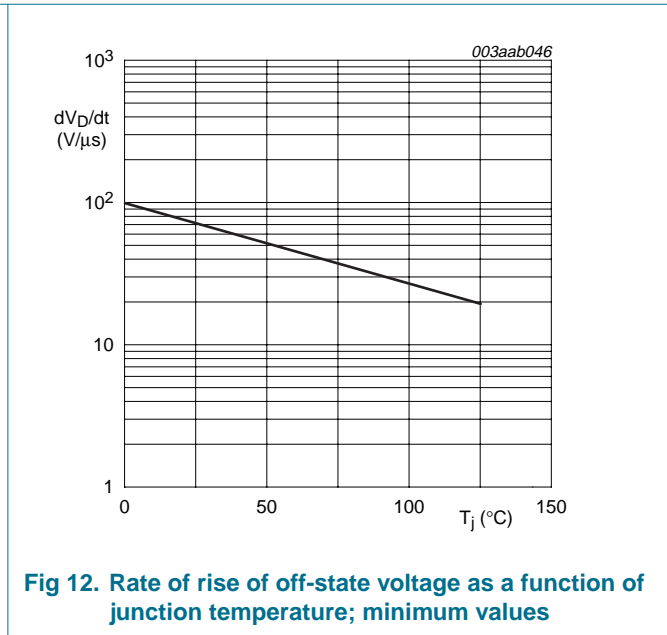
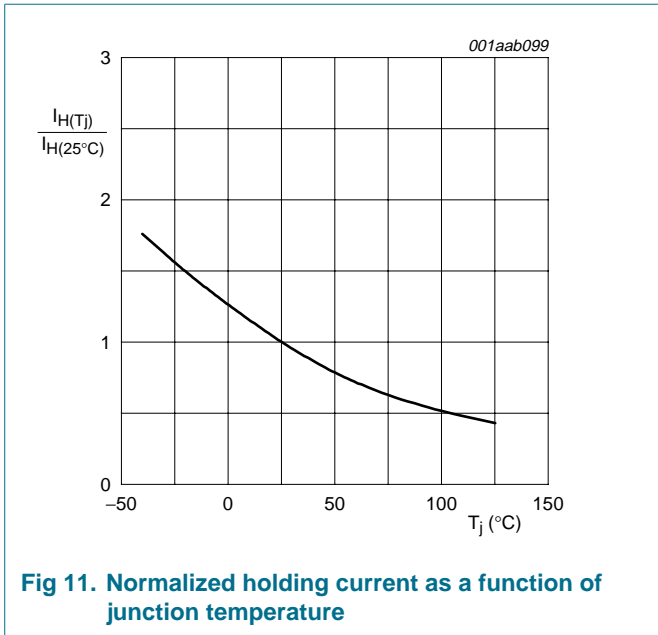


Fig 10. Normalized latching current as a function of junction temperature



7. Package information

Epoxy meets requirements of UL94 V-0 at 1/8 inch.

8. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

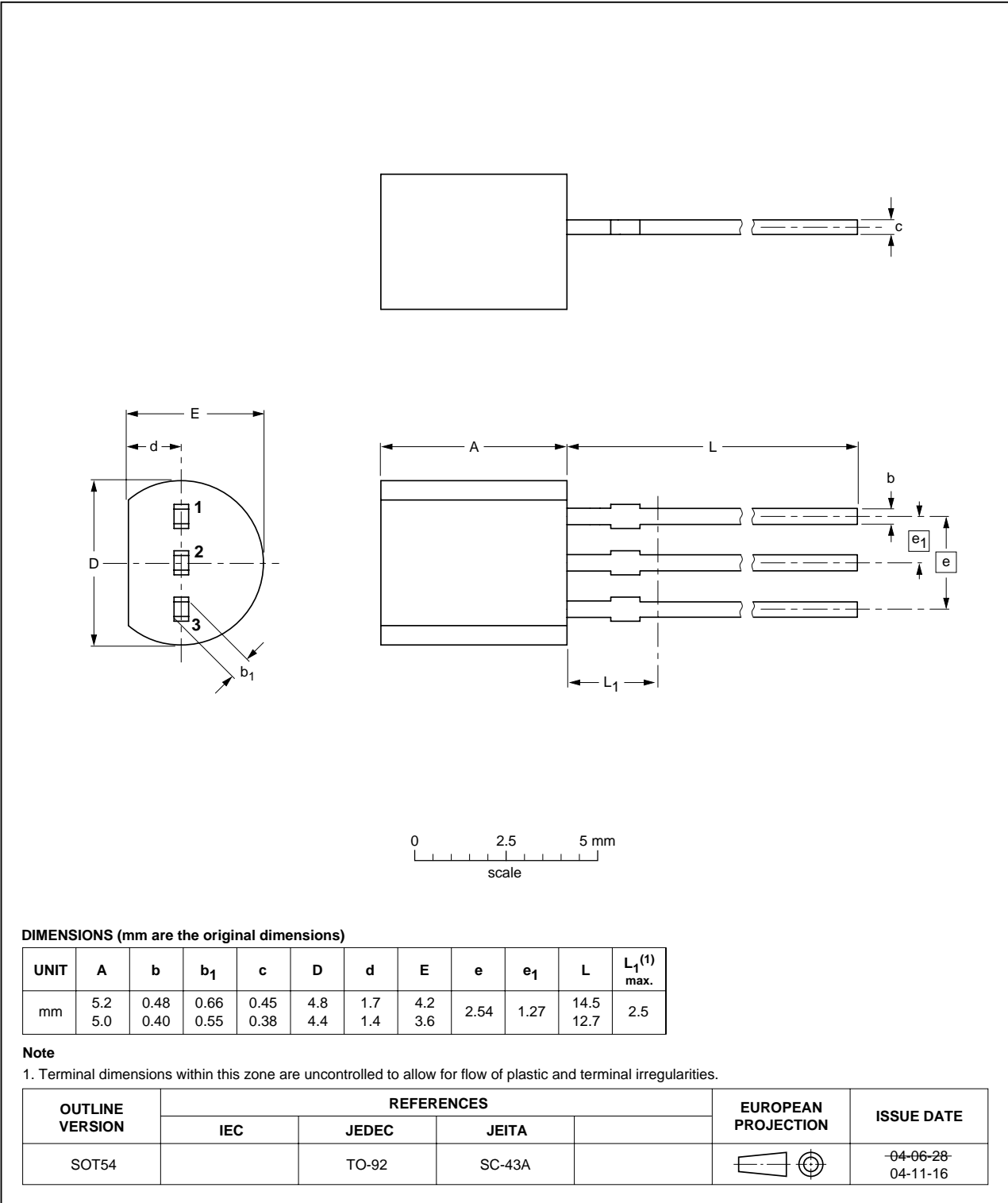


Fig 13. Package outline SOT54 (TO-92)

9. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
BT131_SER_8	20050909	Product data sheet	-	-	BT131_SER_7
Modifications:	<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.• Figure 5: corrected				
BT131_SER_7	20040101	Product specification	-	-	BT131_SER_6
BT131_SER_6	20030801	Product specification	-	-	BT131_SER_5
BT131_SER_5	20001201	Product specification	-	-	BT131_SER_4
BT131_SER_4	20000501	Product specification	-	-	BT131_SER_3
BT131_SER_3	19980401	Product specification	-	-	-

10. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
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