

DATA SHEET

BS250

P-channel enhancement mode
vertical D-MOS transistor

Product specification
File under Discrete Semiconductors, SC13b

April 1995

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DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in TO-92 variant envelope and intended for use in relay, high-speed and line-transformer drivers.

FEATURES

- Low $R_{DS(on)}$
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

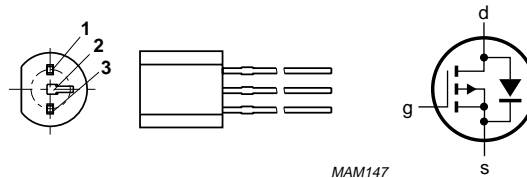
QUICK REFERENCE DATA

Drain-source voltage	$-V_{DS}$	max.	45 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$	P_{tot}	max.	0.83 W
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	$R_{DS(on)}$	typ. max.	9 Ω 14 Ω
Transfer admittance $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$	$ Y_{fs} $	typ.	125 mS

PINNING - TO-92 VARIANT

- 1 = source
- 2 = gate
- 3 = drain

PIN CONFIGURATION



Note: Various pinout configurations available.

Fig.1 Simplified outline and symbol.

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$-V_{DS}$	max.	45 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	$-I_D$	max.	0.25 A
Drain current (peak value)	$-I_{DM}$	max.	0.5 A
Total power dissipation up to $T_{amb} = 25\text{ }^\circ\text{C}$ (note 1)	P_{tot}	max.	0.83 W
Storage temperature range	T_{stg}		-65 to + 150 $^\circ\text{C}$
Junction temperature	T_j	max.	150 $^\circ\text{C}$

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j-a}$	=	150 K/W
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Note

1. Transistor mounted on printed-circuit board, max. lead length 4 mm.

CHARACTERISTICS

 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

Drain-source breakdown voltage $-I_D = 100\text{ }\mu\text{A}; V_{GS} = 0$	$-V_{(BR)DSS}$	min.	45 V
Drain-source leakage current $-V_{DS} = 25\text{ V}; V_{GS} = 0$	$-I_{DSS}$	max.	0.5 μA
Gate-source leakage current $-V_{GS} = 15\text{ V}; V_{DS} = 0$	$-I_{GSS}$	max.	20 nA
Gate threshold voltage $-I_D = 1\text{ mA}; V_{DS} = V_{GS}$	$-V_{GS(th)}$	min. max.	1.0 V 3.5 V
Drain-source ON-resistance $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$	$R_{DS(on)}$	typ. max.	9 Ω 14 Ω
Transfer admittance $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$	$ Y_{fs} $	typ.	125 mS
Input capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{iss}	typ. max.	30 pF 45 pF
Output capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{oss}	typ. max.	20 pF 30 pF
Feedback capacitance at $f = 1\text{ MHz}$ $-V_{DS} = 10\text{ V}; V_{GS} = 0$	C_{rss}	typ. max.	5 pF 10 pF

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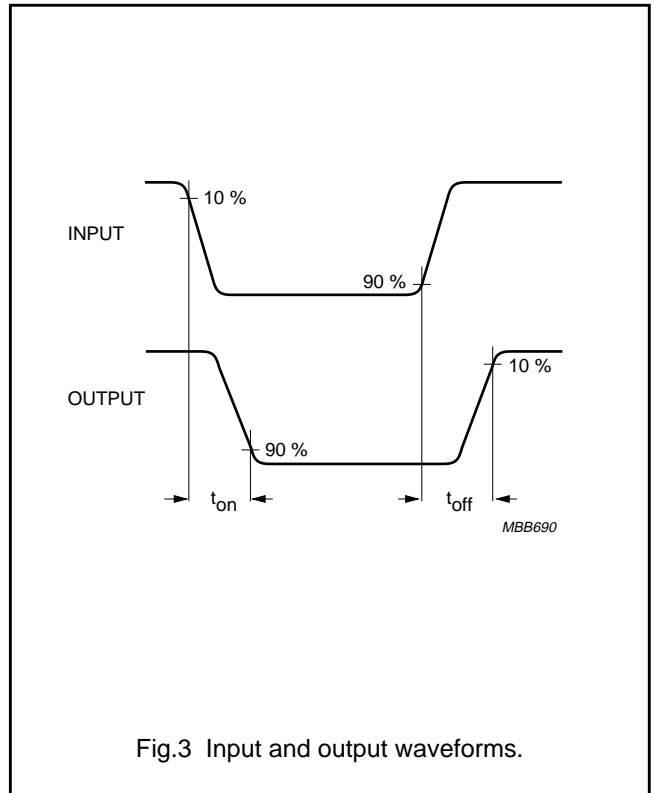
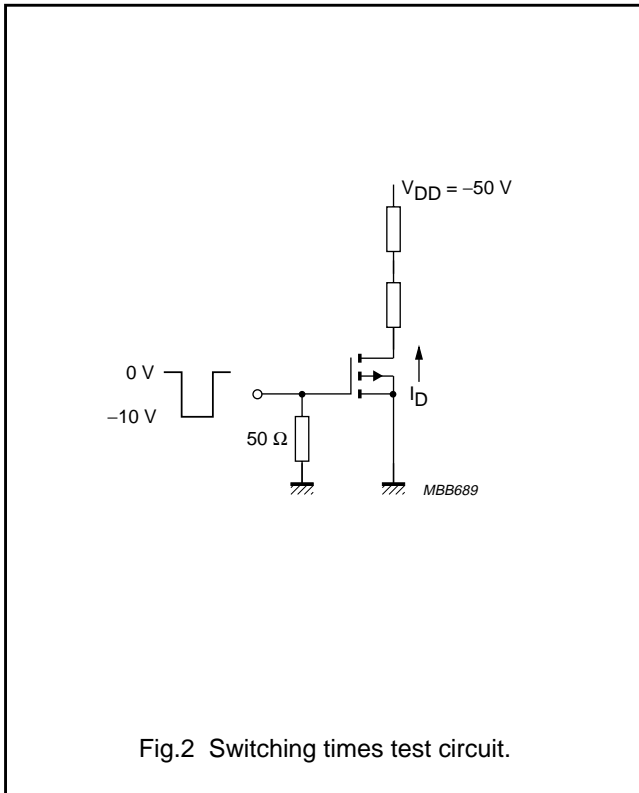
Switching times (see Figs 2 and 3)

$-I_D = 200 \text{ mA}$; $-V_{DD} = 40 \text{ V}$; $-V_{GS} = 0 \text{ to } 10 \text{ V}$

t_{on}
 t_{off}

typ.
typ.

4 ns
10 ns



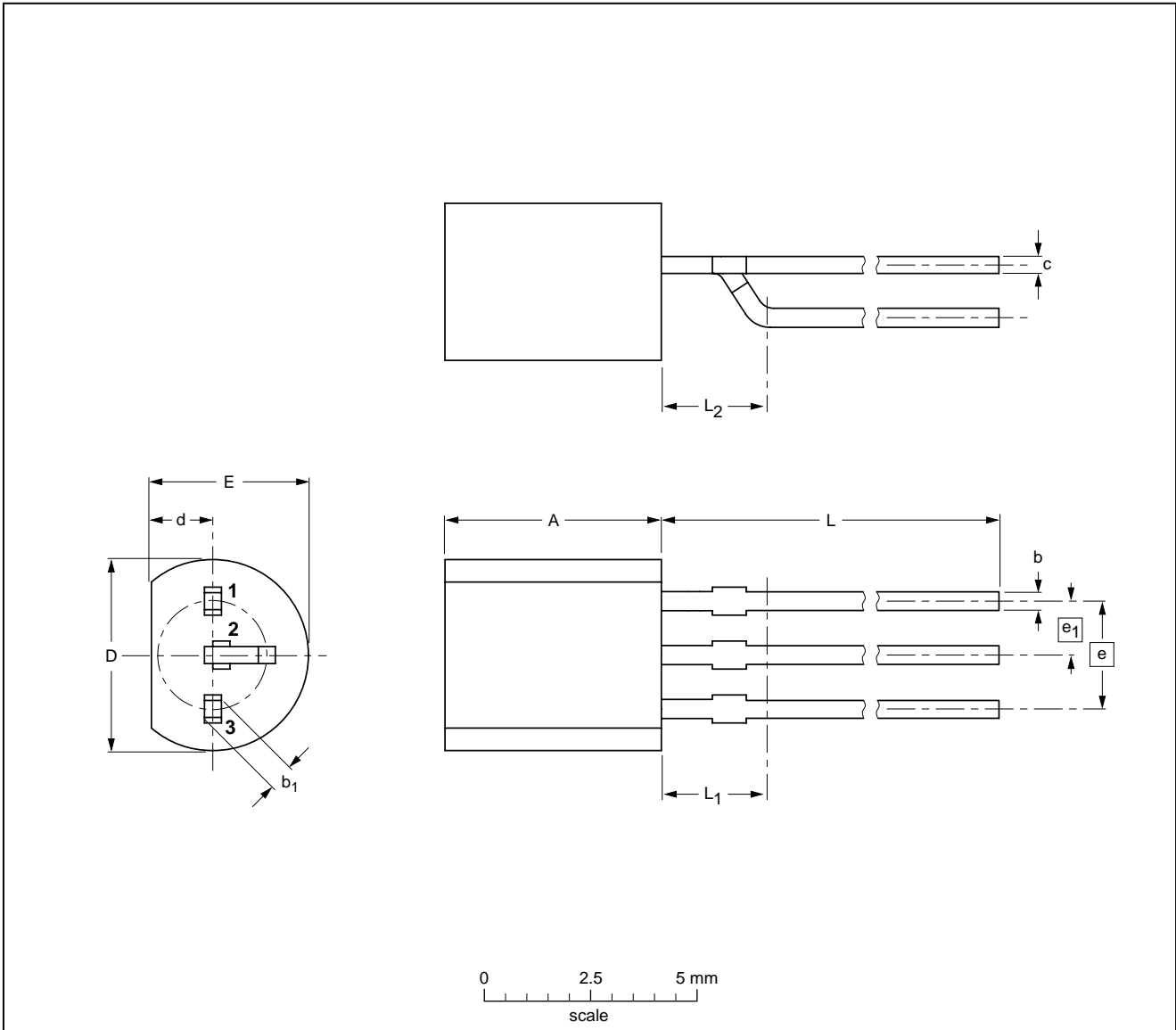
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PACKAGE OUTLINES

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max	L ₂ max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT54 variant		TO-92	SC-43		97-04-14

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BS250**DEFINITIONS**

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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