BGW200EG

IEEE 802.11b System-in-Package

Rev. 01 — 18 July 2007 Product data sheet

1. General description

The BGW200EG is a plug-and-play System-in-Package (SiP) for IEEE Std 802.11b - 1999 Wireless Local Area Network (WLAN) intended for embedded and mobile applications.

The BGW200EG comprises an ARM7TDMI microcontroller with SRAM and ROM, an 802.11b Medium Access Controller (MAC) and compliant modem, a highly integrated RF transceiver, a linear power amplifier and an RF front-end with integrated baluns, filters and switches.

The power management and supply decoupling are fully incorporated in the BGW200EG resulting in a low height, small form factor implementation of the complete 802.11b function from the host interface to the antenna(s).

2. Features

2.1 General

- Plug-and-play IEEE Std 802.11b - 1999 WLAN System-in-Package (SiP)
- Includes all the baseband and radio functions, from host interface up to antenna, needs only external antenna and reference clock
- Support for IEEE 802.11e and Wi-Fi Multi Media (WMM) quality of service enhancements (see Section 2.6)
- Support for IEEE 802.11i and Wi-Fi Protected Access (WPA) security enhancements
- Zero host load; all WLAN functionality is implemented by the BGW200EG
- Small dimensions (10 mm × 15 mm × 1.3 mm) HLLGA68 package
- Lead-free package, RoHS 2006 compliant
- Moisture sensitivity level 4
- Ambient temperature: −30 °C to +85 °C

2.2 Power management

- Supply voltage range:
  - Radio transceiver: 2.7 V to 3.0 V (can be extended to $V_{DD(PA)}$ + 0.6 V)
  - Power amplifier: 2.7 V to 3.0 V
  - Baseband digital parts: 1.65 V to 1.95 V
  - Baseband analog parts: 2.7 V to 3.0 V (can be extended to $V_{DD(PA)}$ + 0.6 V)
  - Baseband peripherals: 2.7 V to 3.0 V (can be extended to $V_{DD(PA)}$ + 0.6 V)
- Low power:
  - Internal or external low-frequency sleep clock
  - Sleep power consumption: 200 μW (typical)

- Receive power consumption: 480 mW (typical)
- Transmit power consumption (17 dBm output): 750 mW (typical)

2.3 Radio transceiver

- Receiver sensitivity (Packet Error Rate: PER = 8 %) at 11 Mbit/s data rate: –83 dBm
- Receiver maximum input power: 0 dBm
- RX blocking filter for suppression of Global System for Mobile communication (GSM) and Data Communication System (DCS) interference signals
- Receiver RF antenna diversity fully supported
- Transmitter maximum output power: 17 dBm (with 15 dB adjustable gain)
- Transmitter Error Vector Magnitude (EVM) for 11 Msymbol/s QPSK modulation: 17 % (RMS)
- Transmitter FCC compliant spurious emission spectrum:
  - Optional output power software back-off to guarantee FCC compliance in application for low data rates in channel 1 and channel 11
  - External filter required for 2nd harmonic suppression
- Internal shielding for better ElectroMagnetic Interference (EMI) immunity

2.4 Baseband hardware

- IEEE 802.11b PHY and MAC:
  - Decision feedback equalizer with > 200 ns multipath delay spread tolerance
  - Antenna diversity fully supported
  - Data rates up to 11 Mbit/s
  - WEP, TKIP, CCM and AES encryption and decryption engines
- Bluetooth coexistence interface:
  - Interfaces to a range of NXP Semiconductors Bluetooth modules
  - Hardware functionality to facilitate connection to 3rd-party Bluetooth solutions
  - Hardware support for IEEE 802.15.2 packet traffic arbitration recommendations
- Embedded 32-bit microcontroller:
  - ARM7TDMI-S RISC controller featuring low mW/MHz
  - Up to 66 MHz core clock speed at 1.8 V supply voltage
  - Instruction pre-fetch unit for improved performance
  - Embedded nonvolatile memory: 256-kbit ROM
  - Embedded volatile memory: 5 × 256-kbit SRAM
  - JTAG compliant in-circuit emulation interface
- Microcontroller peripherals:
  - SPI master/slave interface
  - SPI high-speed slave interface with DMA controller
  - SDIO interface with support for SPI, SD1 and SD4 modes
  - 11 general-purpose I/O pins
  - UART
  - Five 32-bit system timers
  - Watchdog timer

2.5 Software

- Microcontroller firmware
- IEEE 802.11b/e/i protocol firmware (see Section 2.6)
- WPA and WMM1 protocol firmware (see Section 2.6)
- Host drivers for the following operating systems:
  - WinCE 4.2/5.0
  - Embedded Linux
- Configuration utility

2.6 Reference

- The MAC implemented in the SA2443A is fully compliant with the relevant parts of the published IEEE 802.11 standard and further enhanced with changes detailed in the IEEE 802.11b published amendment. The MAC has also been designed to support the soon to be published IEEE 802.11e amendment as well as the proposed WMM1 standard. The flexible architecture should allow incorporation of any further changes to these amendments and proposed standards before ratification and publication.

3. Applications

- IEEE 802.11b WLAN
- Smart phone or feature phone with embedded WLAN
- Personal Digital Assistant (PDA) with embedded WLAN
- Voice over IP (VoIP) cordless phone
- Mobile gaming

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
BGW200EG/01	HLLGA68	plastic thermal enhanced low profile land grid array package; 68 lands; body 10 × 15 × 1.3 mm	SOT858-1

5. Block diagram

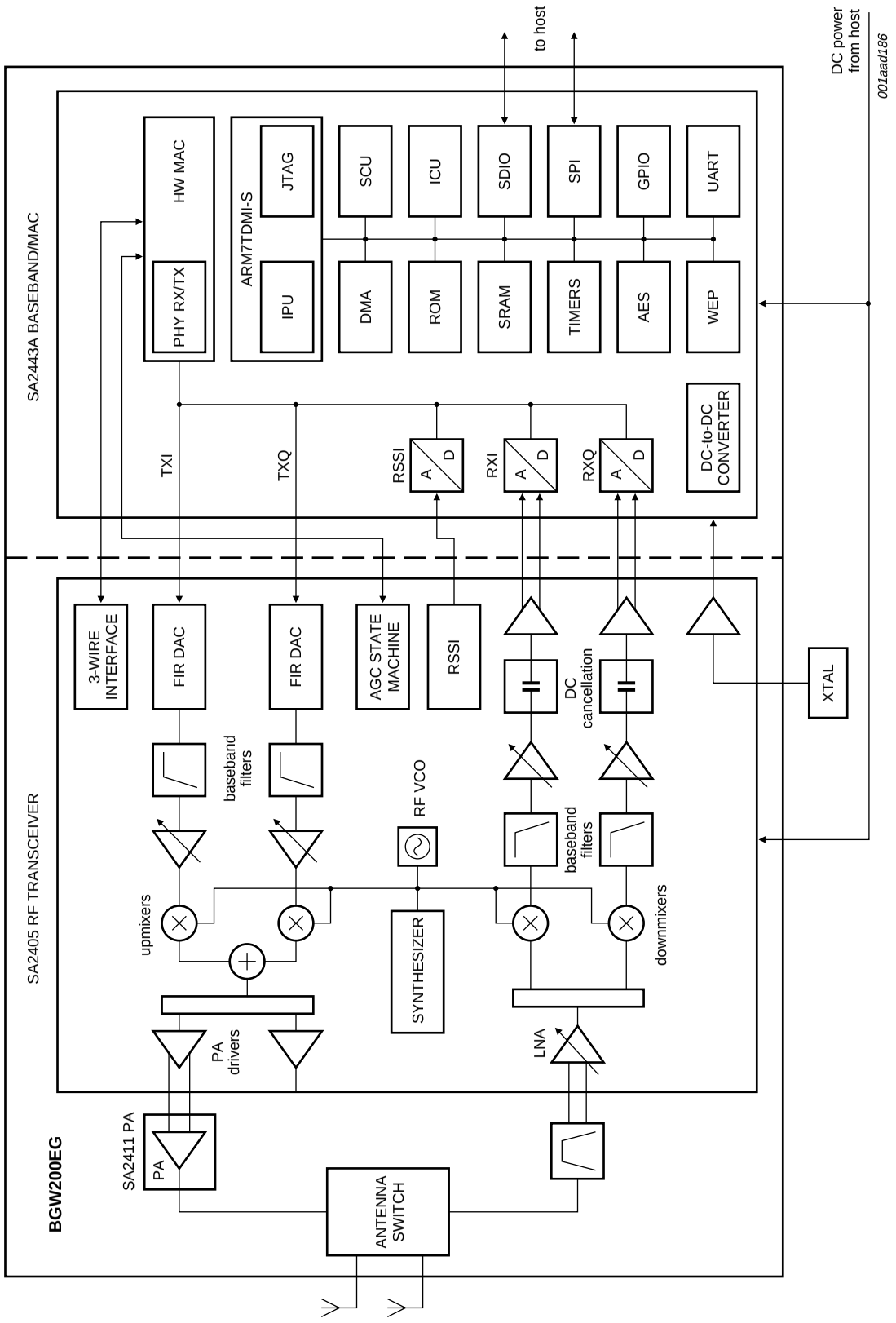
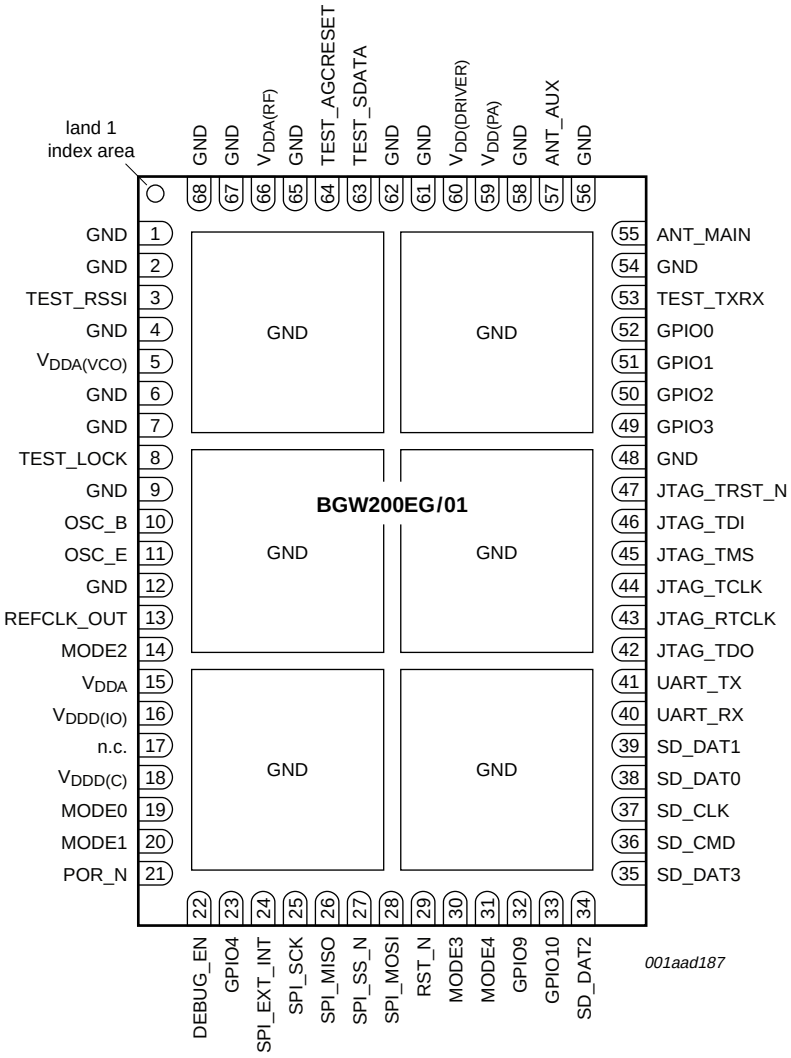


Fig 1. Block diagram

6. Pinning information

6.1 Pinning



Transparent top view

Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Circuit	Reset[1]	Supply	Description
SPI interface						
SPI_SCK	25	I/O; I	3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis	I, pull-down	$V_{DDD(IO)}$	SPI clock; bidirectional; 32 kHz sleep clock input
SPI_SS_N	27	I; I/O	3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis	I, pull-down	$V_{DDD(IO)}$	SPI slave select input; general-purpose I/O bit 6; bidirectional
SPI_EXT_INT	24	O; I/O	3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis	I, pull-down	$V_{DDD(IO)}$	SPI external interrupt output; general-purpose I/O bit 5; bidirectional
SPI_MISO	26	I/O	3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis	I, pull-down	$V_{DDD(IO)}$	SPI data (master in / slave out); bidirectional
SPI_MOSI	28	I/O	3-state; 1 ns slew rate; 4 mA; CMOS	I, pull-down	$V_{DDD(IO)}$	SPI data (master out / slave in); bidirectional
SDIO Interface						
SD_CLK	37	I; I	CMOS; hysteresis	-	$V_{DDD(IO)}$	SD clock input; 32 kHz clock input
SD_CMD	36	I/O	3-state; 1 ns slew rate; 4 mA; CMOS	I	$V_{DDD(IO)}$	SD command; bidirectional
SD_DAT0	38	I/O	3-state; 1 ns slew rate; 4 mA; CMOS	I	$V_{DDD(IO)}$	SD data bit 0; bidirectional
SD_DAT1	39	I/O	3-state; 1 ns slew rate; 4 mA; CMOS	I	$V_{DDD(IO)}$	SD data bit 1; bidirectional
SD_DAT2	34	I/O	3-state; 1 ns slew rate; 4 mA; CMOS	I	$V_{DDD(IO)}$	SD data bit 2; bidirectional
SD_DAT3	35	I/O	3-state; 1 ns slew rate; 4 mA; CMOS	I, pull-up	$V_{DDD(IO)}$	SD data bit 3; bidirectional
UART interface						
UART_RX	40	I; I/O	3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis	I, pull-down	$V_{DDD(IO)}$	UART receive input; general-purpose I/O bit 7; bidirectional
UART_TX	41	O; I/O	3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis	I, pull-down	$V_{DDD(IO)}$	UART transmit output; general-purpose I/O bit 8; bidirectional
Antenna RF ports						
ANT_MAIN	55	I/O	analog	-	-	RF main antenna port; 50 Ω
ANT_AUX	57	I	analog	-	-	RF auxiliary antenna port; 50 Ω
Test pins						
TEST_RSSI	3	O	analog; C_L = 100 pF	LOW	$V_{DDA(RF)}$	test pin for RF RSSI signal output
TEST_LOCK	8	O	CMOS; 4.5 mA	LOW	V_{DDA}	test pin for synthesizer lock indicator
TEST_TXRX	53	O	push-pull; 3 ns slew rate; 4 mA	LOW	$V_{DDD(IO)}$	test pin for RF transmit/receive select signal
TEST_SDATA	63	I/O	3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis	I, pull-down	$V_{DDD(IO)}$ or V_{DDA}	test pin for 3-wire bus data; bidirectional

Table 2. Pin description *...continued*

Symbol	Pin	Type	Circuit	Reset[1]	Supply	Description
TEST_AGCRESET	64	O	push-pull; 3 ns slew rate; 4 mA	LOW	$V_{DDD(IO)}$	test pin for RF AGC reset; output
REFCLK_OUT	13	O	CMOS	-	V_{DDA}	test pin for 44 MHz clock output
Bluetooth coexistence interface						
GPIO0	52	O; O; I/O	3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis	I, pull-down	$V_{DDD(IO)}$	WLAN arbitration signal output; HW MAC CCA output; general-purpose I/O bit 0; bidirectional
GPIO1	51	I; I/O	3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis	I, pull-down	$V_{DDD(IO)}$	BT arbitration signal input; general-purpose I/O bit 1; bidirectional
GPIO2	50	I; I/O	3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis	I, pull-down	$V_{DDD(IO)}$	BT high priority traffic indicator input; general-purpose I/O bit 2; bidirectional
GPIO3	49	O; I/O	3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis	I, pull-down	$V_{DDD(IO)}$	WLAN receive indicator output; general-purpose I/O bit 3; bidirectional
GPIO interface						
GPIO9	32	I/O	3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis	I, pull-down	$V_{DDD(IO)}$	general-purpose I/O bit 9; bidirectional
GPIO10	33	I/O	3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis	I, pull-down	$V_{DDD(IO)}$	general-purpose I/O bit 10; bidirectional
JTAG and debug interface						
JTAG_TCLK	44	I	CMOS; hysteresis; pull-up	-	$V_{DDD(IO)}$	JTAG clock input
JTAG_RTCLK	43	O	push-pull; 3 ns slew rate; 4 mA	LOW	$V_{DDD(IO)}$	synchronized JTAG clock output
JTAG_TMS	45	I	CMOS; hysteresis; pull-up	-	$V_{DDD(IO)}$	JTAG test mode select input
JTAG_TRST_N	47	I	CMOS; hysteresis; pull-up	-	$V_{DDD(IO)}$	JTAG reset input; active LOW
JTAG_TDI	46	I	CMOS; hysteresis; pull-up	-	$V_{DDD(IO)}$	JTAG test data input
JTAG_TDO	42	O	3-state; 3 ns slew rate; 4 mA	high-Z	$V_{DDD(IO)}$	JTAG test data output
DEBUG_EN	22	I	CMOS; hysteresis; pull-down	-	$V_{DDD(IO)}$	debug enable input
Miscellaneous						
OSC_B	10	I	analog	-	V_{DDA}	crystal oscillator / buffer input
OSC_E	11	O	analog	-	V_{DDA}	crystal oscillator output
GPIO4	23	I; I/O	3-state; 3 ns slew rate; 4 mA; CMOS; hysteresis	I, pull-down	$V_{DDD(IO)}$	32 kHz sleep clock input; general-purpose I/O bit 4; bidirectional
RST_N[2]	29	I	CMOS; hysteresis	-	$V_{DDD(IO)}$	system reset input; active LOW
POR_N	21	O	push-pull; 3 ns slew rate; 4 mA	LOW	$V_{DDD(IO)}$	power-on reset output; active LOW
MODE0	19	I	CMOS; hysteresis	-	$V_{DDD(IO)}$	load source 0 input
MODE1	20	I	CMOS; hysteresis	-	$V_{DDD(IO)}$	load source 1 input
MODE2	14	-	connected to ground	-	-	reserved for pin-compatibility with BGW211

Table 2. Pin description *...continued*

Symbol	Pin	Type	Circuit	Reset[1]	Supply	Description
MODE3	30	-	not connected	-	-	reserved for pin-compatibility with BGW211
MODE4	31	-	not connected	-	-	reserved for pin-compatibility with BGW211
n.c.	17	-	not connected	-	-	reserved for pin-compatibility with BGW211
Power supplies						
$V_{DDA(VCO)}$	5	-	-	-	-	VCO analog supply voltage
V_{DDA}	15	-	-	-	-	analog supply voltage
$V_{DDD(IO)}$	16	-	-	-	-	I/O digital supply voltage
$V_{DDD(C)}$	18	-	-	-	-	core digital supply voltage
$V_{DD(PA)}$	59	-	-	-	-	power amplifier supply voltage
$V_{DD(DRIVER)}$	60	-	-	-	-	driver supply voltage
$V_{DDA(RF)}$	66	-	-	-	-	RF analog supply voltage
GND	1	-	-	-	-	ground
GND	2	-	-	-	-	ground
GND	4	-	-	-	-	ground
GND	6	-	-	-	-	ground
GND	7	-	-	-	-	ground
GND	9	-	-	-	-	ground
GND	12	-	-	-	-	ground
GND	48	-	-	-	-	ground
GND	54	-	-	-	-	ground
GND	56	-	-	-	-	ground
GND	58	-	-	-	-	ground
GND	61	-	-	-	-	ground
GND	62	-	-	-	-	ground
GND	65	-	-	-	-	ground
GND	67	-	-	-	-	ground
GND	68	-	-	-	-	ground

[1] I = input mode.

[2] The RST_N pin should be linked to the POR_N pin; use of an external reset signal is not supported.

7. Functional description

7.1 General

The BGW200EG contains the following parts in one SiP (with embedded software):

- IEEE 802.11b RF transceiver
- IEEE 802.11b compliant modem
- IEEE 802.11b MAC
- ARM7TDMI-S microcontroller
- Static RAM (SRAM)
- Interface circuits
- Power management circuit

Together with a reference clock and antenna with harmonic filter, this device forms a complete WLAN solution. The system architecture is ideal for mobile products and requires no load on the host processor. The host sleeps while the WLAN listens for the beacon and is woken by the WLAN when appropriate.

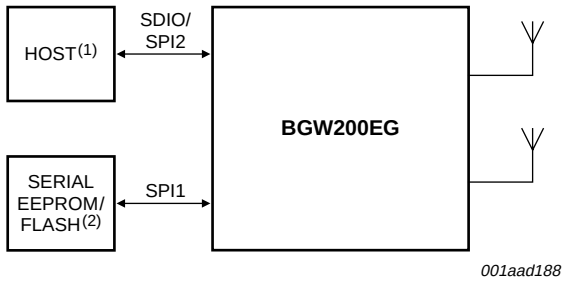
The BGW200EG is designed to be used for wireless links operating in the globally available ISM band, between 2402 MHz and 2497 MHz. The radio part is composed of a fully integrated, state-of-the-art, direct conversion transceiver chip, a linear power amplifier chip, an RX antenna filter for out-of-band blocking, TX/RX and antenna diversity switches, TX and RX baluns and a basic amount of supply decoupling. The SiP radio circuit is integrated on an organic substrate. The total WLAN system is integrated in a 10 mm $\times$ 15 mm HLLGA68 package and can be handled as a standard pick-and-place component. The device is a ‘plug-and-play’ SiP. Robust design requires no manufacturing trimming, resulting in a cost-optimized solution. The RF antenna ports have a normalized 50 Ω impedance and each can be connected directly to an external antenna with a 50 Ω transmission line.

The BGW200EG supports two host interfaces. The high-speed SPI slave (SPI2) interface is ideal for embedded applications since only 5 signal lines are required to connect to the host controller, and the protocol for this interface has a low processing overhead. The SDIO interface can operate in SPI, SD1 and SD4 modes, and can be used in an embedded application or in a secure digital NIC card. The ARM7TDMI-S RISC core, today considered as the standard RISC processor in the telecommunications industry, is integrated in the SA2443A. The processor is characterized by its extremely low mW/MIPS ratio. The BGW200EG has 1 Mbit of on-chip SRAM, thereby eliminating the need for external SRAM. This reduces the total footprint of the WLAN solution as well as the power consumption of the system. The functionality of the IEEE 802.11 MAC is split between hardware and software running on the ARM microcontroller. The IEEE 802.11b modem is implemented in hardware with control and configuration handled by software.

The BGW200EG is designed to be used as a low-cost, low-power wireless LAN link. Existing WLAN solutions, aimed at the computing market, have made use of the host processor to implement such functions as fragmentation and defragmentation. The BGW200EG implements all WLAN functions internally (implemented in either hardware or firmware) with the result that there is no processing load on the host controller. This link

will be the basis for smart phones and PDAs to communicate with a LAN network through a WLAN access point both for voice (VoIP) and data access. It is designed to handle the IEEE 802.11b specification.

The BGW200EG combines the IEEE 802.11b PHY and MAC with the embedded HCI firmware for selected host operating systems through either the SPI or SDIO interfaces. A typical example of the BGW200EG in its environment is illustrated in Figure 3. Together with an antenna, reference clock and filtering as required by the application, this device forms a complete WLAN solution. The system architecture is ideal for mobile products and requires no load on the host processor. The host sleeps while the WLAN listens for the beacon and is woken by the WLAN when appropriate.



(1) Host is typically a mobile device such as a cell phone or PDA.

(2) Serial EEPROM/flash is optional.

Fig 3. Typical application of the BGW200EG

7.2 Subblock overview

Table 3 gives an overview of some subblocks shown in Figure 1 and provides a reference to the section of the data sheet that describes these blocks.

Table 3. Subblock overview

Block name	Description	Reference
SA2405 RF transceiver		
FIRDAC	finite impulse response digital-to-analog converter	Section 8
AGC state machine	automatic gain control state machine	
RSSI	receive signal strength indicator	
SA2411 RF power amplifier		
PA	power amplifier	Section 9
SA2443A Baseband/MAC		
SCU	system configuration unit	Section 10.1
Processor:		
ARM7TDMI-S	fast RISC processor controlling other blocks via AHB and VPB buses	Section 10.2
IPU	instruction pre-fetch unit	
JTAG	joint test action group interface for ARM7 emulation	
SRAM	system RAM for use by firmware	
ROM	read only program memory	

Table 3. Subblock overview *…continued*

Block name	Description	Reference
MAC:		
HW MAC	hardware medium access control layer	Section 10.3
PHYTX	physical layer transmitter	Section 10.7
PHYRX	physical layer receiver	Section 10.8
WEP	WEP encryption and decryption engine	Section 10.4
AES (CCM)	CCM encryption and decryption engine	Section 10.5
DMA	general-purpose DMA engine	Section 10.6
RFIF	RF interface	Section 10.9
TIMERS	system timers	Section 10.10
ICU	interrupt control unit	Section 10.11
UART	universal asynchronous receiver/transmitter interface	Section 10.12
SPI:		
SPI1	master/slave serial peripheral interface	Section 10.13
SPI2	high-speed slave serial peripheral interface	Section 10.14
SDIO	secure digital input/output interface	Section 10.15
GPIO	general-purpose input/output pin(s)	Section 10.16

8. SA2405 RF transceiver

The SA2405 RF transceiver is targeted for operation in the 2.45 GHz band, specifically for IEEE 802.11b 1 Mbit/s and 2 Mbit/s DSSS, and 5.5 Mbit/s and 11 Mbit/s CCK high rate standards.

The RF VCO is common to both the transmitter and the receiver. The RF VCO is a differential 4.8 GHz Local Oscillator (LO) with the frequency determining components internal to the IC. The VCO is connected internally to a frequency divider and a quadrature generator circuit which produces the local oscillator frequencies for the I and Q up mixers and down mixers. The divider output is also internally connected to the synthesizer which can be programmed in order to produce the desired LO frequency. The frequency step size of the synthesizer is 0.5 MHz.

The RF LNA has two stepped gains controlled internally by the on-chip AGC control loop. The RF signal is downconverted to baseband by the quadrature mixers. The I and Q low-pass filters are fully integrated active Type I Chebychev filters. The I/Q pass band extends from DC to a −3 dB corner at 7 MHz. Three stepped gains are incorporated in the channel filters. Additional adjustable gain is provided in baseband amplifiers to achieve a totally adjustable gain range of 90 dB. The RX output to the baseband are differential I and Q signals.

The RX chain also integrates a high-pass filter (DC notch) for cancellation of the DC offset inherent to zero-IF architecture. The high-pass filter has a programmable lower 3 dB cut-off frequency of 10 MHz, 1 MHz, 100 kHz or 10 kHz. The DC offset cancellation occurs simultaneously with the on-chip AGC loop settling process. During the AGC settling phase, the high-pass cut-off frequency is dynamically selected between 10 MHz and 1 MHz to quickly reduce DC offset values from +50 dBc to below −20 dBc relative to a −76 dBm input signal at the antenna.

After the AGC settling (may be more than one AGC cycle with antenna diversity), the high-pass is configured to 100 kHz for 5 μs before switching to a final 10 kHz cut-off frequency. The low value of 10 kHz is required for minimizing the signal distortion created by a high-pass function at zero frequency. The high-pass will then remain set to the 10 kHz cut-off frequency until a new AGC cycle for the next receive data burst is started. Whenever there is a frequency change in the high-pass filter lower cut-off, the DC offset can change from a very low value to approximately 50 % (1 MHz ≥ 100 kHz step) or 10 % (100 kHz ≥ 10 kHz step) of the signal level. This DC offset then decays according to the high-pass response of the filter.

The receiver contains a fully integrated automatic gain control loop. It works by adjusting the internal gain such that the RX output amplitude meets a predefined target value. A measured RSSI is used to realize the gain adjustment. By default, the AGC is always set to a default maximum gain (adjustable by register value GMAX) whenever the BGW200EG enters the receive mode of operation from another operational mode. The receiver takes 5 μs to settle after entering the receive mode, which includes the time for DC offsets to be removed with a 1 MHz lower cut-off frequency of the high-pass filtering. This lower cut-off frequency of 1 MHz remains unchanged as long as the AGC remains in the default maximum gain state. By successively reducing the gain from its initial maximum value, the AGC loop searches for the correct gain value to provide a nominal RX output amplitude to the baseband. This is achieved after a maximum of 8 μs with the default wait periods. This settling time is determined by wait periods necessary to settle the receiver after gain switching actions. The individual wait periods can be adjusted by means of register settings.

The Receive Signal Strength Indicator (RSSI) is implemented as an error signal derived from comparing the signal level at the RX output to a nominal value. The RSSI acts on the modulated RF signal envelope that is extracted from the baseband I and Q signals, and reflects on a logarithmic scale the amplitude of the instantaneous modulated RF signal envelope. The RSSI signal is filtered by a 3rd-order Bessel low-pass filter with 0.5 MHz cut-off frequency. The RSSI signal will include DC offsets and will, therefore, show transient decaying errors when the DC cancellation corner frequency is changed.

The receiver is designed to exceed the 802.11 specifications for the blocking and intermodulation. It can accept continuous or randomly pulsed interference single signals or multitone signals that are more than 35 dB stronger than the required signal and up to −10 dBm of interference level. The spurious I and Q outputs are maintained to less than −20 dBc of the required signal level.

The transmitter input binary data streams are sampled with a 44 MHz reference clock and integrated FIRDACs provide additional pulse shaping filtering. The wideband I/Q up converter includes reconstruction filters (4th order low-pass Butterworth with 9.75 MHz 3 dB upper cut-off frequency). At 18 dBm maximum transmitter output level, the out-of-band (FCC forbidden band) spurious signal power is less than −77 dBc (integrated over 1 MHz with a 100 kHz resolution bandwidth) for the 11 Msymbol/s CCK modulation.

By using the on-chip calibration loop the transmitter carrier leakage can be reduced to levels far less than required by the standard. An RF power meter detects the LO level, converts it into a digital signal and a state machine determines the compensation values which are fed through an on-chip DAC directly to the I/Q inputs. The I/Q gain and phase imbalance, the InterSymbol Interference (ISI) of the reconstruction filter and in-channel noise produce a typical modulation EVM of less than 8 % (RMS) for 11 Msymbol/s CCK modulation.

Upon entering the TX mode, the ramping-up of the RF TX signal is delayed by an internal power ramping circuit. The ramping-up time is fixed while the delay prior to ramping-up can be programmed by register settings. There is 15 dB of gain control with 1 dB resolution. A gain adjustment range of 0 dB to 7 dB in 1 dB steps is provided in the TX reconstruction filter. An additional 8 dB of gain control is provided in the upconverters via a single 8 dB gain step.

9. SA2411 RF power amplifier

The power stage of the transmit amplifier is a fixed gain, class AB amplifier designed to give typically 18 dBm output power at the antenna pin for an 11 Msymbol/s CCK modulation. The device has differential inputs and an integrated balun and harmonic filter at the output. The integrated power detector detects the power level and transforms it into a low-frequency voltage input for the baseband.

10. SA2443A IEEE 802.11b medium access controller and modem

10.1 System configuration unit

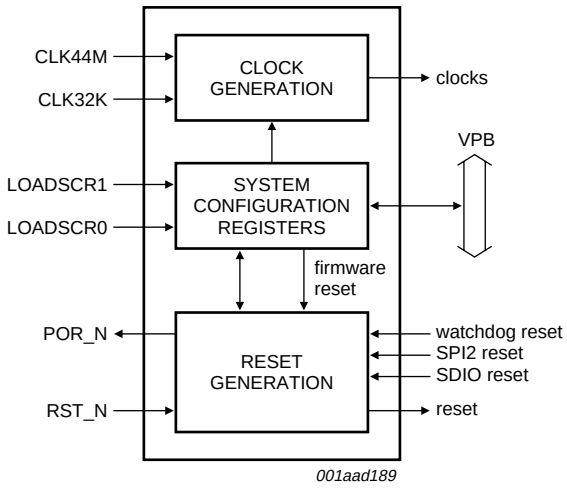


Fig 4. Block diagram of the system configuration unit

The 44 MHz reference clock for the SA2443A is supplied by the SA2405.

Power consumption is substantially reduced in doze mode using a low-frequency sleep clock. The sleep clock can be derived from an internal 1 MHz oscillator, located in the clock generation block, or supplied externally (typically 32 kHz).

The clock generation block generates all clocks required by the SA2443A from the 44 MHz, 1 MHz and 32 kHz clocks. The microcontroller and bus clock frequency can be configured between 32 kHz and 66 MHz to allow power consumption to be optimized.

The SA2443A has five reset sources:

- External reset (pin RST_N)
- Watchdog timer reset
- Firmware reset
- SPI2 reset
- SDIO reset

A power-on reset signal is generated when the core supply voltage is applied. The reset signal remains active for 4 ms after the 1.8 V supply is stable. The signal is available on pin POR_N. The RST_N pin should be linked to the POR_N pin; use of an external reset signal is not supported.

The MODE0 and MODE1 pins are used to control the boot mode of the SA2443A as shown in Table 4.

Table 4. SA2443A boot modes

MODE0	MODE1	Boot mode	Description	Boot clock
L	L	SPI embedded	firmware download from the host via SPI2	44 MHz
H	L	SPI flash	firmware read from a serial flash via SPI1	
L	H	SDIO embedded	firmware download from the host via SDIO	
H	H	reserved	-	-

The SPI embedded boot mode is used when the WLAN solution is embedded in an application, such as a cellular phone or PDA. In this case, the SA2443A firmware will be downloaded from the host processor via the high-speed SPI slave interface (SPI2).

The SPI flash mode is used primarily for firmware development and debugging. In this mode, firmware is read from a serial flash memory connected to the master/slave SPI interface (SPI1).

The SDIO embedded mode operates in the same way as the SPI embedded mode, except that code is downloaded from the SDIO interface.

10.2 Microcontroller subsystem

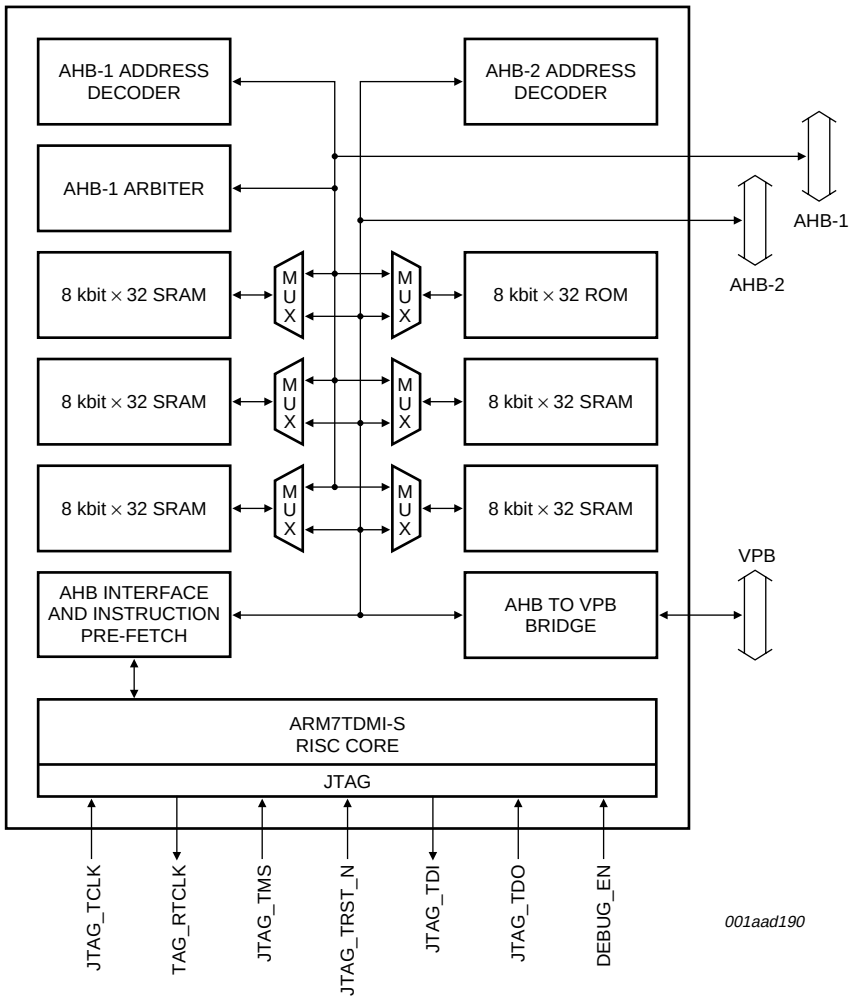


Fig 5. Block diagram of the microcontroller subsystem

The microcontroller subsystem is based around an ARM7TDMI-S RISC controller and has the following features:

- Embedded nonvolatile memory: 256-kbit ROM
- Embedded volatile memory: 5 × 256-kbit SRAM
- Instruction pre-fetch unit for enhanced microcontroller performance
- Two high-performance AHB buses for optimized throughput:
  - AHB1 is a multimaster bus used for DMA transfers
  - AHB2 is a single-master bus used by the microcontroller
- VPB bus for lower-speed peripherals
- JTAG-compliant interface for ARM7 in-circuit emulation (enabled by pulling the DEBUG_EN pin HIGH)

10.3 Hardware medium access control layer

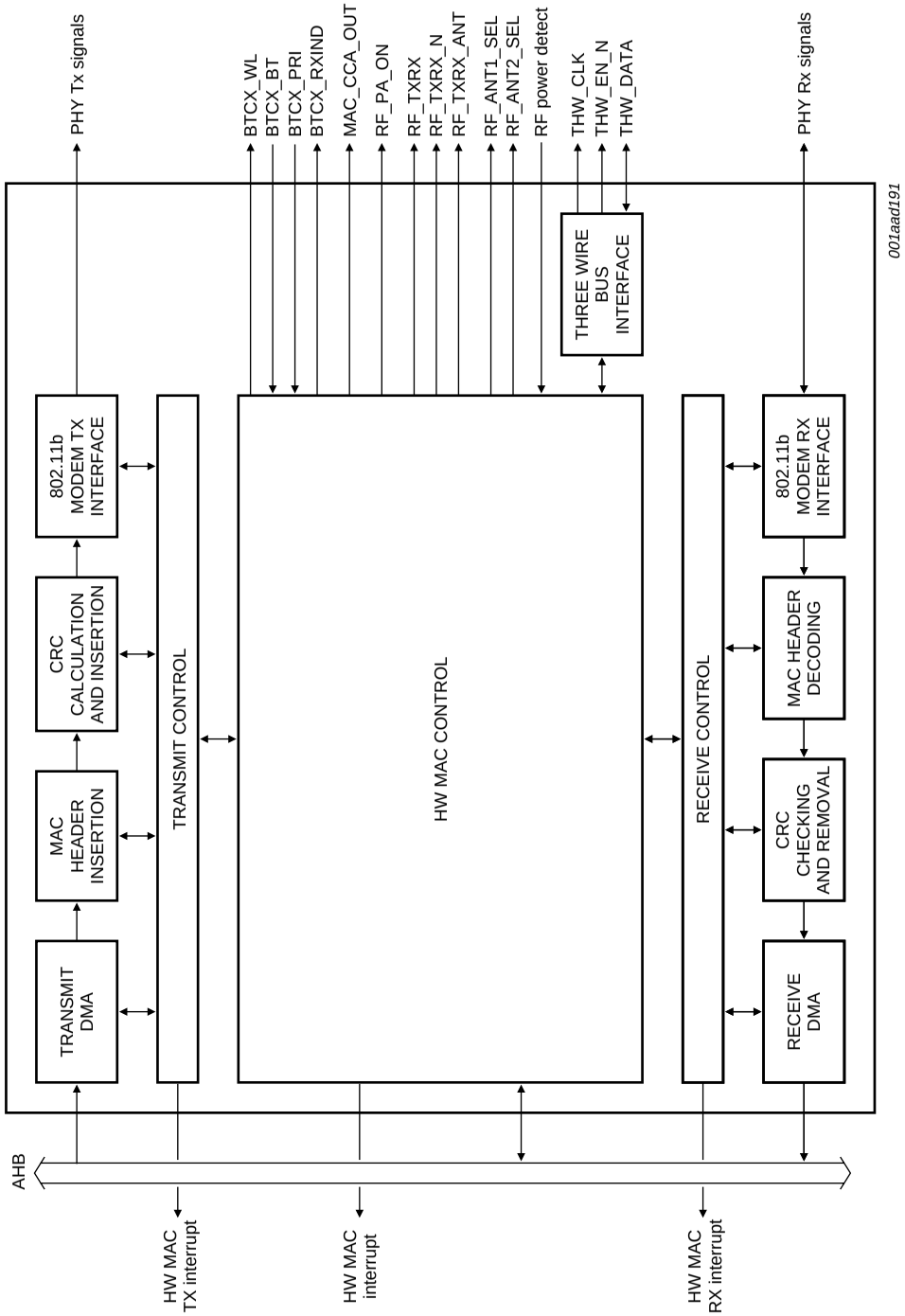


Fig 6. HW MAC block diagram

The IEEE 802.11b compliant HW MAC supports the following features:

- Data rates up to 11 Mbit/s
- SIFS timer
- Cyclic Redundancy Check (CRC) calculation and checking
- Back-off mechanism support
- Automated transmit timing control
- Automated TBTT/TXOP boundary checking
- Automated NAV timer update
- Automated IBSS mode beacon handling
- Automated TSF update from the beacon packet
- Automated insertion of TSF into the beacon packet
- Automatic wake-up for beacon reception
- Automated header field insertion (e.g. transmit address)
- QoS support:
  - 4 EDCF channels
  - 2 streams for HCF
- ATIM handler
- SW programmable automated response mechanism (e.g. ACK, RTS, CTS and QoS Null)
- Programmable unicast, multicast and beacon filtering
- Receive and transmit DMA engines for efficient data transfer
- Configurable TX/RX status interrupts
- Bluetooth coexistence Packet Traffic Arbitration (PTA) support
- Configurable antenna TX/RX and diversity switch control signals

The HW MAC block has the following external interfaces:

- SA2405 2.45 GHz transceiver control interface
- Antenna, TX/RX and diversity switch control signals
- Bluetooth coexistence interface

The HW MAC block has interfaces to the following subblocks:

- Physical layer transmitter (PHYTX); see Section 10.7
- Physical layer receiver (PHYRX); see Section 10.8
- RF interface (RFIF); see Section 10.9

10.4 WEP encryption and decryption coprocessor

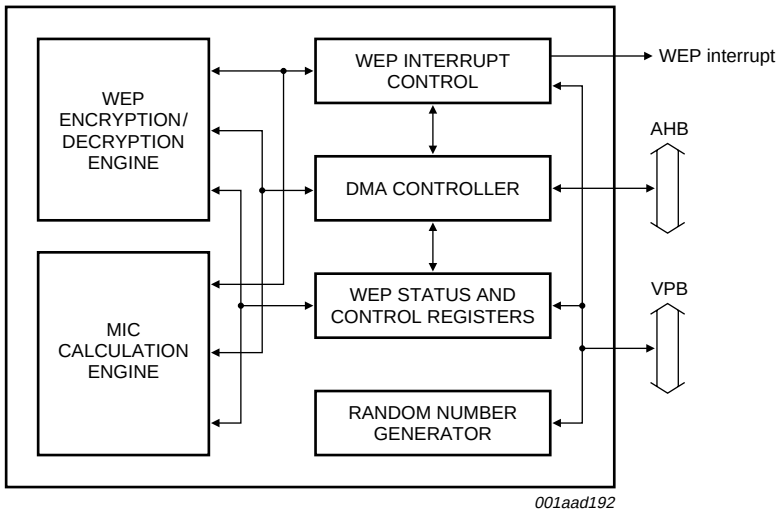


Fig 7. Block diagram of the WEP encryption and decryption coprocessor

The WEP encryption and decryption coprocessor has the following features:

- WEP 64-bit and 128-bit encryption and decryption
- WEP2 support in conjunction with firmware running on the microcontroller
- MIC calculation to facilitate TKIP support in conjunction with firmware running on the microcontroller
- DMA controller for high data throughput with minimum processing load on the microcontroller
- Random number generator to assist in the generation of encryption keys

10.5 CCM encryption and decryption coprocessor

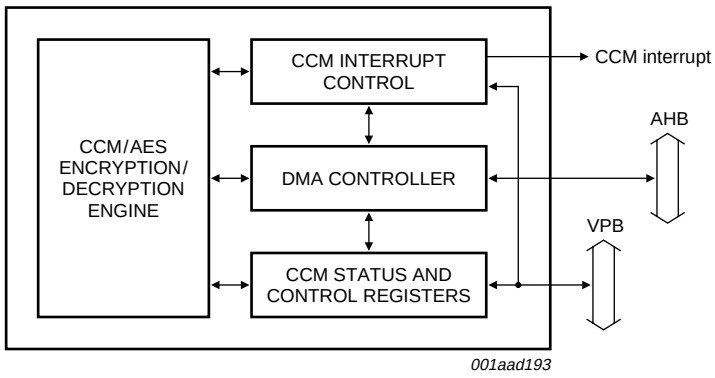


Fig 8. Block diagram of the CCM encryption and decryption coprocessor

The CCM encryption and decryption coprocessor supports both the CCM (counter mode with CBC-MAC) and the AES security algorithms. A DMA engine is incorporated to allow high data throughput with minimum loading on the microcontroller.

10.6 General-purpose DMA engine

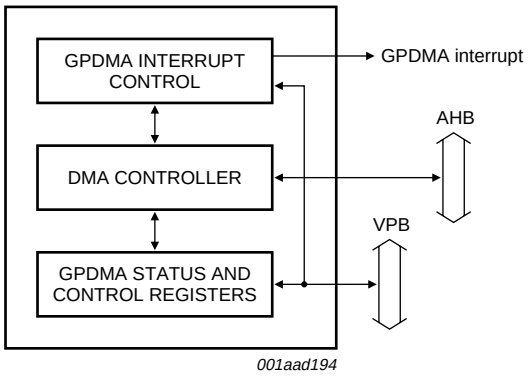


Fig 9. Block diagram of the general-purpose DMA engine

The general-purpose DMA engine can be used to move data from one memory location to another with minimum firmware involvement. Uses of the block include fragmentation and defragmentation assistance.

10.7 Physical layer transmitter

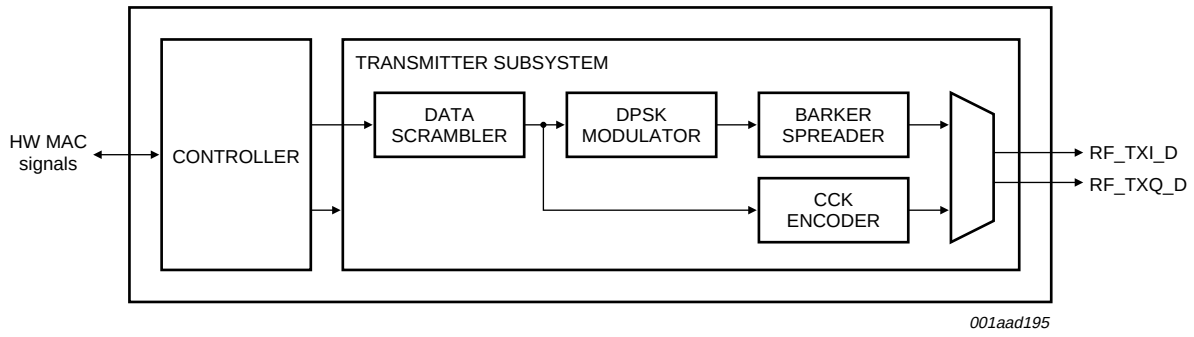


Fig 10. Block diagram of the physical layer transmitter

The PHYTX block is IEEE 802.11b compliant and supports the following features:

- 1 Mbit/s, 2 Mbit/s, 5.5 Mbit/s and 11 Mbit/s data rates
- Short and long preambles

The PHYTX block is tightly coupled to the SA2443A HW MAC block; see Section 10.3. Control and configuration of the PHYTX block are performed by the HW MAC block and firmware.

The PHYTX block comprises the controller and the transmitter subsystem.

The controller is responsible for interfacing with the HW MAC unit, generation of the PLCP header and control of the transmitter subsystem. The controller passes a serial bit stream into the transmitter subsystem. The transmitter subsystem generates modulated I and Q signals compatible with the serial digital transmit interface on the SA2405 transceiver.

The test modes available with the PHYTX block and their uses are given in Table 5.

Table 5. PHYTX test modes

Test mode	Description	Measurement uses
RANDOM	continuous modulated random data	EVM, spectral mask
0101	continuous 0101 sequence	carrier suppression
CW	unmodulated I/Q data	transmit frequency offset

10.8 Physical layer receiver

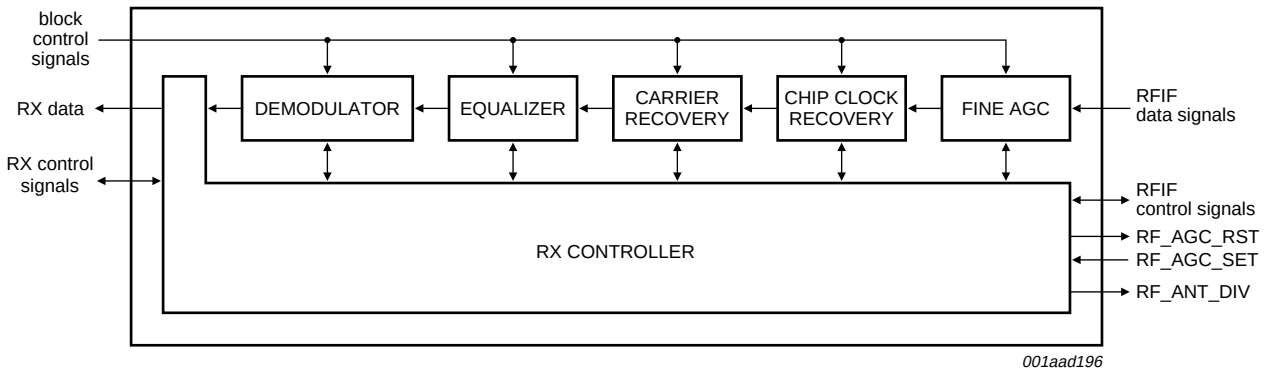


Fig 11. Block diagram of the physical layer receiver

The PHYRX block is IEEE 802.11b compliant and supports the following features:

- 1 Mbit/s, 2 Mbit/s, 5.5 Mbit/s and 11 Mbit/s data rates
- Short and long preambles
- Decision feedback equalizer with > 200 ns RMS multipath delay spread tolerance
- Antenna diversity

The PHYRX block is tightly coupled to the SA2443A HW MAC block; see Section 10.3. Control and configuration of the PHYRX block is performed by the HW MAC block and firmware. The PHYRX also interfaces to the RF interface block; see Section 10.9.

The RX controller contains the state machine that switches the modes of the RX blocks and performs the following functions:

- Clear Channel Assessment (CCA)
- Bit synchronization
- Antenna diversity

The fine AGC block adjusts the received signal level for optimum receiver performance. Sampling clock correction and carrier frequency correction are handled by the chip clock recovery and carrier recovery blocks respectively. Correction for multipath distortion is performed by a fractionally spaced decision feedback equalizer.

The operation performed by the demodulator is dependent on the data rate. For 1 Mbit/s or 2 Mbit/s rates the demodulator will differentially decode the output of a Barker de-spreader. For 5.5 Mbit/s or 11 Mbit/s data rates a CCK decoder is used to translate the output of the equalizer into data bits. In both cases, a descrambler removes the pseudorandom sequence from the data.

10.9 RF interface

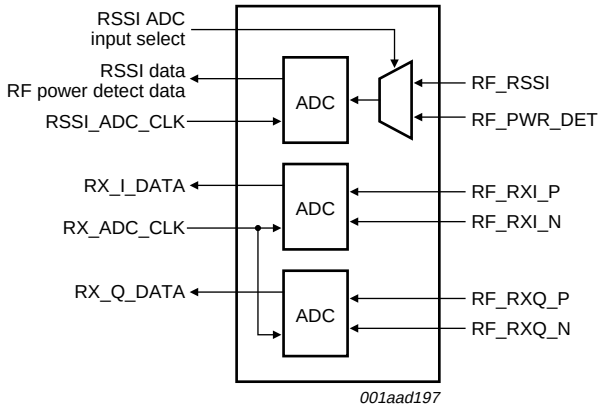


Fig 12. Block diagram of the RF interface

The RF interface has the following features:

- RSSI and power detect input:
  - 8-bit ADC
  - Multiplexed ADC input
- Analog receive inputs:
  - Differential inputs
  - 8-bit ADC

Digitized received I/Q signals are routed, together with RSSI values, to the physical layer receiver; see Section 10.8. Power detector samples are routed to the HW MAC; see Section 10.3.

10.10 System timers

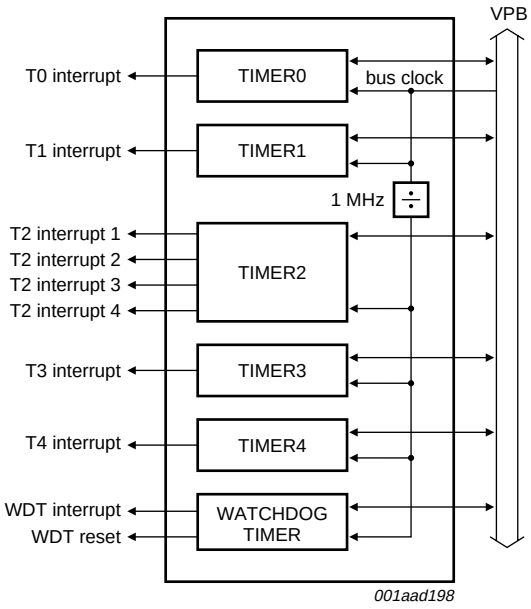


Fig 13. Block diagram of system timers

The SA2443A contains five general-purpose timers and a WatchDog Timer (WDT). Table 6 provides an overview of the timer functionality.

Table 6. Timer overview

Timer name	Type	Count frequency	Interrupt conditions
TIMER0	down count	bus clock	on zero
TIMER1	down count	bus clock	on zero
TIMER2	up count	1 MHz	when count matches any of four programmed values
TIMER3	down count	1 MHz	on zero
TIMER4	down count	1 MHz	on zero
WDT	down count	1 MHz	interrupt when count matches programmed value; reset generated when count reaches zero

Timers 0, 1, 3 and 4 can be programmed with a start value. Operation can be either single shot or continuous. An interrupt is generated when a timer counts down to zero.

Timer 2 is programmed with up to four interrupt compare values. An interrupt is generated when the counter value matches one of the interrupt compare values. Operation can be either one shot or continuous.

The watchdog timer provides a mechanism to reset the SA2443A if for some reason the firmware becomes locked. A start value is programmed from which the counter counts down to zero. For correct operation of the SA2443A the firmware must reset the start value before the counter reaches zero. If the counter reaches zero the SA2443A is reset. An interrupt compare value can be programmed, allowing a warning to be generated prior to the full reset.

10.11 Interrupt control unit

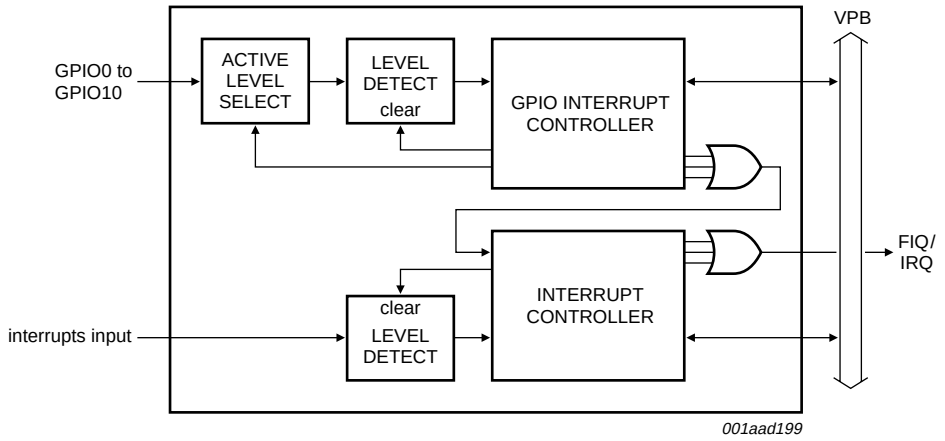


Fig 14. Block diagram of the IRQ/FIQ interrupt controller

Two primary interrupt controllers are implemented:

- Fast Interrupt reQuest (FIQ) interrupt controller
- Interrupt ReQuest (IRQ) interrupt controller

For each of the primary interrupt controllers there is a secondary GPIO interrupt controller.

The FIQ interrupt controller provides fast, low-latency interrupt handling, whereas the IRQ interrupt controller is used for general interrupts.

For each interrupt controller it is possible to enable or disable individual interrupts, read the status of the interrupts and observe the interrupt input status.

The FIQ and IRQ interrupt controllers also provide a vector register that contains an instruction address that the firmware interrupt handler can jump to. A different address will be reported for each interrupt. In the case of simultaneous interrupts, the vector address will be for the highest priority interrupt. Interrupt 0 is the highest priority and interrupt 31 is the lowest priority.

All interrupts are level sensitive and for GPIO interrupts the active level can be configured by firmware.

10.12 Universal asynchronous receiver transmitter

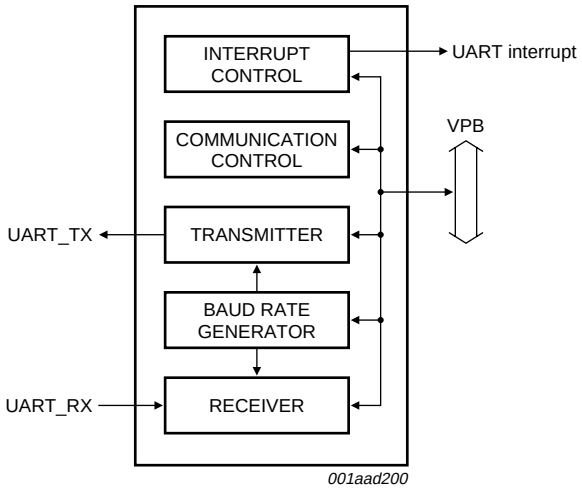


Fig 15. Block diagram of the UART interface

The Universal Asynchronous Receiver Transmitter (UART) supports the following features:

- Parity generation and detection: even, odd, fixed logic 1 or logic 0 or no parity
- Stop bit generation: 1, 1.5 (5-bit character size only) or 2 stop bits
- Character sizes: 5-bit, 6-bit, 7-bit or 8-bit
- Programmable standard baud rates up to 4.125 Mbit/s
- Automatic line error checking: stop bit failure (framing), RX overrun, parity error
- Compatible with the industry standard 16450 UART

The UART provides an asynchronous interface that includes interrupt handling and a baud rate generator allowing 16 times oversampling. The interface supports character formats from 5-bit to 8-bit length with an optional parity bit and 1, 1.5 or 2 stop bits. All standard bit rates are supported.

10.13 Master/slave serial peripheral interface

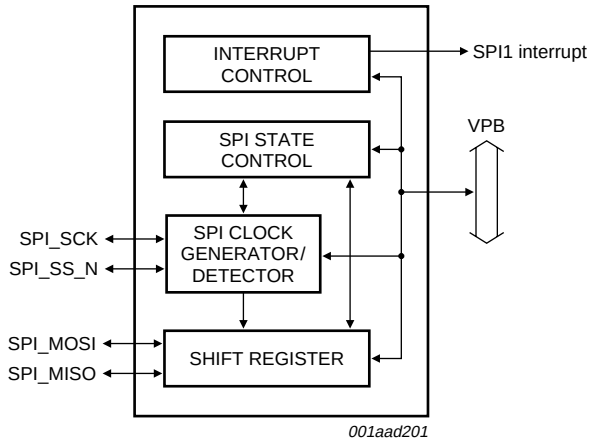


Fig 16. Block diagram of the master/slave SPI interface (SPI1)

The master/slave SPI interface (SPI1) has the following features:

- Master or slave mode operation
- SPI mode 0 and mode 3 supported in both master and slave modes
- Programmable clock frequency up to 8.25 MHz
- Automatic error checking: write collision, read overrun, mode fault and slave abort

The SPI1 interface block can be configured to work with most SPI master or slave devices. Clock frequency, polarity (bit CPOL) and phase (bit CPHA) are configurable by firmware, as is the data bit order (LSB first or MSB first).

The primary use of the interface is as an SPI master connected to a serial EEPROM or flash memory. In this case, one of the GPIO pins (see Section 10.16) must be controlled by firmware to generate the EEPROM slave select signal. When used in master mode pin SPI_SS_N must be held HIGH to prevent a mode fault occurring.

The SPI clock is oversampled by a factor of 8. The maximum SPI1 clock frequency is therefore limited to 1/8 of the bus clock.

The I/O pins for this interface are multiplexed with the I/O pins for the SPI2 block; see Section 10.14.

10.14 High-speed slave serial peripheral interface

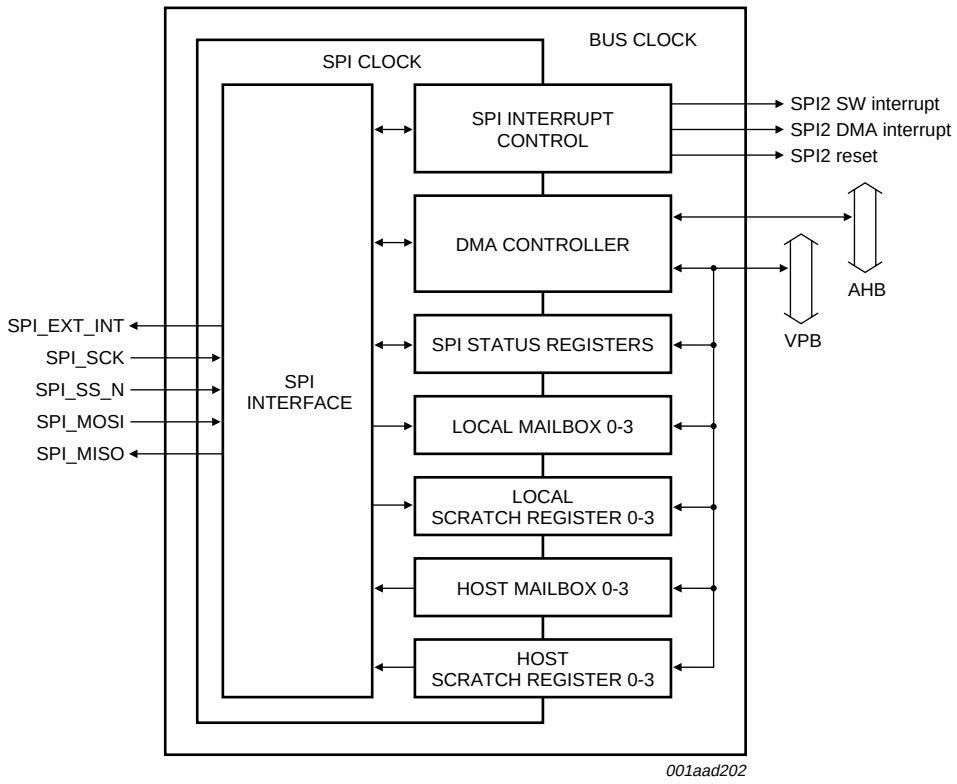


Fig 17. Block diagram of the high-speed SPI slave interface (SPI2)

The high-speed SPI slave interface (SPI2) has the following features:

- SPI mode 3 slave interface
- Up to 66 Mbit/s data transfer rate (when SPI_MOSI is clocked from the positive edge of SPI_SCK)
- 8-bit minimum packet length
- Half-duplex operation
- DMA controller
- 8 mailboxes (4 local and 4 host)
- 8 scratch registers (4 local and 4 host)
- Low-overhead link protocol
- External signal for interrupting SPI master
- SPI host can reset the SA2443A

The SPI2 interface of the SA2443A is a high-speed SPI slave interface intended for high-throughput host communication.

The I/O pins for this interface are multiplexed with the I/O pins for the SPI1 block; see Section 10.13.

10.14.1 SPI interface

The SPI interface operates entirely in the SPI clock domain. This enables the use of a higher SPI clock frequency than would be allowed with the usual oversampling scheme. SPI2 clock frequencies of up to 66 MHz are allowed.

The SPI_SCK for SPI2 only needs to run when a data transfer is in progress. No additional clock pulses are needed.

When the SA2443A is the only slave on the SPI bus the SPI_SS_N signal can be tied permanently LOW, without any impact on power consumption.

The SPI interface supports mode 3 slave operation. The relationship between SPI_SCK, SPI_MOSI and SPI_MISO is illustrated in Figure 18. Data on SPI_MOSI is sampled on the rising edge of SPI_SCK. The SA2443A can be programmed (by firmware running on the SA2443A microcontroller) to transition SPI_MISO on either the falling edge or rising edge of SPI_SCK.

Care should be taken that none of the SPI interface signals are driven HIGH when V_{DDA} is lower than the minimum recommended operating voltage; see Table 66.

The write register command and all initialization packets are always sent MSB first. The bit order of the read register data, DMA size and DMA data packets can be programmed (by firmware running on the SA2443A microcontroller) to allow either the LSB or the MSB in a packet to be transferred first.

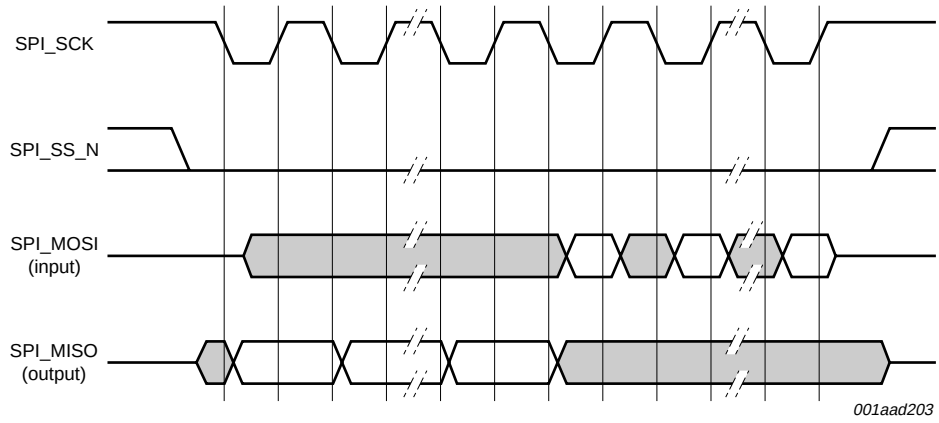


Fig 18. SPI2 timing diagram

10.14.2 Mailboxes and scratch registers

The SPI2 interface contains 8 mailboxes: 4 local mailboxes (SPI2_LOC_MB0 to SPI2_LOC_MB3; see Table 20) and 4 host mailboxes (SPI2_HST_MB0 to SPI2_HST_MB3; see Table 22).

The local mailboxes are written to by the host and read from by the SA2443A microcontroller. A local SPI2 interrupt is generated when the host writes to one of the local mailboxes. The enabling of generation of the interrupt is programmable.

The host mailboxes are written to by the SA2443A microcontroller and read from by the host. A host interrupt is signaled on the SPI_EXT_INT pin when the microcontroller writes to one of the host mailboxes.

Eight scratch registers are provided: 4 local registers (SPI2_LOC_SR0 to SPI2_LOC_SR3; see Table 21) and 4 host registers (SPI2_HST_SR0 to SPI2_HST_SR3; see Table 23). The scratch registers are accessed in the same way as the mailbox registers, the only difference being that no interrupts are generated when the scratch registers are written.

10.14.3 DMA controller

The DMA controller provides efficient transfer of data between the host and SA2443A internal memory. The host initiates all DMA transfers.

The DMA controller supports data transfers from 0 bytes to 65535 bytes.

10.14.4 Host SPI operations

The host can read or write registers in the SPI2 interface and initiate DMA transfers.

10.14.4.1 Write register command

The write register command is used by the host to write data into SPI interface registers. It consists of one 16-bit packet. The command format is shown in Table 7.

Table 7. Write register command packet

Bit	Symbol	Value	Description
15	COMMAND_TYPE	1h	indicates a host-to-slave transfer
14 to 10	REG_ADDR[4:0]	00h to 1Ah	see Table 16 for valid register addresses
9 and 8	-	-	reserved
7 to 0	REG_DATA[7:0]	00h to FFh	register data

10.14.4.2 Read register command

The read register command sequence is used by the host to read data from SPI interface registers and consists of two packets:

- Read register initialization packet (16-bit, host-to-slave). The format of this packet is shown in Table 8.
- Read data package (16-bit, slave-to-host). The format of this packet is shown in Table 9.

Table 8. Read register command initialization packet

Bit	Symbol	Value	Description
15	COMMAND_TYPE	0h	indicates a slave-to-host transfer
14 to 10	REG_ADDR[4:0]	00h to 1Ah	see Table 16 for valid register addresses
9 to 0	-	-	reserved

Table 9. Read register command data packet

Bit	Symbol	Value	Description
15 to 8	-	-	reserved
7 to 0	REG_DATA[7:0]	00h to FFh	register data

10.14.4.3 Host-to-slave DMA transfer

The host-to-slave DMA command sequence is used to transfer data from the host into internal memory in the SA2443A and consists of the following packets:

- DMA initialization packet (16-bit, host-to-slave); see Table 10.
- DMA length packet (16-bit, host-to-slave); see Table 11.
- DMA data packets (8-bit, host-to-slave); see Table 12.

Table 10. Host-to-slave DMA initialization packet

Bit	Symbol	Value	Description
15	COMMAND_TYPE	1h	indicates a host-to-slave transfer
14 to 10	INIT_CODE[4:0]	03h	host-to-slave DMA initialization
9 to 0	-	-	reserved

Table 11. Host-to-slave DMA length packet

Bit	Symbol	Value	Description
15 to 0	DATA_LEN[15:0]	0000h to FFFFh	number of bytes to be transferred

Table 12. Host-to-slave DMA data packet

Bit	Symbol	Value	Description
7 to 0	DATA[7:0]	00h to FFh	DMA data

10.14.4.4 Slave-to-host DMA command sequence

The slave-to-host DMA command sequence is used to transfer data from SA2443A internal memory to the host and consists of the following packets:

- DMA initialization packet (16-bit, slave-to-host); see Table 13.
- DMA length packet (16-bit, slave-to-host); see Table 14.
- DMA data packets (8-bit, slave-to-host); see Table 15.

Table 13. Slave-to-host DMA initialization packet

Bit	Symbol	Value	Description
15	COMMAND_TYPE	0h	indicates a slave-to-host transfer
14 to 10	INIT_CODE[4:0]	04h	slave-to-host DMA initialization
9 to 0	-	-	reserved

Table 14. Slave-to-host DMA length packet

Bit	Symbol	Value	Description
15 to 0	DATA_LEN[15:0]	0000h to FFFFh	number of bytes to be transferred

Table 15. Slave-to-host DMA data packet

Bit	Symbol	Value	Description
7 to 0	DATA[7:0]	00h to FFh	DMA data

10.14.5 SPI2 registers

10.14.5.1 Register overview

Table 16. SPI2 registers

Register	Address	Access		Description	Reference
		Local	Host		
SPI2_LOC_ISCR	00h	R/W	R	local mailbox interrupt status and control	Table 17
SPI2_HST_ISCR	01h	R	R/W	host mailbox interrupt status and control	Table 18
SPI2_DMA_SCR	02h	R/W	R	DMA status and control register	Table 19
SPI2_LOC_MB0	05h	R	R/W	local mailbox 0 (host-to-slave)	Table 20
SPI2_LOC_MB1	06h	R	R/W	local mailbox 1 (host-to-slave)	
SPI2_LOC_MB2	07h	R	R/W	local mailbox 2 (host-to-slave)	
SPI2_LOC_MB3	08h	R	R/W	local mailbox 3 (host-to-slave)	
SPI2_LOC_SR0	0Ah	R	R/W	local scratch register 0 (host-to-slave)	Table 21
SPI2_LOC_SR1	0Bh	R	R/W	local scratch register 1 (host-to-slave)	
SPI2_LOC_SR2	0Ch	R	R/W	local scratch register 2 (host-to-slave)	
SPI2_LOC_SR3	0Dh	R	R/W	local scratch register 3 (host-to-slave)	
SPI2_HST_MB0	0Fh	R/W	R	host mailbox 0 (slave-to-host)	Table 22
SPI2_HST_MB1	10h	R/W	R	host mailbox 1 (slave-to-host)	
SPI2_HST_MB2	11h	R/W	R	host mailbox 2 (slave-to-host)	
SPI2_HST_MB3	12h	R/W	R	host mailbox 3 (slave-to-host)	
SPI2_HST_SR0	14h	R/W	R	host scratch register 0 (slave-to-host)	Table 23
SPI2_HST_SR1	15h	R/W	R	host scratch register 1 (slave-to-host)	
SPI2_HST_SR2	16h	R/W	R	host scratch register 2 (slave-to-host)	
SPI2_HST_SR3	17h	R/W	R	host scratch register 3 (slave-to-host)	
SPI2_RST_CR	19h	R/W	R/W	reset control register	Table 24
SPI2_DMA_ISCR	1Ah	R/W	R	DMA interrupt status and control	Table 25

10.14.5.2 Register details

Table 17. SPI2_LOC_ISCR register - SPI2 local mailbox interrupt status and control (00h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7	LMB3_INT_EN	R/W	R		local mailbox 3 interrupt control
				0*	do not generate interrupt when mailbox is written
				1	generate interrupt when mailbox is written by the host
6	LMB2_INT_EN	R/W	R		local mailbox 2 interrupt control
				0*	do not generate interrupt when mailbox is written
				1	generate interrupt when mailbox is written by the host
5	LMB1_INT_EN	R/W	R		local mailbox 1 interrupt control
				0*	do not generate interrupt when mailbox is written
				1	generate interrupt when mailbox is written by the host

Table 17. SPI2_LOC_ISCR register - SPI2 local mailbox interrupt status and control (00h) *…continued*

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
4	LMB0_INT_EN	R/W	R		local mailbox 0 interrupt control
				0*	do not generate interrupt when mailbox is written
				1	generate interrupt when mailbox is written by the host
3	LMB3_INT_STAT	R/W[1]	R		local mailbox 3 interrupt status
				0*	no interrupt pending
				1	mailbox 3 interrupt pending
2	LMB2_INT_STAT	R/W[1]	R		local mailbox 2 interrupt status
				0*	no interrupt pending
				1	mailbox 2 interrupt pending
1	LMB1_INT_STAT	R/W[1]	R		local mailbox 1 interrupt status
				0*	no interrupt pending
				1	mailbox 1 interrupt pending
0	LMB0_INT_STAT	R/W[1]	R		local mailbox 0 interrupt status
				0*	no interrupt pending
				1	mailbox 0 interrupt pending

[1] This bit will be cleared following a local read.

Table 18. SPI2_HST_ISCR register - SPI2 host mailbox interrupt status and control (01h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7	HMB3_INT_EN	R	R/W		host mailbox 3 interrupt control
				0*	do not generate interrupt when mailbox is written
				1	generate interrupt when mailbox is written by the slave
6	HMB2_INT_EN	R	R/W		host mailbox 2 interrupt control
				0*	do not generate interrupt when mailbox is written
				1	generate interrupt when mailbox is written by the slave
5	HMB1_INT_EN	R	R/W		host mailbox 1 interrupt control
				0*	do not generate interrupt when mailbox is written
				1	generate interrupt when mailbox is written by the slave
4	HMB0_INT_EN	R	R/W		host mailbox 0 interrupt control
				0*	do not generate interrupt when mailbox is written
				1	generate interrupt when mailbox is written by the slave
3	HMB3_INT_STAT	R	R/W[1]		host mailbox 3 interrupt status
				0*	no interrupt pending
				1	mailbox 3 interrupt pending
2	HMB2_INT_STAT	R	R/W[1]		host mailbox 2 interrupt status
				0*	no interrupt pending
				1	mailbox 2 interrupt pending

Table 18. SPI2_HST_ISCR register - SPI2 host mailbox interrupt status and control (01h) *...continued*

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
1	HMB1_INT_STAT	R	R/W[1]		host mailbox 1 interrupt status
				0*	no interrupt pending
				1	mailbox 1 interrupt pending
0	HMB0_INT_STAT	R	R/W[1]		host mailbox 0 interrupt status
				0*	no interrupt pending
				1	mailbox 0 interrupt pending

[1] This bit will be cleared following a host read.

Table 19. SPI2_DMA_SCR register - SPI2 DMA status and control (02h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7	S2H_DMA1_STAT	R	R		slave-to-host DMA channel 1 status
				0*	DMA idle
				1	DMA transfer is ongoing
6	S2H_DMA0_STAT	R	R		slave-to-host DMA channel 0 status
				0*	DMA idle
				1	DMA transfer is ongoing
5	H2S_DMA1_STAT	R	R		host-to-slave DMA channel 1 status
				0*	DMA idle
				1	DMA transfer is ongoing
4	H2S_DMA0_STAT	R	R		host-to-slave DMA channel 0 status
				0*	DMA idle
				1	DMA transfer is ongoing
3	S2H_DMA_PEND1	R/W	R		slave-to-host DMA channel 1 data pending status
				0*	no data pending
				1	data pending
2	S2H_DMA_PEND0	R/W	R		slave-to-host DMA channel 0 data pending status
				0*	no data pending
				1	data pending
1	NEXT_S2H_CHAN	R/W	R		DMA channel to be used for next slave-to-host transfer
				0*	TX DMA channel 0 will be used
				1	TX DMA channel 1 will be used
0	NEXT_H2S_CHAN	R/W	R		DMA channel to be used for next host-to-slave transfer
				0*	RX DMA channel 0 will be used
				1	RX DMA channel 1 will be used

Table 20. SPI2_LOC_MBn[1] register - SPI2 local mailbox n (05h to 08h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	MBOX_DATA[7:0]	R	R/W[2]	00h*	mailbox data

[1] Register definition is the same for all local mailboxes; replace n with the mailbox number (0 to 3).

[2] Writing to this register generates an interrupt to the local microcontroller if bit LMBn_INT_EN is set in register SPI2_LOC_ISCR (see Table 17). A local read clears the interrupt.

Table 21. SPI2_LOC_SRn[1] register - SPI2 local scratch register n (0Ah to 0Dh)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	SCRCH_DATA[7:0]	R	R/W	00h*	scratch data

[1] Register definition is the same for all local scratch registers; replace n with the scratch register number (0 to 3).

Table 22. SPI2_HST_MBn[1] register - SPI2 host mailbox n (Fh to 12h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	MBOX_DATA[7:0]	R/W[2]	R	00h*	mailbox data

[1] Register definition is the same for all host mailboxes; replace n with the mailbox number (0 to 3).

[2] Writing to this register generates an interrupt to the SPI host if bit HMBn_INT_EN is set in register SPI2_HST_ISCR; see Table 18. A host read clears the interrupt.

Table 23. SPI2_HST_SRn[1] register - SPI2 host scratch register n (14h to 17h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	SCRCH_DATA[7:0]	R/W	R	00h*	scratch data

[1] Register definition is the same for all host scratch registers; replace n with the scratch register number (0 to 3).

Table 24. SPI2_RST_CR register - SPI2 reset control (19h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 3	-	R	R	00h*	reserved
2	SPI2_HOST_RST	R/W	R		SPI2 interface host side reset status
				0*	SPI2 interface host side operational
				1	SPI2 interface host side reset ongoing
1	SPI2_SLAVE_RST	R/W	R		SPI2 interface slave side reset status
				0*	SPI2 interface slave side operational
				1	SPI2 interface slave side reset ongoing

Table 24. SPI2_RST_CR register - SPI2 reset control (19h) *…continued*

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
0	RST_SA2443A	R	R/W		SA2443A reset control
				0*	do not reset SA2443A
				1	reset SA2443A[1]

[1] A host write to this bit will result in the SA2443A being reset.

Table 25. SPI2_DMA_ISCR register - SPI2 DMA interrupt status and control (1Ah)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7	H2S1_INT_EN	R/W	R		host-to-slave DMA channel 1 interrupt control
				0*	interrupt disabled
				1	interrupt will be generated on transfer completion
6	H2S0_INT_EN	R/W	R		host-to-slave DMA channel 0 interrupt control
				0*	interrupt disabled
				1	interrupt will be generated on transfer completion
5	S2H1_INT_EN	R/W	R		slave-to-host DMA channel 1 interrupt control
				0*	interrupt disabled
				1	interrupt will be generated on transfer completion
4	S2H0_INT_EN	R/W	R		slave-to-host DMA channel 0 interrupt control
				0*	interrupt disabled
				1	interrupt will be generated on transfer completion
3	H2S1_INT_STAT	R[1]	R		host-to-slave DMA channel 1 interrupt status
				0*	no interrupt pending
				1	transfer complete interrupt pending
2	H2S0_INT_STAT	R[1]	R		host-to-slave DMA channel 0 interrupt status
				0*	no interrupt pending
				1	transfer complete interrupt pending
1	S2H1_INT_STAT	R[1]	R		slave-to-host DMA channel 1 interrupt status
				0*	no interrupt pending
				1	transfer complete interrupt pending
0	S2H0_INT_STAT	R[1]	R		slave-to-host DMA channel 0 interrupt status
				0*	no interrupt pending
				1	transfer complete interrupt pending

[1] This bit will be cleared by a local read.

10.15 Secure digital interface

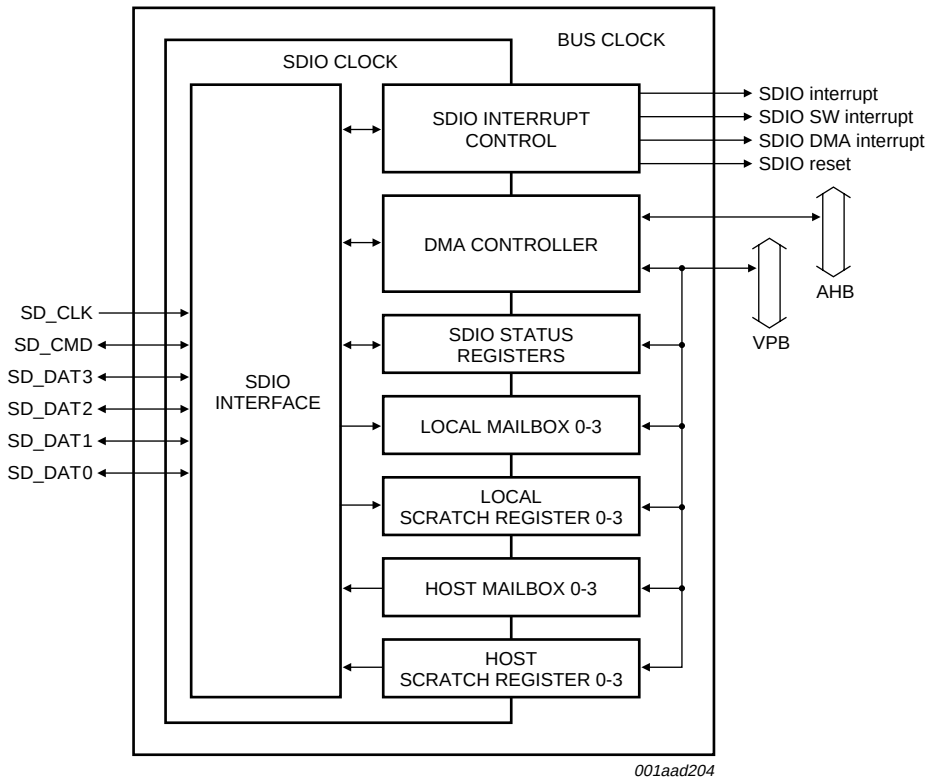


Fig 19. Block diagram of the secure digital interface

The secure digital interface has the following features:

- Compliant with version 1.00 of the SDIO standard
- Supports SPI, SD1 and SD4 modes
- SA2443A mapped to SDIO function 1
- Block sizes up to 2048 bytes supported
- DMA controller
- 8 mailboxes (4 local and 4 host)
- 8 scratch registers (4 local and 4 host)
- SDIO master can reset the SA2443A

The SDIO interface of the SA2443A is intended for high-throughput host communication. The SDIO clock is independent of the bus clock (no over-sampling) and has a maximum operating frequency of 25 MHz.

Most operations are handled by the SDIO block hardware. The role of the SA2443A firmware is to handle interrupts and to specify the location of the DMA data in SA2443A memory.

10.15.1 Mailboxes and scratch registers

The SDIO interface contains 8 mailboxes: 4 local mailboxes (SD_LOC_MB0 to SD_LOC_MB3; see Table 53) and 4 host mailboxes (SD_HST_MB0 to SD_HST_MB3; see Table 55).

The local mailboxes are written by the host and read by the SA2443A microcontroller. A local SDIO interrupt is generated when the host writes to one of the local mailboxes. The enabling of generation of the interrupt is programmable.

The host mailboxes are written by the SA2443A microcontroller and read by the host. A host interrupt is signaled when the microcontroller writes to one of the host mailboxes.

Eight scratch registers are provided: 4 local (SD_LOC_SR0 to SD_LOC_SR3; see Table 54) and 4 host (SD_HST_SR0 to SD_HST_SR3; see Table 56). The scratch registers are accessed in the same way as the mailbox registers, the only difference being, that no interrupts are generated when the scratch registers are written to.

10.15.2 DMA controller

The DMA controller provides efficient data transfer of data between the host and SA2443A internal memory. The host initiates all DMA transfers.

The DMA controller supports data transfers from 0 bytes to 65535 bytes.

10.15.3 SDIO host operations

The host can read from and write to registers in the SA2443A SDIO interface and initiate DMA transfers.

10.15.3.1 SDIO interface register access

Host-addressable registers within the SA2443A SDIO interface can be accessed with the SDIO IO_RW_DIRECT command (CMD52). In the case of a read, the register value will be returned using the IO_RW_DIRECT response (R5).

10.15.3.2 Host-to-function 1 DMA transfer

To initiate a host-to-function DMA transfer the host must first program the transfer size (in bytes) into the SD_H2F_DSIZEL and SD_H2F_DSIZEH registers (see Table 59 and Table 60) using the IO_RW_DIRECT command (two writes are required to set the 16-bit size value). The data can then be transferred using an IO_RW_EXTENDED command (CMD53) write to the SD_H2F_DDAW register; see Table 51. Note that the block mode bit of CMD53 should be set to logic 1, indicating a block mode transfer and the OP code bit should be set to logic 0, indicating a multibyte R/W to fixed address.

10.15.3.3 Function 1-to-host DMA transfer

For a function-to-host DMA transfer the host must read the transfer size (in bytes) from the SD_F2H_DSIZEL and SD_F2H_DSIZEH registers (see Table 61 and Table 62) using the IO_RW_DIRECT command (two accesses are required to read the 16-bit size value). The data can then be transferred using an IO_RW_EXTENDED command (CMD53) read from the SD_F2H_DDAW register; see Table 52. Note that the block mode bit of CMD53 should be set to logic 1, indicating a block mode transfer and the OP code bit should be set to logic 0, indicating a multibyte R/W to fixed address.

10.15.4 SDIO registers

10.15.4.1 Register overview

Table 26. SDIO registers

Registers	Address	Access		Description	Reference
		Local	Host		
Card common control registers					
SD_CCCR_REV	0 0000h	-	R	CCCR and SDIO revision register	Table 27
SD_SD_REV	0 0001h	-	R	SD specification revision register	Table 28
SD_IOE	0 0002h	-	R/W	I/O enable register	Table 29
SD_IOR	0 0003h	R/W	R	I/O ready register	Table 30
SD_IEN	0 0004h	-	R/W	interrupt enable register	Table 31
SD_INT	0 0005h	-	R	interrupt pending register	Table 32
SD_AS_RES	0 0006h	-	W	I/O abort select and reset register	Table 33
SD_BUS_CR	0 0007h	-	R/W	bus interface control register	Table 34
SD_CAPABILITY	0 0008h	R/W	R/W	card capability register	Table 35
SD_CCIS_PTR	0 0009h	R/W	R	common CIS pointer	Table 36
SD_BUS_STAT	0 000Ch	-	R/W	bus status register	Table 37
SD_FS	0 000Dh	-	R	function select register	Table 38
SD_EX	0 000Eh	-	R	execution flag register	Table 39
SD_RF	0 000Fh	-	R	ready flag register	Table 40
SD_BLK_SIZE0	0 0010h	-	R/W	function 0 block size	Table 41
Function basic registers					
SD_FIC_STD1	0 0100h	R/W	R/W	function 1 standard function interface code	Table 42
SD_FIC_EXT1	0 0101h	R/W	R	function 1 extended standard function interface code	Table 43
SD_CIS_PTR1	0 0109h	R/W	R	function 1 CIS pointer	Table 44
SD_CSA_PTR1	0 010Ch	-	R	function 1 CSA pointer	Table 45
SD_CSA_DAW1	0 010Fh	-	R/W	function 1 CSA data access window	Table 46
SD_BLK_SIZE1	0 0110h	-	R/W	function 1 I/O block size register	Table 47
Function 1 registers					
SD_LOC_ISCR	0 0100h	R/W	R	local mailbox interrupt status and control	Table 48
SD_HST_ISCR	0 0104h	R	R/W	host mailbox interrupt status and control	Table 49
SD_DMA_SCR	0 0108h	R/W	R	DMA status/control register	Table 50
SD_H2F_DDAW	0 010Ch	-	W	host-to-function DMA data access window	Table 51
SD_F2H_DDAW	0 0110h	-	R	function-to-host DMA data access window	Table 52
SD_LOC_MB0	0 0114h	R	R/W	local mailbox 0 (host-to-function)	Table 53
SD_LOC_MB1	0 0118h	R	R/W	local mailbox 1 (host-to-function)	
SD_LOC_MB2	0 011Ch	R	R/W	local mailbox 2 (host-to-function)	
SD_LOC_MB3	0 0120h	R	R/W	local mailbox 3 (host-to-function)	

Table 26. SDIO registers *...continued*

Registers	Address	Access		Description	Reference
		Local	Host		
SD_LOC_SR0	0 0128h	R	R/W	local scratch register 0 (host-to-function)	Table 54
SD_LOC_SR1	0 012Ch	R	R/W	local scratch register 1 (host-to-function)	
SD_LOC_SR2	0 0130h	R	R/W	local scratch register 2 (host-to-function)	
SD_LOC_SR3	0 0134h	R	R/W	local scratch register 3 (host-to-function)	
SD_HST_MB0	0 013Ch	R/W	R	host mailbox 0 (function-to-host)	Table 55
SD_HST_MB1	0 0140h	R/W	R	host mailbox 1 (function-to-host)	
SD_HST_MB2	0 0144h	R/W	R	host mailbox 2 (function-to-host)	
SD_HST_MB3	0 0148h	R/W	R	host mailbox 3 (function-to-host)	
SD_HST_SR0	0 0150h	R/W	R	host scratch register 0 (function-to-host)	Table 56
SD_HST_SR1	0 0154h	R/W	R	host scratch register 1 (function-to-host)	
SD_HST_SR2	0 0158h	R/W	R	host scratch register 2 (function-to-host)	
SD_HST_SR3	0 015Ch	R/W	R	host scratch register 3 (function-to-host)	
SD_RST_CR	0 0164h	R/W	R/W	reset control register	Table 57
SD_DMA_ISCR	0 0168h	R/W	R	DMA interrupt status/control	Table 58
SD_H2F_DSIZEL	0 0198h	-	R/W	host-to-function DMA data size (lower byte)	Table 59
SD_H2F_DSIZEH	0 019Ch	-	R/W	host-to-function DMA data size (upper byte)	Table 60
SD_F2H_DSIZEL	0 01A0h	-	R	function-to-host DMA data size (lower byte)	Table 61
SD_F2H_DSIZEH	0 01A4h	-	R	function-to-host DMA data size (upper byte)	Table 62
SD_F2H_DMAERR	0 01A8h	-	R/W	function-to-host DMA error	Table 63
SD_F2H_DMAOK	0 01ACh	-	R	function-to-host DMA OK	Table 64

10.15.4.2 Card common control registers

The card common control registers are located in the function 0 address space.

Table 27. SD_CCCR_REV register - SDIO CCCR and SDIO revision (FN0 0 0000h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 4	SDIO[3:0]	-	R	0*	SDIO revision supported
3 to 0	CCCR[3:0]	-	R	0*	CCCR revision supported

Table 28. SD_SD_REV register - SDIO SD specification revision (FN0 0 0001h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 4	-	-	-	-	reserved
3 to 0	SD[3:0]	-	R	0*	SD physical specification revision supported

Table 29. SD_IOE register - SDIO I/O enable (FN0 0 0002h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 2	-	-	-	-	reserved
1	IOE1	-	R/W		function 1 I/O enable
				0*	I/O disabled
				1	I/O enabled
0	-	-	-	-	reserved

Table 30. SD_IOR register - SDIO I/O ready (FN0 0 0003h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 2	-	-	-	-	reserved
1	IOR1	R/W	R		function 1 I/O ready flag
				0*	not ready for I/O operation
				1	ready for I/O operation
0	-	-	-	-	reserved

Table 31. SD_IEN register - SDIO interrupt enable (FN0 0 0004h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 2	-	-	-	-	reserved
1	IEN1	-	R/W		function 1 interrupt enable
				0*	function 1 interrupts will not be sent to host
				1	function 1 interrupts will be sent to the host. The IENM bit must also be set for the function 1 interrupt to be sent to the host.
0	IENM	-	R/W		master interrupt enable
				0*	interrupts will not be sent to the host
				1	interrupts will be sent to the host

Table 32. SD_INT register - SDIO interrupt pending (FN0 0 0005h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 2	-	-	-	-	reserved
1	INT1	-	R		function 1 interrupt pending
				0*	no interrupts from this function are pending
				1	an interrupt is pending
0	-	-	-	-	reserved

Table 33. SD_AS_RES register - SDIO I/O abort select and reset (FN0 0 0006h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 4	-	-	-	-	reserved
3	RES	-	W		card reset control
				0*	no action
				1	reset all SDIO functions. This bit will be cleared following the card reset.
2 to 0	AS[2:0]	-	W	0h*	function selected for abort

Table 34. SD_BUS_CR register - SDIO bus interface control (FN0 0 0007h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7	CD_DISABLE	-	R/W		card detect pull-up resistor control
				0*	connect pull-up resistor on SD_DAT3 pin
				1	disconnect pull-up resistor
6	SCSI	R/W	R		continuous SPI interrupt support
				0	disable
				1*	enable
5	ECSI	-	R/W		continuous SPI interrupt enable
				0*	disable
				1	enable
4 to 2	-	-	-	-	reserved
1 and 0	BUS_WIDTH[1:0]	R	R/W		data transfer bus width control
				0*	1-bit bus width
				1	reserved
				2	4-bit bus width
				3	reserved

Table 35. SD_CAPABILITY register - SDIO card capability (FN0 0 0008h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7	4BLS	R/W	R		4-bit low-speed support
				0*	low-speed card not supporting 4-bit data transfer or full-speed card
				1	low-speed card supporting 4-bit data transfer
6	LSC	R/W	R		card speed
				0*	full-speed
				1	low-speed

Table 35. SD_CAPABILITY register - SDIO card capability (FN0 0 0008h) *…continued*

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
5	E4MI	R/W	R/W		4-bit mode inter-block interrupt control
				0	do not generate interrupts during 4-bit multiblock data transfers
				1*	generate interrupts during 4-bit multiblock data transfers
4	S4MI	R/W	R		4-bit mode inter-block interrupt support
				0	card cannot generate interrupts during 4-bit multiblock data transfers
				1*	card can generate interrupts during 4-bit multiblock data transfers
3	SBS	R/W	R		suspend and resume support
				0	suspend and resume not supported
				1*	suspend and resume supported
2	SRW	R/W	R		read wait control support
				0	read wait control not supported
				1*	read wait control supported
1	SMB	R/W	R		multiblock mode support
				0	multiblock mode not supported
				1*	multiblock mode supported
0	SDC	R/W	R		direct command support
				0	direct command during data transfer not supported
				1*	direct command during data transfer supported

Table 36. SD_CCIS_PTR register - SDIO common CIS pointer (FN0 0 0009h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
23 to 0	CCIS_PTR[23:0]	R/W	R	00 1000h*	pointer to the start of the common CIS area

Table 37. SD_BUS_STAT register - SDIO bus status (FN0 0 000Ch)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 2	-	-	-	-	reserved
1	BR	-	R/W		bus release request status and control. For SPI mode this bit is read-only and will always return to logic 0.
				0*	cancel a pending suspension request
				1	suspend addressed function. Bits BR and BS will be cleared when the addressed function has executed the suspend command.

Table 37. SD_BUS_STAT register - SDIO bus status (FN0 0 000Ch) *...continued*

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
0	BS	-	R		bus status
				0	addressed function not executing data transfer. The function is selected using either the function select register (SD_FS) or by setting the function number in an I/O command. Bits BR and BS will be cleared when the addressed function has executed the suspend command.
				1*	addressed function executing data transfer

Table 38. SD_FS register - SDIO function select (FN0 0 000Dh)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7	DF	-	R		resume data flag. The function is selected using the FS[3:0] field.
				0*	no data to transfer after resume for selected function
				1	data to be transferred after resume for selected function
6 to 4	-	-	-	-	reserved
3 to 0	FS[3:0]	-	R/W	0h*	function select for suspend and resume. If the selected function is suspended when this field is written then a resume will occur.

Table 39. SD_EX register - SDIO execution flags (FN0 0 000Eh)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 2	-	-	-	-	reserved
1	EX1	-	R		function 1 execution flag
				0*	function idle
				1	function executing command
0	-	-	-	-	reserved

Table 40. SD_RF register - SDIO ready flags (FN0 0 000Fh)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 2	-	-	-	-	reserved
1	RF1	-	R		function 1 ready flag
				0*	not ready for read/write data transfer
				1	ready for read/write data transfer
0	-	-	-	-	reserved

Table 41. SD_BLK_SIZE0 - SDIO function 0 block size (FN0 0 0010h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
15 to 0	BLK_SIZE[15:0]	-	R/W	0000h*	function 0 I/O block size (1 to 2048)

10.15.4.3 Function basic registers

The function basic registers are located in the function 0 address space.

Table 42. SD_FIC_STD1 register - SDIO function 1 standard function interface code (FN0 0 0100h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7	CSA_ENBL	-	R/W		function 1 CSA enable
				0*	disable CSA access
				1	enable CSA access
6	CSA_SUP	R/W	R		function 1 CSA support
				0*	CSA not supported
				1	CSA supported and valid
5 and 4	-	-	-	-	reserved
3 to 0	FIC_STD[3:0]	R/W	R	7h*	standard SDIO function interface code

Table 43. SD_FIC_EXT1 register – SDIO function 1 extended standard function interface code (FN0 0 0101h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	FIC_EXT[7:0]	R/W	R	00h*	extended standard SDIO function interface code

Table 44. SD_CIS_PTR1 register - SDIO function 1 CIS pointer (FN0 0 0109h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
23 to 0	CIS_PTR[23:0]	R/W	R	00 2000h*	function 1 CIS pointer

Table 45. SD_CSA_PTR1 register - SDIO function 1 CSA pointer (FN0 0 010Ch)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
23 to 0	CSA_PTR[23:0]	-	R	00 0000h*	function 1 CSA pointer. The value of CSA_PTR will be incremented following each access to the SD_CSA_DAW1 register.

Table 46. SD_CSA_DAW1 register - SDIO function 1 CSA data access window (FN0 0 010Fh)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	CSA_DAW[7:0]	-	R/W	00h*	function 1 CSA data access window

Table 47. SD_BLK_SIZE1 register - SDIO function 1 I/O block size (FN0 0 0110h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
31 to 16	-	-	-	-	reserved
15 to 0	BLK_SIZE[15:0]	-	R/W	0000h*	function 1 I/O block size (0 to 2048)

10.15.4.4 Function 1 registers

Function 1 registers are located in the function 1 address space.

Table 48. SD_LOC_ISCR register - SDIO local mailbox interrupt status and control (FN1 0 0100h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7	LMB3_INT_EN	R/W	R		local mailbox 3 interrupt control
				0*	disable interrupt
				1	generate interrupt when mailbox is written by the host
6	LMB2_INT_EN	R/W	R		local mailbox 2 interrupt control
				0*	disable interrupt
				1	generate interrupt when mailbox is written by the host
5	LMB1_INT_EN	R/W	R		local mailbox 1 interrupt control
				0*	disable interrupt
				1	generate interrupt when mailbox is written by the host
4	LMB0_INT_EN	R/W	R		local mailbox 0 interrupt control
				0*	disable interrupt
				1	generate interrupt when mailbox is written by the host
3	LMB3_INT_STAT	R/W[1]	R		local mailbox 3 interrupt status
				0*	no interrupt pending
				1	mailbox 3 interrupt pending
2	LMB2_INT_STAT	R/W[1]	R		local mailbox 2 interrupt status
				0*	no interrupt pending
				1	mailbox 2 interrupt pending
1	LMB1_INT_STAT	R/W[1]	R		local mailbox 1 interrupt status
				0*	no interrupt pending
				1	mailbox 1 interrupt pending
0	LMB0_INT_STAT	R/W[1]	R		local mailbox 0 interrupt status
				0*	no interrupt pending
				1	mailbox 0 interrupt pending

[1] This bit will be cleared following a local read.

Table 49. SD_HST_ISCR register - SDIO host mailbox interrupt status and control (FN1 0 0104h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7	HMB3_INT_EN	R	R/W		host mailbox 3 interrupt control
				0*	disable interrupt
				1	generate interrupt when mailbox is written by the card
6	HMB2_INT_EN	R	R/W		host mailbox 2 interrupt control
				0*	disable interrupt
				1	generate interrupt when mailbox is written by the card
5	HMB1_INT_EN	R	R/W		host mailbox 1 interrupt control
				0*	disable interrupt
				1	generate interrupt when mailbox is written by the card
4	HMB0_INT_EN	R	R/W		host mailbox 0 interrupt control
				0*	disable interrupt
				1	generate interrupt when mailbox is written by the card
3	HMB3_INT_STAT	R	R/W[1]		host mailbox 3 interrupt status
				0*	no interrupt pending
				1	mailbox 3 interrupt pending
2	HMB2_INT_STAT	R	R/W[1]		host mailbox 2 interrupt status
				0*	no interrupt pending
				1	mailbox 2 interrupt pending
1	HMB1_INT_STAT	R	R/W[1]		host mailbox 1 interrupt status
				0*	no interrupt pending
				1	mailbox 1 interrupt pending
0	HMB0_INT_STAT	R	R/W[1]		host mailbox 0 interrupt status
				0*	no interrupt pending
				1	mailbox 0 interrupt pending

[1] This bit will be cleared following a host read.

Table 50. SD_DMA_SCR register - SDIO DMA status and control (FN1 0 0108h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7	F2H_DMA1_STAT	R	R		function-to-host DMA channel 1 status
				0*	DMA idle
				1	DMA transfer is ongoing
6	F2H_DMA0_STAT	R	R		function-to-host DMA channel 0 status
				0*	DMA idle
				1	DMA transfer is ongoing
5	H2F_DMA1_STAT	R	R		host-to-function DMA channel 1 status
				0*	DMA idle
				1	DMA transfer is ongoing

Table 50. SD_DMA_SCR register - SDIO DMA status and control (FN1 0 0108h) *…continued*

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
4	H2F_DMA0_STAT	R	R		host-to-function DMA channel 0 status
				0*	DMA idle
				1	DMA transfer is ongoing
3	F2H_DMA_PEND1	R/W	R		function-to-host DMA channel 1 data pending status
				0*	no data pending
				1	data pending
2	F2H_DMA_PEND0	R/W	R		function-to-host DMA channel 0 data pending status
				0*	no data pending
				1	data pending
1	NEXT_F2H_CHAN	R/W	R		DMA channel for next function-to-host transfer
				0*	TX DMA channel 0 will be used
				1	TX DMA channel 1 will be used
0	NEXT_H2F_CHAN	R/W	R		DMA channel for next host-to-function transfer
				0*	RX DMA channel 0 will be used
				1	RX DMA channel 1 will be used

Table 51. SD_H2F_DDAW register - SDIO host-to-function DMA data access window (FN1 0 010Ch)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	DMA_DAW[7:0]	-	W	00h*	host-to-function DMA data access window

Table 52. SD_F2H_DDAW register - SDIO function-to-host DMA data access window (FN1 0 0110h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	DMA_DAW[7:0]	-	R	00h*	function-to-host DMA data access window

Table 53. SD_LOC_MBn[1] register - SDIO local mailbox n (FN1 0 0114h to 0 0120h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	MBOX_DATA[7:0]	R	R/W[2]	00h*	mailbox data

[1] Register definition is the same for all local mailboxes; replace n with the mailbox number (0 to 3).

[2] Writing to this register generates an interrupt to the local microcontroller if bit LMBn_INT_EN is set in register SD_LOC_ISCR; see Table 48. A local read clears the interrupt.

Table 54. SD_LOC_SRn[1] register - SDIO local scratch register n (FN1 0 0128h to 0 0134h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	SCRCH_DATA[7:0]	R	R/W	00h*	scratch data

[1] Register definition is the same for all local scratch registers; replace n with the scratch register number (0 to 3).

Table 55. SD_HST_MBn[1] register - SDIO host mailbox n (FN1 0 013Ch to 0 0148h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	MBOX_DATA[7:0]	R/W[2]	R	00h*	mailbox data

[1] Register definition is the same for all host mailboxes; replace n with the mailbox number (0 to 3).

[2] Writing to this register generates an interrupt to the SDIO host if bit HMBn_INT_EN is set in register SD_HST_ISCR (see Table 49). A host read clears the interrupt.

Table 56. SD_HST_SRn[1] register - SDIO host scratch register n (FN1 0 0150h to 0 015Ch)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	SCRCH_DATA[7:0]	R/W	R	00h*	scratch data

[1] Register definition is the same for all host scratch registers; replace n with the scratch register number (0 to 3).

Table 57. SD_RST_CR register - SDIO reset control (FN1 0 0164h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 3	-	R	R	00h*	reserved
2	SDIO_HOST_RST	R/W	R		SDIO interface host side reset status
				0*	SDIO interface host side operational
				1	SDIO interface host side reset ongoing
1	SDIO_FUNC_RST	R/W	R		SDIO interface function side reset status
				0*	SDIO interface function side operational
				1	SDIO interface function side reset ongoing
0	SA2443A_RST	R	R/W		SA2443A reset control
				0*	do not reset SA2443A
				1	reset SA2443A. A host write to this bit will result in the SA2443A being reset.

Table 58. SD_DMA_ISCR register - SDIO DMA interrupt status and control (FN1 0 0168h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7	H2F1_INT_EN	R/W	R		host-to-function DMA channel 1 interrupt control
				0*	interrupt disabled
				1	interrupt will be generated on transfer completion
6	H2F0_INT_EN	R/W	R		host-to-function DMA channel 0 interrupt control
				0*	interrupt disabled
				1	interrupt will be generated on transfer completion
5	F2H1_INT_EN	R/W	R		function-to-host DMA channel 1 interrupt control
				0*	interrupt disabled
				1	interrupt will be generated on transfer completion
4	F2H0_INT_EN	R/W	R		function-to-host DMA channel 0 interrupt control
				0*	interrupt disabled
				1	interrupt will be generated on transfer completion
3	H2F1_INT_STAT	R[1]	R		host-to-function DMA channel 1 interrupt status
				0*	no interrupt pending
				1	transfer complete interrupt pending
2	H2F0_INT_STAT	R[1]	R		host-to-function DMA channel 0 interrupt status
				0*	no interrupt pending
				1	transfer complete interrupt pending
1	F2H1_INT_STAT	R[1]	R		function-to-host DMA channel 1 interrupt status
				0*	no interrupt pending
				1	transfer complete interrupt pending
0	F2H0_INT_STAT	R[1]	R		function-to-host DMA channel 0 interrupt status
				0*	no interrupt pending
				1	transfer complete interrupt pending

[1] This bit will be cleared by a local read.

Table 59. SD_H2F_DSIZEL register - SDIO host-to-function DMA data size - lower byte (FN1 0 0198h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	DATA_SIZE[7:0]	-	R/W	00h*	host-to-function DMA data size (lower byte)

Table 60. SD_H2F_DSIZEH register - SDIO host-to-function DMA data size - upper byte (FN1 0 019Ch)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	DATA_SIZE[15:8]	-	R/W	00h*	host-to-function DMA data size (upper byte)

Table 61. SD_F2H_DSIZEL register - SDIO function-to-host DMA data size - lower byte (FN1 0 01A0h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	DATA_SIZE[7:0]	-	R	00h*	host-to-function DMA data size (lower byte)

Table 62. SD_F2H_DSIZEH register - SDIO function-to-host DMA data size - upper byte (FN1 0 01A4h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	DATA_SIZE[15:8]	-	R	00h*	host-to-function DMA data size (upper byte)

Table 63. SD_F2H_DMAERR register - SDIO function-to-host DMA error (FN1 0 01A8h)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	CRC_ERR[7:0]	-	R/W	00h*	function-to-host DMA CRC error found[1]

[1] A read or write to this register by the host will indicate that a CRC error was found on the most recent function-to-host DMA transfer.

Table 64. SD_F2H_DMAOK register - SDIO function-to-host DMA OK (FN1 0 01ACh)

*Legend: * reset value*

Bit	Symbol	Access		Value	Description
		Local	Host		
7 to 0	CRC_OK[7:0]	-	R/W	00h*	no function-to-host DMA CRC error found[1]

[1] A read or write to this register by the host will indicate that no CRC error was found on the most recent function-to-host DMA transfer.

10.16 General-purpose I/O unit

11 programmable general-purpose I/Os are provided on the SA2443A.

Each GPIO can be configured as either an input or an output. Registers are provided to allow data to be written to and read from the GPIO pins.

When configured as an input the circuit can be configured as plain, pull-up, pull-down or repeater (the repeater option allows the last driven state on the pin to be held).

Many of the GPIO pins are multiplexed with other functions; see Table 2.

11. Limiting values

Table 65. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DDA(VCO)}$	VCO analog supply voltage			–0.5	+3.85	V
V_{DDA}	analog supply voltage			–0.5	+3.85	V
$V_{DDD(IO)}$	I/O digital supply voltage			–0.5	+4.6	V
$V_{DDD(C)}$	core digital supply voltage			–0.5	+2.5	V
$V_{DD(PA)}$	power amplifier supply voltage			–0.5	+3.85	V
$V_{DD(DRIVER)}$	driver supply voltage			–0.5	+3.85	V
$V_{DDA(RF)}$	RF analog supply voltage			–0.5	+3.85	V
V_I	input voltage			–0.5	$V_{DDD(IO)}$ + 0.5	V
I_{latch}	latch-up current	$V_I < 0$ V or $V_I > V_{DD}$	[1]	-	100	mA
V_{esd}	electrostatic discharge voltage	HBM	[2]	–1000	+1000	V
		MM	[3]	–200	+200	V
		CDM	[4]	–500	+500	V
T_{stg}	storage temperature			–55	+155	°C

[1] JEDEC standard JESD78A, IC latch-up test.

[2] JEDEC standard JESD22-A114-D, Electrostatic Discharge (ESD) sensitivity testing Human Body Model (HBM).

[3] JEDEC standard JESD22-A115-A, Electrostatic Discharge (ESD) sensitivity testing Machine Model (MM).

[4] JEDEC standard JESD22-C101C, field-induced Charged Device Model (CDM) test method for electrostatic discharge withstand thresholds of microelectronic components.

12. Recommended operating conditions

Table 66. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DDA(VCO)}$	VCO analog supply voltage		[1]	2.7	2.85	3.0	V
V_{DDA}	analog supply voltage		[1]	2.7	2.85	3.0	V
$V_{DDD(IO)}$	I/O digital supply voltage		[1]	2.7	2.85	3.0	V
$V_{DDD(C)}$	core digital supply voltage			1.65	1.8	1.95	V
$V_{DD(PA)}$	power amplifier supply voltage			2.7	2.85	3.0	V
$V_{DD(DRIVER)}$	driver supply voltage			2.7	2.85	3.0	V
$V_{DDA(RF)}$	RF analog supply voltage			2.7	2.85	3.0	V
T_{amb}	ambient temperature			–30	+25	+85	°C

[1] It is possible to extend the voltage range of the baseband and radio supplies up to $V_{DD(PA)}$ + 0.6 V (see Section 22 “Contact information”).

13. Static characteristics

Table 67. Supply characteristics

All values at nominal supply voltage; T_{amb} = 25 °C; channel 6; unless otherwise stated.

Symbol	Parameter	Conditions[1]		Min	Typ	Max	Unit
Core logic supply							
$V_{DDD(C)}$	core digital supply voltage			1.65	1.8	1.95	V
$I_{DD(C)(sleep)}$	sleep core supply current		[2]	-	80	-	µA
$I_{DD(C)(rcv)}$	receive core supply current	see Figure 20	[3]	-	93.9	99.5	mA
$I_{DD(C)(tx)}$	transmit core supply current			-	16.0	17.5	mA
Digital I/O, analog RF and VCO supplies							
V_{DD}	supply voltage			2.7	2.85	3.0	V
$I_{DDA(sleep)}$	sleep analog supply current	$I_{DDA(RF)(sleep)}$ + $I_{DDA(VCO)(sleep)}$ + $I_{DDD(IO)(sleep)}$	[2]	-	25	-	µA
$I_{DDA(rcv)}$	receive analog supply current	$I_{DDA(RF)(rcv)}$ + $I_{DDA(VCO)(rcv)}$ + $I_{DDD(IO)(rcv)}$; see Figure 21	[3]	-	111.5	120	mA
$I_{DDA(tx)}$	transmit analog supply current	$I_{DDA(RF)(tx)}$ + $I_{DDA(VCO)(tx)}$ + $I_{DDD(IO)(tx)}$; see Figure 22		-	94.2	103	mA
PA and driver supply							
V_{DDA2}	analog supply voltage 2			2.7	2.85	3.0	V
I_{DDA2}	analog supply current 2	$I_{DD(PA)(sleep)}$ + $I_{DD(DRIVER)(sleep)}$	[2]	-	10	-	µA
		$I_{DD(PA)(rcv)}$ + $I_{DD(DRIVER)(rcv)}$	[3]	-	10	-	µA
		$I_{DD(PA)(tx)}$ + $I_{DD(DRIVER)(tx)}$; see Figure 23		-	177.5	197.6	mA

[1] All current measurements are made on the evaluation board.

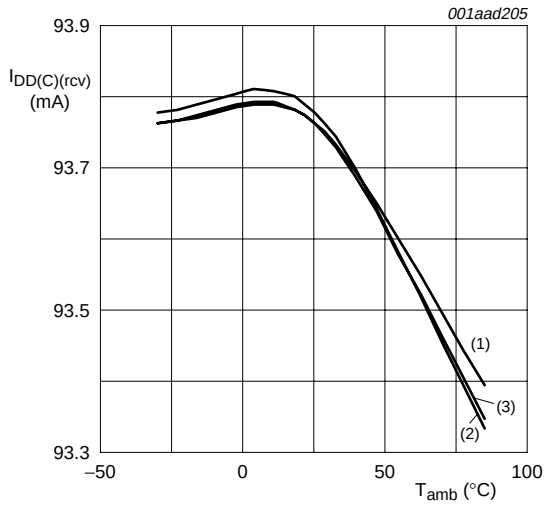
[2] Sleep mode is defined for the low-power state where the system is inactive but still able to wake up to receive beacons.

[3] Receive current is defined as the average current measured for 1024-byte packets at 11 Mbit/s data rate with a short preamble and 200 µs idle time.

Table 68. Digital input/output characteristics

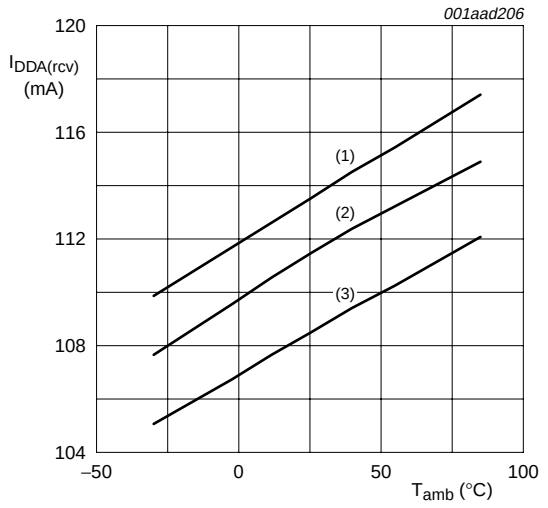
$V_{DDD(C)}$ = 1.8 V ± 0.15 V; typical values at T_{amb} = 25 °C; unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input levels						
V_{IL}	LOW-level input voltage		–0.5	-	$+0.3V_{DDD(IO)}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD(IO)}$	-	$V_{DDD(IO)}$ + 0.5	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA	$V_{DDD(IO)}$ – 0.4	-	-	V
Input current						
$I_{I(pd)}$	pull-down input current	$V_{IH} = V_{DDD(IO)}$	-	61	100	µA
$I_{I(pu)}$	pull-up input current	V_{IL} = 0 V	–10	+0.35	-	µA



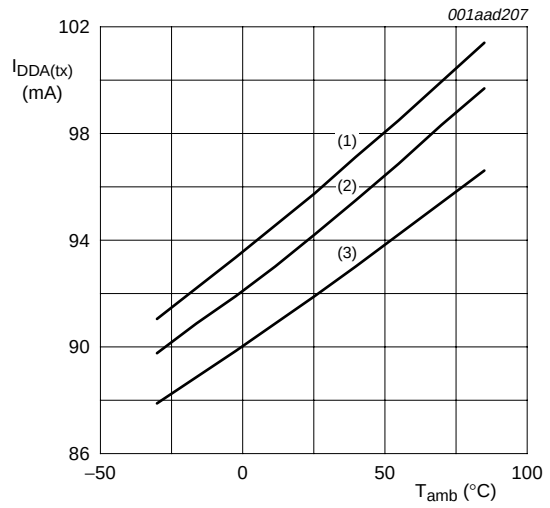
(1) V_{DD} = 1.95 V
(2) V_{DD} = 1.65 V
(3) V_{DD} = 1.8 V

Fig 20. Core supply current in receive mode as a function of temperature



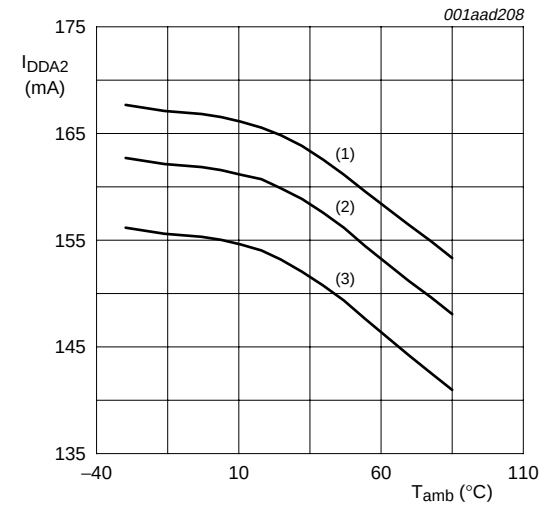
(1) V_{DD} = 3.0 V
(2) V_{DD} = 2.85 V
(3) V_{DD} = 2.7 V

Fig 21. Digital I/O, analog RF and VCO supply current in receive mode as a function of temperature



(1) V_{DD} = 3.0 V
(2) V_{DD} = 2.85 V
(3) V_{DD} = 2.7 V

Fig 22. Digital I/O, analog RF and VCO supply current in transmit mode for 11 Mbit/s at fixed gain setting CFh as a function of temperature



(1) V_{DD} = 3.0 V
(2) V_{DD} = 2.85 V
(3) V_{DD} = 2.7 V

Fig 23. Driver and power amplifier supply current for 11 Mbit/s at fixed gain setting CFh as a function of temperature

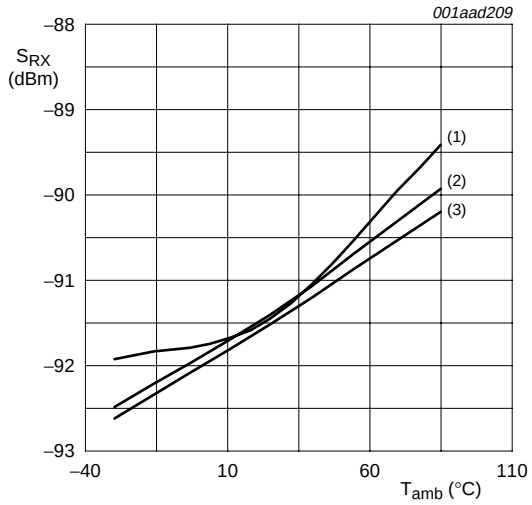
14. Dynamic characteristics

14.1 Receiver

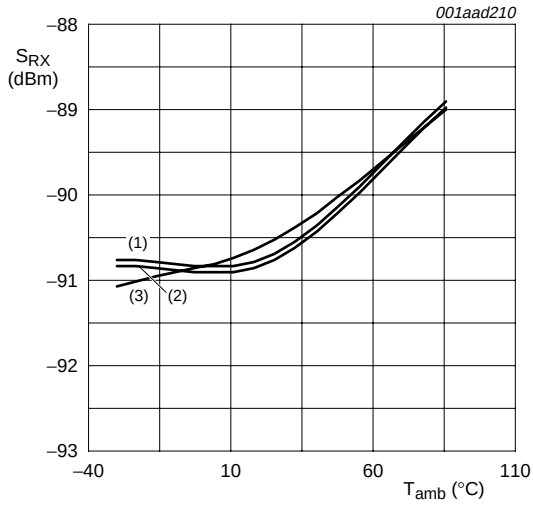
Table 69. Receiver characteristics

All values at nominal supply voltage; T_{amb} = 25 °C; channel 6; unless otherwise stated.

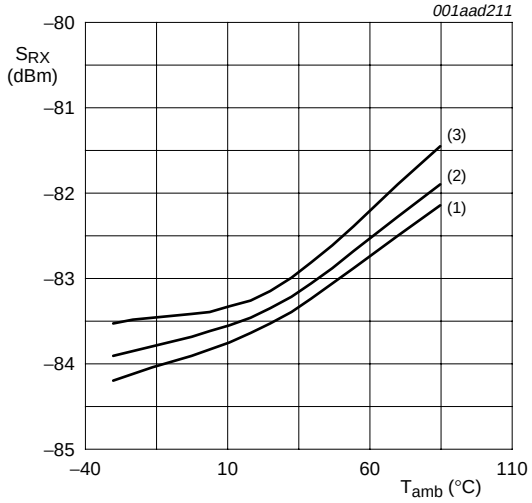
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Receiver sensitivity; see Figure 24						
S_{RX}	receiver sensitivity	PER < 8 %; PSDU = 1024 bytes				
		1 Mbit/s	-	–91	-	dBm
		2 Mbit/s	-	–87	-	dBm
		5.5 Mbit/s	-	–83	-	dBm
		11 Mbit/s	–84	–83	–80	dBm
		11 Mbit/s on pin ANT_AUX	-	–83	-	dBm
Maximum input level						
$V_{i(max)}$	maximum input voltage	PER < 8 %; PSDU = 1024 bytes				
		2 Mbit/s	-	–0.4	-	dBm
		11 Mbit/s	-	0.6	-	dBm
Adjacent channel rejection						
ACR	adjacent channel rejection	PER < 8 %; PSDU = 1024 bytes				
		11 Mbit/s	-	41	-	dB
Receiver tolerances						
Δt_d	delay time variation	during frame; PER < 8 %; exponential delay profile	-	200	-	ns
Out-of-band signal blocking						
$\alpha_{sup(oob)}$	out-of-band suppression	resulting in 1 dB sensitivity loss				
		824 MHz to 915 MHz signal blocking	-	–22	-	dBm
		1710 MHz to 1910 MHz signal blocking	-	–24	-	dBm
		1920 MHz to 1980 MHz signal blocking	-	–24	-	dBm



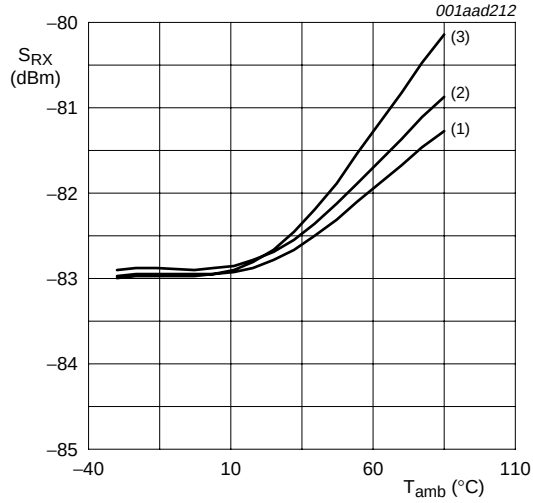
a. 1 Mbit/s packets in channel 1



b. 1 Mbit/s packets in channel 14



c. 11 Mbit/s packets in channel 1



d. 11 Mbit/s packets in channel 14

(1) V_{DD} = 2.7 V

(2) V_{DD} = 2.85 V

(3) V_{DD} = 3.0 V

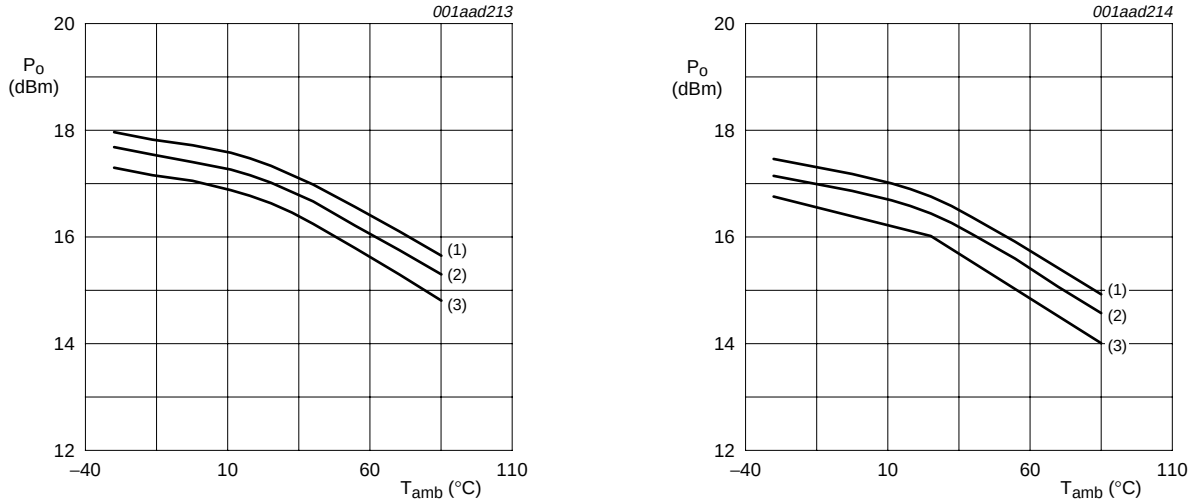
Fig 24. Receiver sensitivity as a function of temperature

14.2 Transmitter

Table 70. Transmitter characteristics

All values at nominal supply voltage; T_{amb} = 25 °C; channel 6; unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Linear output power; see Figure 25 to Figure 26						
P_o	output power	meets FCC restricted band specifications				
		1 Mbit/s and 2 Mbit/s	12.6	16.1	18.4	dBm
		5.5 Mbit/s and 11 Mbit/s	14.3	17.6	20.1	dBm
Transmit spectrum mask; see Figure 27 to Figure 28						
ACPR	adjacent channel power ratio	typical linear output power; f_{lo} – 22 MHz < f < f_{lo} – 11 MHz and f_{lo} + 11 MHz < f < f_{lo} + 22 MHz; RMS detection				
		1 Mbit/s and 2 Mbit/s	-	–32	-	dBr
		5.5 Mbit/s and 11 Mbit/s	-	–33	-	dBr
$ACPR_{alt}$	alternate adjacent channel power ratio	typical linear output power; f < f_{lo} – 22 MHz and f > f_{lo} + 22 MHz; RMS detection				
		1 Mbit/s and 2 Mbit/s	-	–51	-	dBr
		5.5 Mbit/s and 11 Mbit/s	-	–55	-	dBr
Transmit modulation accuracy						
EVM	error vector magnitude	typical linear output power; as defined in IEEE 802.11b - 1999 specification section 18.4.7.8				
		1 Mbit/s	-	16	-	%
		2 Mbit/s	-	19	-	%
		5.5 Mbit/s	-	17	-	%
		11 Mbit/s	-	17	35	%
Transmit power-on and power-down ramp						
$t_{r(pu)}$	power-up rise time	for 10 % to 90 % output power; typical linear output power	-	1.2	-	µs
$t_{f(pd)}$	power-down fall time	for 90 % to 10 % output power; typical linear output power	-	0.13	-	µs
Other spectral parameters						
$P_{L(fc)}/P_{tx(tot)}$	center frequency power leakage relative to the overall transmit power	typical linear output power; 2 Mbit/s	-	–20	–15	dB
α_{2H}	second harmonic level	typical linear output power; 1 MHz resolution bandwidth; peak detection	-	–32	-	dBm
α_{3H}	third harmonic level	typical linear output power; 1 MHz resolution bandwidth; peak detection	-	–40	-	dBm
N_{WB}	wideband noise	15 dBm output power				
		in frequency range 869 MHz to 1.990 GHz	-	–135	-	dBm/Hz
		in frequency range 2.110 GHz to 2.170 GHz	-	–130	-	dBm/Hz



a. 11 Mbit/s modulation in channel 1

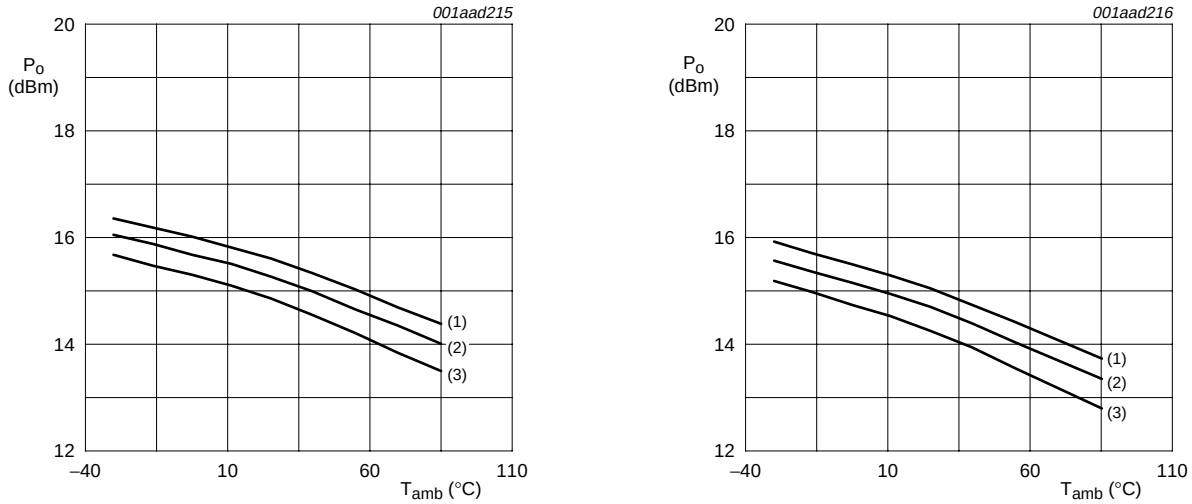
b. 11 Mbit/s modulation in channel 11

(1) V_{DD} = 3.0 V

(2) V_{DD} = 2.85 V

(3) V_{DD} = 2.7 V

Fig 25. Output power at gain setting CFh as a function of temperature



a. 1 Mbit/s modulation in channel 1

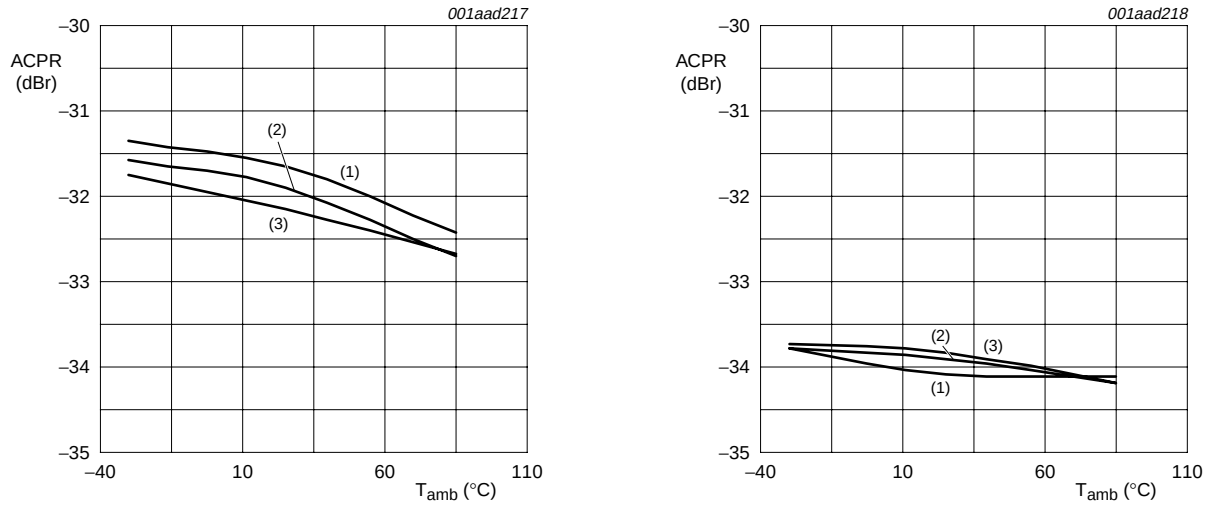
b. 11 Mbit/s modulation in channel 1

(1) V_{DD} = 3.0 V

(2) V_{DD} = 2.85 V

(3) V_{DD} = 2.7 V

Fig 26. Output power at gain setting AFh as a function of temperature



a. 11 Mbit/s modulation in channel 1

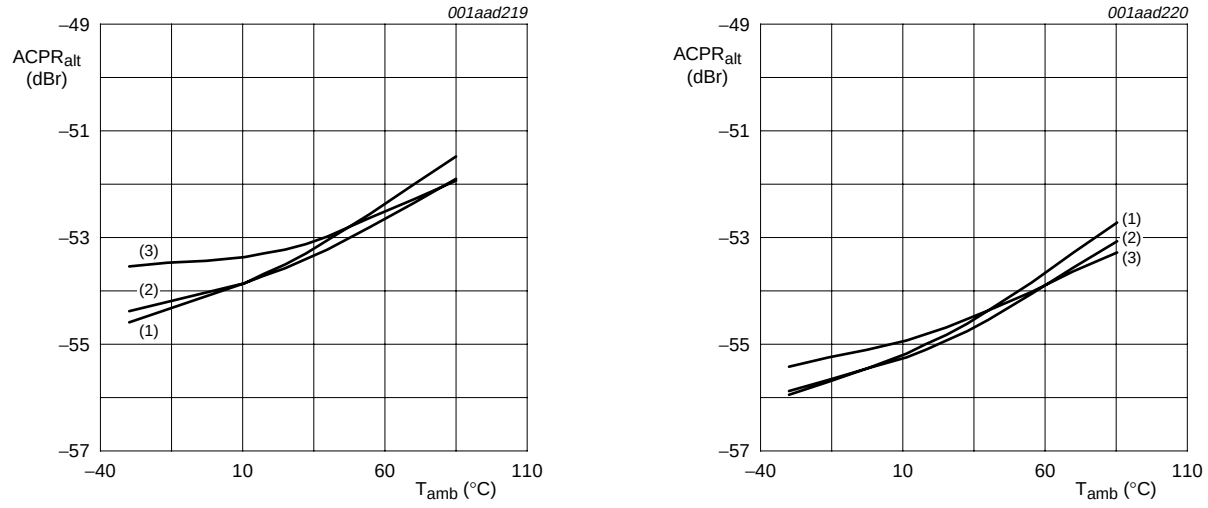
b. 11 Mbit/s modulation in channel 11

(1) V_{DD} = 2.7 V

(2) V_{DD} = 2.85 V

(3) V_{DD} = 3.0 V

Fig 27. Adjacent channel power ratio at gain setting CFh as a function of temperature



a. 11 Mbit/s modulation in channel 1

b. 11 Mbit/s modulation in channel 11

(1) V_{DD} = 3.0 V

(2) V_{DD} = 2.85 V

(3) V_{DD} = 2.7 V

Fig 28. Alternate adjacent channel power ratio at gain setting CFh as a function of temperature

14.3 Clock and reset

Table 71. Dynamic characteristics for clock and reset signals

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reference clock; see Figure 29						
$f_{clk(ref)}$	reference clock frequency		43.9889	44.0000	44.0011	MHz
$t_{wH(clk)(ref)}$	reference clock HIGH pulse width		10.5	-	-	ns
$t_{wL(clk)(ref)}$	reference clock LOW pulse width		10.5	-	-	ns
Sleep clock; see Figure 30						
$f_{clk(sleep)}$	sleep clock frequency		28	32	1000	kHz
$t_{wH(clk)(sleep)}$	sleep clock HIGH pulse width		50.0	-	-	ns
$t_{wL(clk)(sleep)}$	sleep clock LOW pulse width		50.0	-	-	ns
Reset; see Figure 31						
$t_{wL(RST\_N)}$	RST_N LOW pulse width		10.0	-	-	ns
Power-on reset; see Figure 32						
V_{POR}	power-on reset voltage		-	1.3	-	V
$t_{wL(POR)}$	power-on reset LOW pulse width time		3.5	4.0	4.7	ms

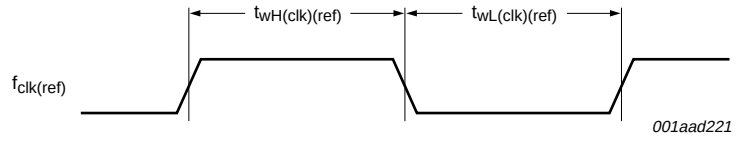


Fig 29. 44 MHz reference clock timing

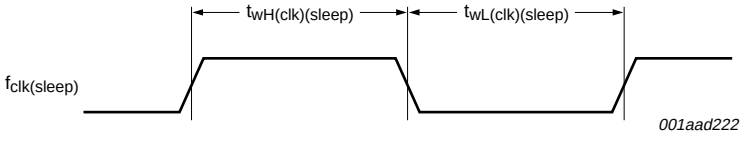


Fig 30. Sleep clock timing

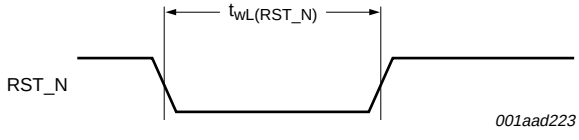


Fig 31. Reset timing

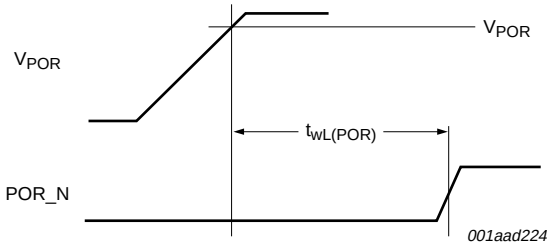


Fig 32. Power-on reset timing

14.4 SPI1 interface

Table 72. Dynamic characteristics for SPI1

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI clock input; see Figure 33						
T_{SPI_SCK}	SPI_SCK period		120.0	-	-	ns
$t_{clk(H)}$	clock HIGH time		50.0	-	-	ns
$t_{clk(L)}$	clock LOW time		50.0	-	-	ns
SPI slave select input; see Figure 35 and Figure 36						
$t_{su(SPI\_SS\_N)}$	SPI_SS_N set-up time		100.0	-	-	ns
$t_{h(SPI\_SS\_N)}$	SPI_SS_N hold time		100.0	-	-	ns
SPI_MOSI output; see Figure 33 and Figure 34;						
$t_{d(o)(SPI\_MOSI)}$	SPI_MOSI output delay time	C_L = 10 pF	-	-	5.0	ns
$t_{h(o)(SPI\_MOSI)}$	SPI_MOSI output hold time	C_L = 10 pF	–1.0	-	-	ns
SPI_MOSI input; see Figure 35 and Figure 36						
$t_{su(SPI\_MOSI)}$	SPI_MOSI set-up time		3.0	-	-	ns
$t_{h(i)(SPI\_MOSI)}$	SPI_MOSI input hold time		2.0	-	-	ns
SPI_MISO output; see Figure 35 and Figure 36						
$t_{en(o)(SPI\_MISO)}$	SPI_MISO output enable time	C_L = 10 pF	-	-	10.0	ns
$t_{dis(o)(SPI\_MISO)}$	SPI_MISO output disable time	C_L = 10 pF	-	-	10.0	ns
$t_{d(o)(SPI\_MISO)}$	SPI_MISO output delay time	C_L = 10 pF	-	-	100.0	ns
$t_{h(o)(SPI\_MISO)}$	SPI_MISO output hold time	C_L = 10 pF	0.0	-	-	ns
SPI_MISO input; see Figure 33 and Figure 34						
$t_{su(SPI\_MISO)}$	SPI_MISO set-up time		20.0	-	-	ns
$t_{h(i)(SPI\_MISO)}$	SPI_MISO input hold time		5.0	-	-	ns

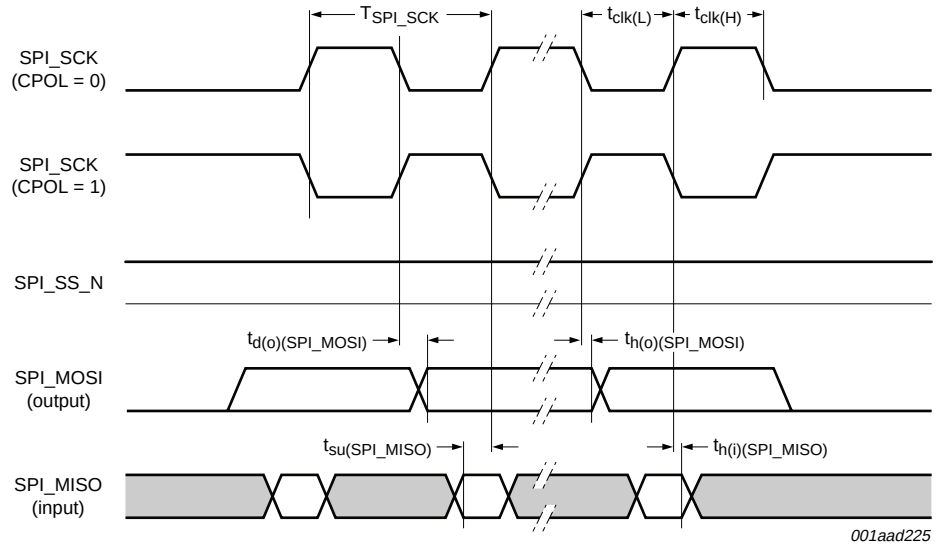


Fig 33. SPI1 master timing (CPHA = 0)

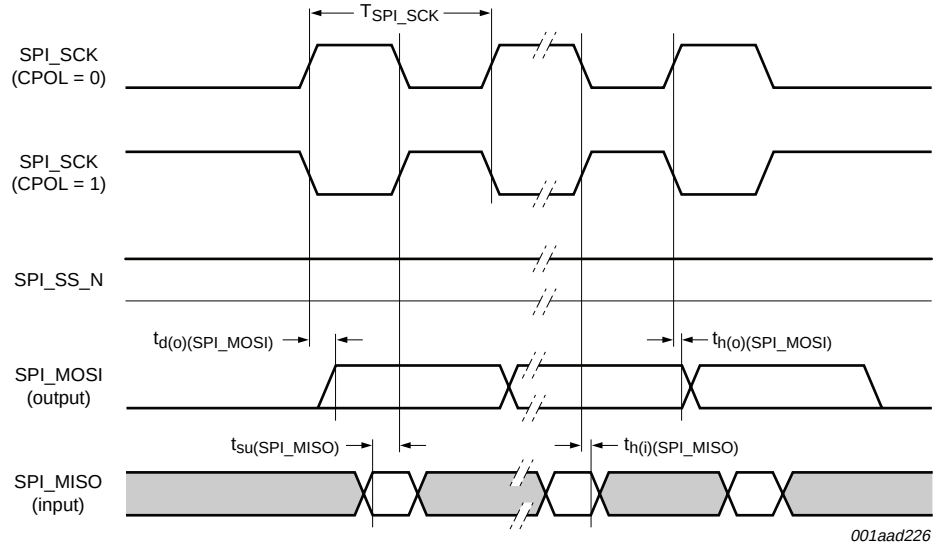


Fig 34. SPI1 master timing (CPHA = 1)

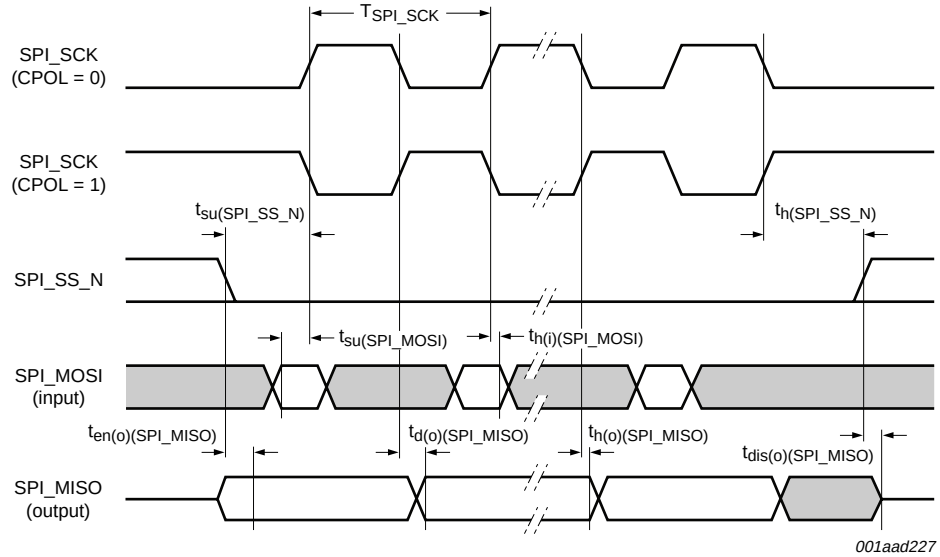


Fig 35. SPI1 slave timing (CPHA = 0)

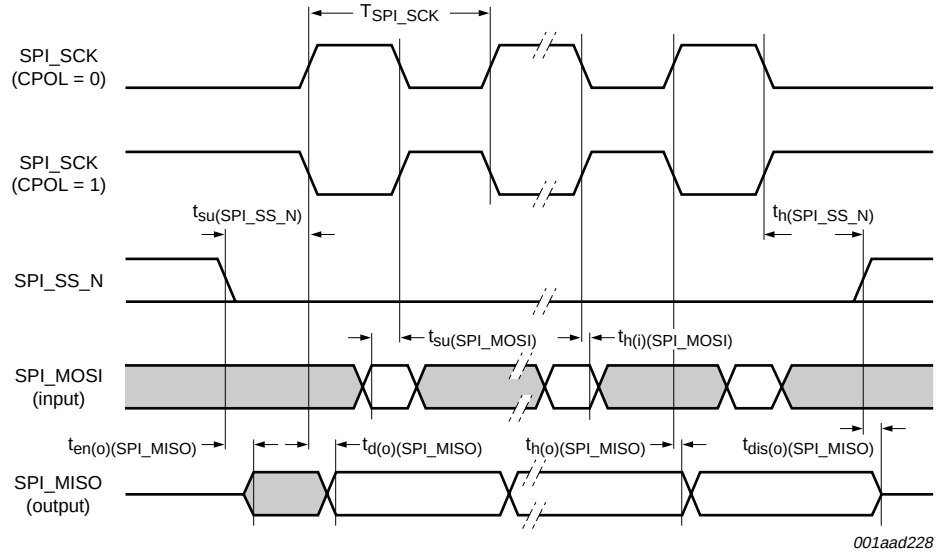


Fig 36. SPI1 slave timing (CPHA = 1)

14.5 SPI2 interface

Table 73. Dynamic characteristics for SPI2

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
SPI clock input; see Figure 37 and Figure 38							
T_{SPI_SCK}	SPI_SCK period			15.0	-	-	ns
$t_{clk(H)}$	clock HIGH time			7.0	-	-	ns
$t_{clk(L)}$	clock LOW time			7.0	-	-	ns
SPI slave select input; see Figure 37 and Figure 38							
$t_{su(SPI\_SS\_N)}$	SPI_SS_N set-up time			3.0	-	-	ns
$t_{h(SPI\_SS\_N)}$	SPI_SS_N hold time			0.0	-	-	ns
SPI_MOSI input; see Figure 37 and Figure 38							
$t_{su(SPI\_MOSI)}$	SPI_MOSI set-up time			4.0	-	-	ns
$t_{h(i)(SPI\_MOSI)}$	SPI_MOSI input hold time			0.0	-	-	ns
SPI_MISO output; see Figure 37 and Figure 38							
$t_{en(o)(SPI\_MISO)}$	SPI_MISO output enable time	C_L = 10 pF		-	-	8.0	ns
$t_{dis(o)(SPI\_MISO)}$	SPI_MISO output disable time	C_L = 10 pF		-	-	6.0	ns
$t_{d(o)(SPI\_MISO)}$	SPI_MISO output delay time	C_L = 10 pF; negative edge	[1]	-	-	10.0	ns
		C_L = 10 pF; positive edge	[2]	-	-	10.0	ns
$t_{h(o)(SPI\_MISO)}$	SPI_MISO output hold time	C_L = 10 pF; negative edge	[1]	0.0	-	-	ns
		C_L = 10 pF; positive edge	[2]	3.0	-	-	ns

[1] When clocked from negative edge of SPI_SCK.

[2] When clocked from positive edge of SPI_SCK.

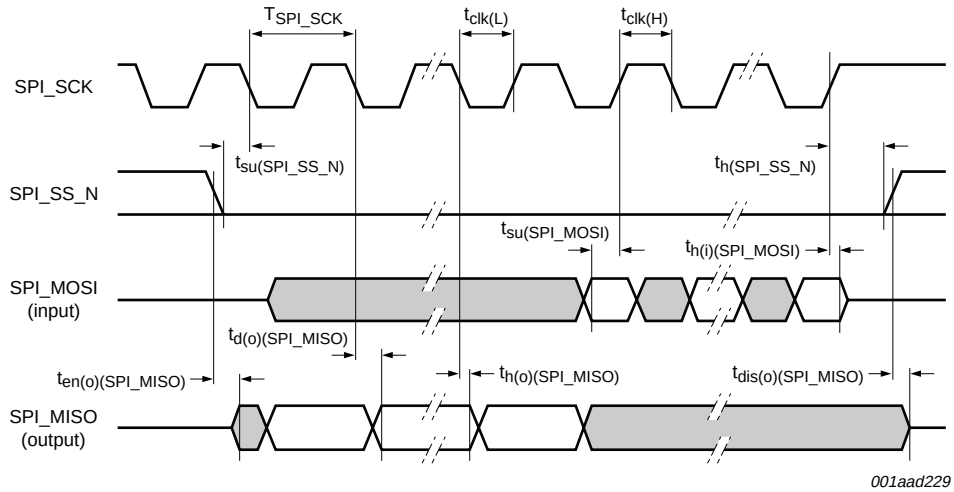


Fig 37. SPI2 timing (SPI_MISO clocked on negative edge of SPI_SCK)

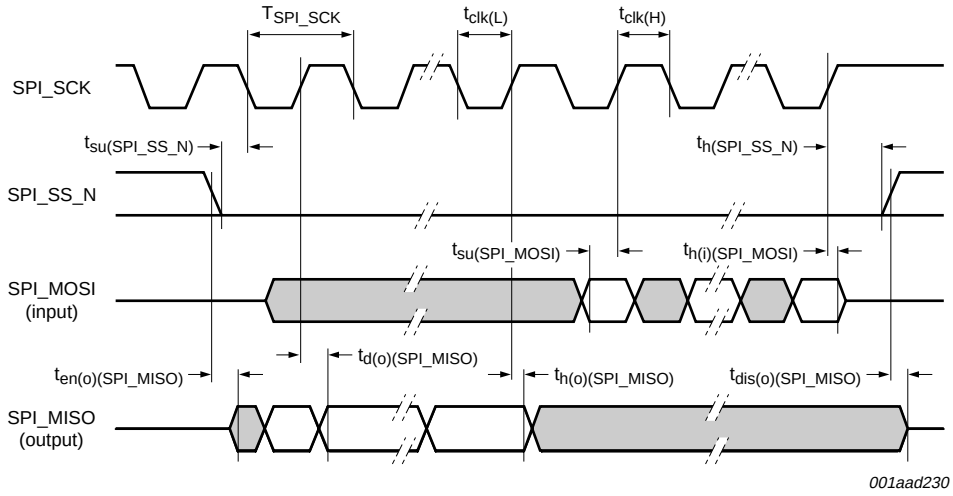


Fig 38. SPI2 timing (SPI_MISO clocked on positive edge of SPI_SCK)

14.6 SDIO interface

Table 74. Dynamic characteristics for the SDIO interface

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SD clock input; see Figure 39						
T_{SD_CLK}	SD_CLK period		40.0	-	-	ns
$t_{clk(H)}$	clock HIGH time		10.0	-	-	ns
$t_{clk(L)}$	clock LOW time		10.0	-	-	ns
SD command input/output; see Figure 39						
$t_{su(i)(SD\_CMD)}$	SD_CMD input set-up time		5.0	-	-	ns
$t_{h(i)(SD\_CMD)}$	SD_CMD input hold time		5.0	-	-	ns
$t_{d(o)(SD\_CMD)}$	SD_CMD output delay time	C_L = 10 pF	-	-	14.0	ns
$t_{h(o)(SD\_CMD)}$	SD_CMD output hold time	C_L = 10 pF	0.0	-	-	ns
SD data input/output; see Figure 39						
$t_{su(i)(SD\_DATx)}$	SD_DATx input set-up time		5.0	-	-	ns
$t_{h(i)(SD\_DATx)}$	SD_DATx input hold time		5.0	-	-	ns
$t_{d(o)(SD\_DATx)}$	SD_DATx output delay time	C_L = 10 pF	-	-	14.0	ns
$t_{h(o)(SD\_DATx)}$	SD_DATx output hold time	C_L = 10 pF	0.0	-	-	ns

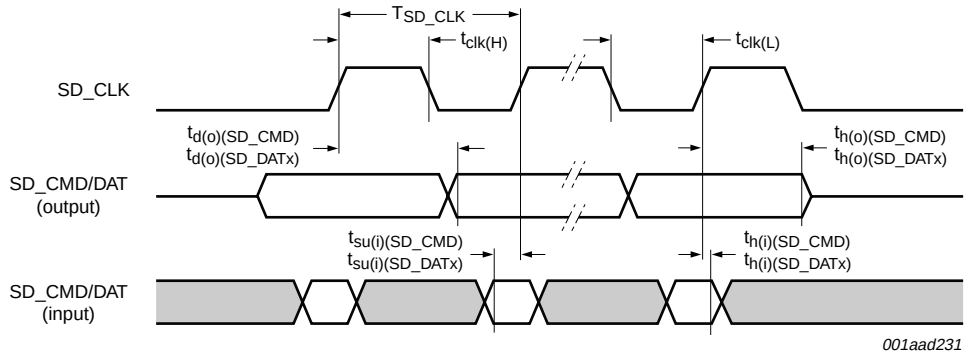
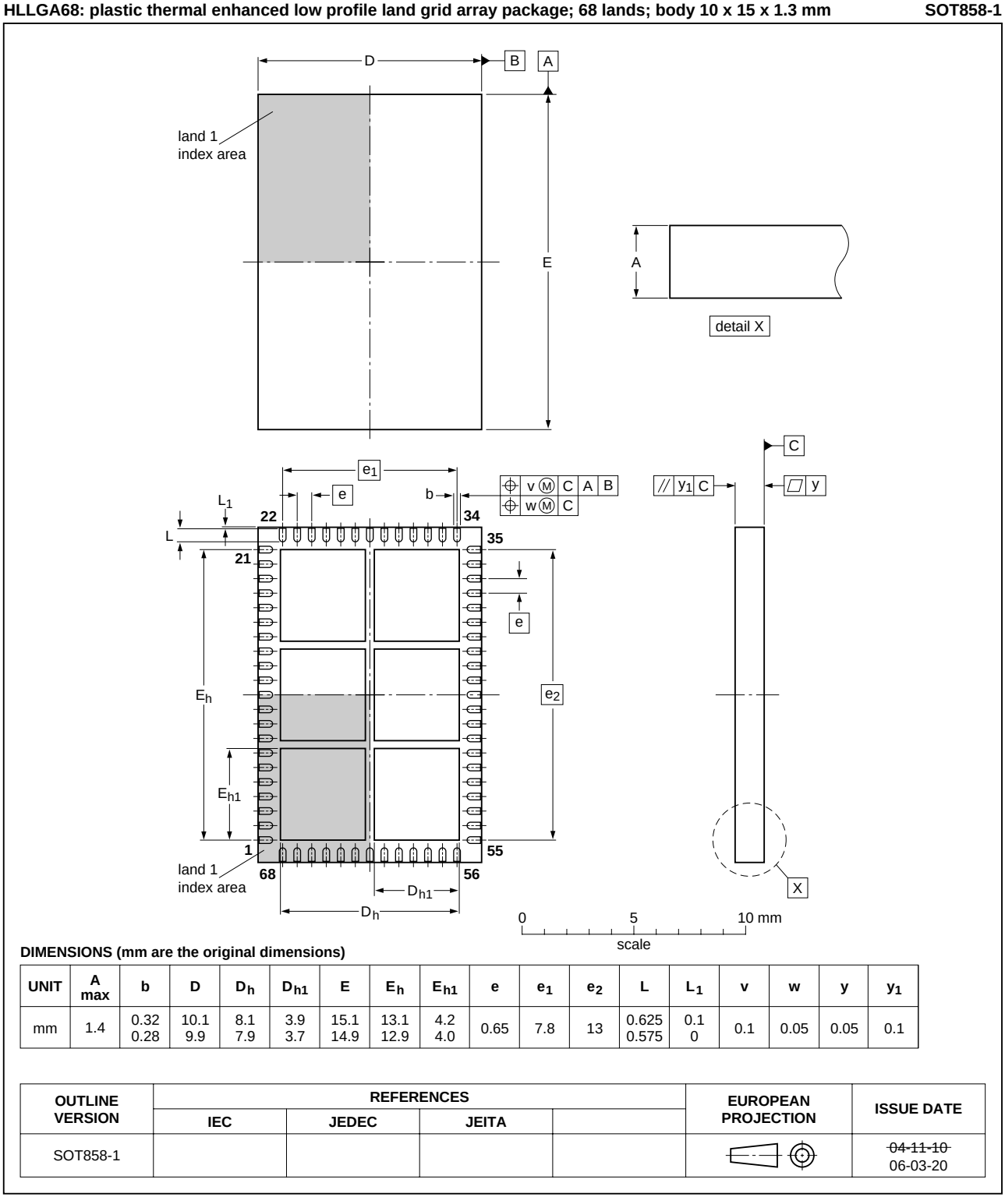


Fig 39. SDIO interface timing

15. Package outline

HLLGA68: plastic thermal enhanced low profile land grid array package; 68 lands; body 10 x 15 x 1.3 mm **SOT858-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	b	D	D_h	D_{h1}	E	E_h	E_{h1}	e	e_1	e_2	L	L_1	v	w	y	y_1
mm	1.4	0.32 0.28	10.1 9.9	8.1 7.9	3.9 3.7	15.1 14.9	13.1 12.9	4.2 4.0	0.65	7.8	13	0.625 0.575	0.1 0	0.1	0.05	0.05	0.1

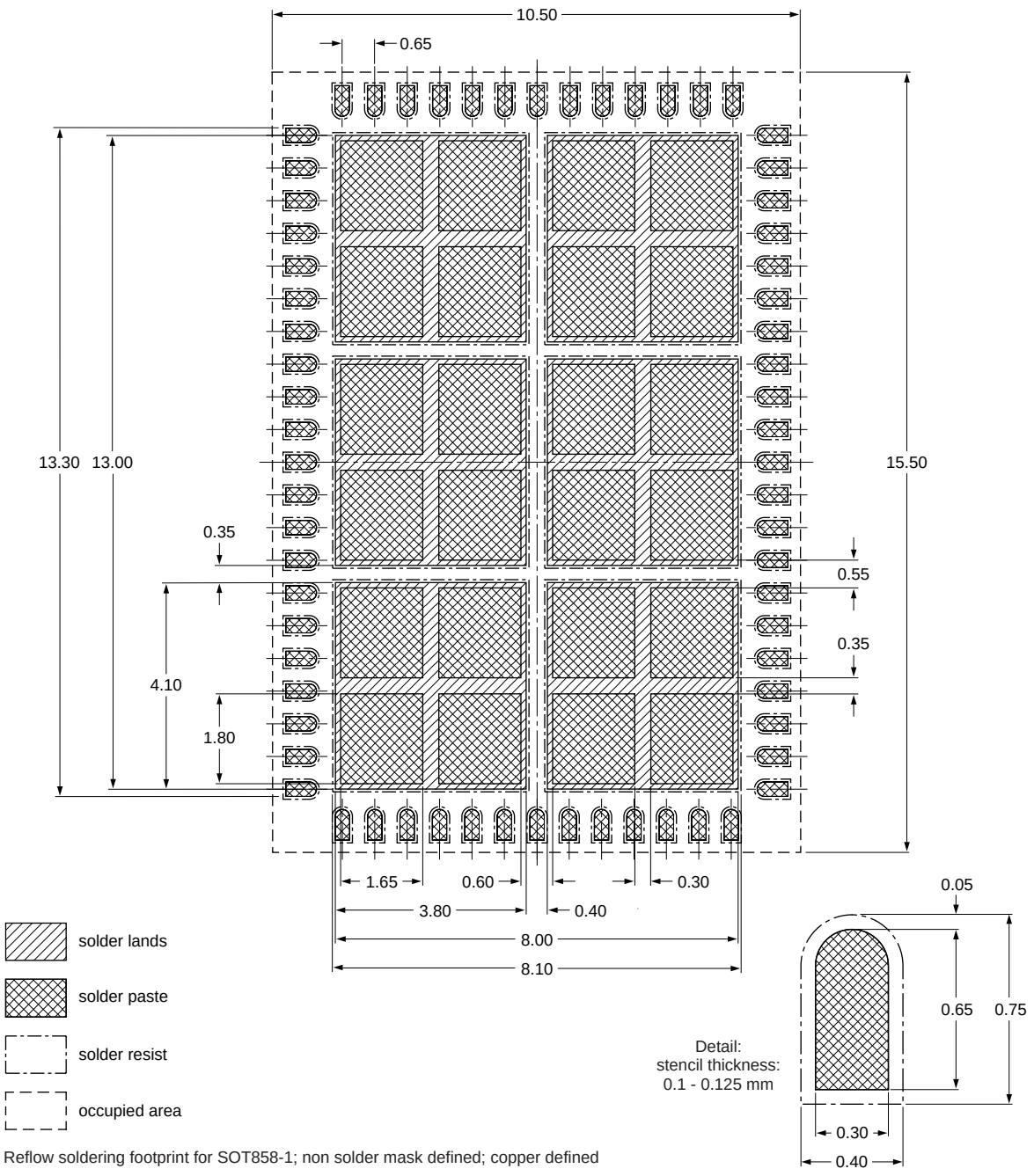
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT858-1						~~04-11-10~~ 06-03-20

Fig 40. Package outline SOT858-1 (HLLGA68)

16. Soldering

16.1 Printed-circuit board

16.1.1 PCB footprint layout



Reflow soldering footprint for SOT858-1; non solder mask defined; copper defined

Fig 41. PCB footprint outline

16.1.1.1 Vias design

Through-hole vias in the ground plane should be plugged and preferably have a top metallization. In case that through-hole vias are used to connect the terminal pads, than they should be placed outside the package area to prevent shorts and voids.

Voiding in the solder joints can further be minimized by locating the through-hole vias under the stencil web area or close to the corner of the stencil apertures (see Figure 42).

Microvias can be placed in both central ground pad and terminal pads. Voiding in the solder joints can further be minimized by locating the microvias under the stencil web area or close to the corner of the stencil apertures.

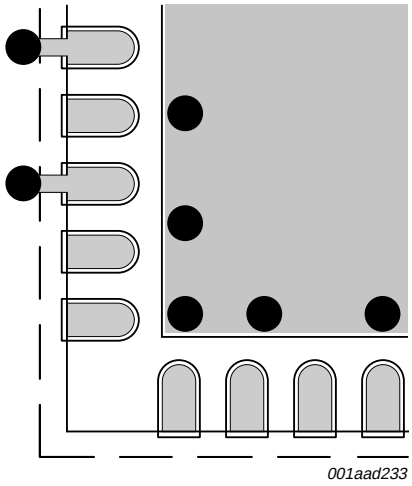


Fig 42. Via placing around solder land

16.1.2 PCB finish

The packages can be used on a variety of PCB finishes such as immersion gold (Ni/Au) or Hot Air Solder Level (HASL) or Organic Surface Protection (OSP).

Ni/Au finish is recommended. OSP is not recommended in cases that OSP does not withstand a Pb-free or a double-sided reflow application.

16.1.3 Stencil design

The stencil opening for terminal pads should be 100 % of solder land size while the stencil openings of the center/ground pad should be divided in an array, such that 80 % to 90 % coverage of the center solder land is achieved. This array of openings minimizes the risk of smearing during stencil print and risk of short circuit or voiding during reflow. Stencil thickness can range from 0.10 mm to 0.15 mm. Using rounded corners, tapered and smoothed walls can further optimize solder paste transfer.

16.2 Soldering

16.2.1 Solder paste

Standard (no-clean) Sn/Pb (63 % / 37 %) or Pb-free solder pastes should be used for soldering the package. Solder pastes should be selected based on their printing and reflow behavior. For Pb-free solder paste it is recommended to use ‘SAC’ type solder paste (e.g. SnAg3.8Cu0.7) with melting point of 217 °C.

16.2.2 Reflow profile

An industrial convection reflow oven should be used to mount the packages. The profile depends on the printed-circuit board and other components that are used in the customer application. For maximum peak temperature JEDEC specification should be followed. Following reflow profile and constraints are recommended for eutectic Sn/Pb and Pb-free reflow solders.

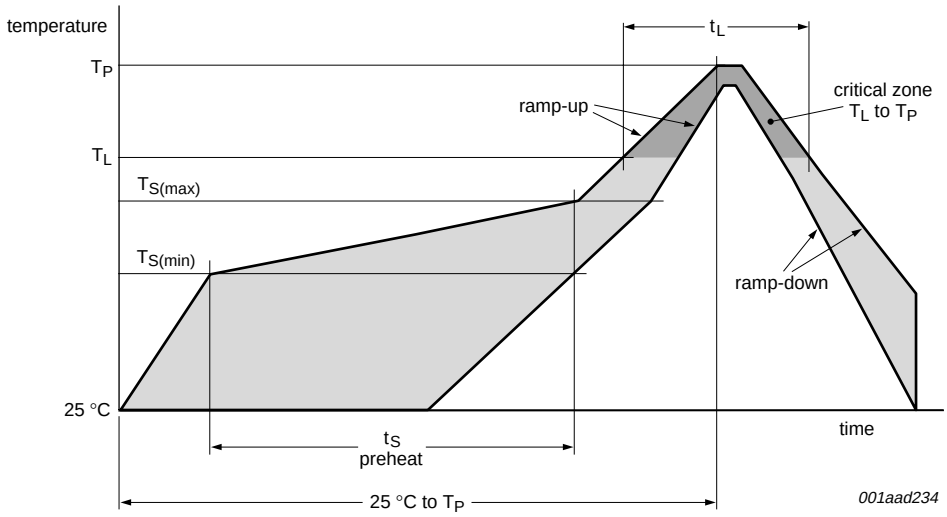


Fig 43. Reflow temperature profile

Table 75. Recommended reflow profile data

Parameter	Eutectic Sn/Pb	Pb-free
Average ramp-up rate [$T_{S(max)}$ to T_P]	3 °C/s maximum	2 °C/s maximum[1]
Preheat		
• Temperature min [$T_{S(min)}$]	100 °C	150 °C
• Temperature max [$T_{S(max)}$]	150 °C	200 °C
• Time t_S [$T_{S(min)}$ to $T_{S(max)}$]	60 s to 120 s	75 s to 90 s (≤ 0.75 °C/s)
Time maintained above		
• Temperature (T_L)	183 °C	217 °C
• Time (t_L)	60 s to 90 s	70 s to 90 s
Maximum peak temperature (T_P)	240 °C (+0 °C to –5 °C)	240 °C to (250 + 0) °C
Time within 5 °C of actual peak temperature (T_P)	10 s to 30 s	20 s to 30 s
Ramp-down rate	> 180 °C: 2 °C/s maximum	> 180 °C: 2 °C/s maximum[1]
	< 180 °C: 6 °C/s maximum	< 180 °C: 6 °C/s maximum
Minimum peak temperature [$T_{P(min)}$]	205 °C	230 °C
Time 25 °C to T_P	4 min to 5 min	4 min to 5 min

[1] Ramp-up and ramp-down is lower than specified in JEDEC J-STD-020C.

16.3 Rework

If rework is needed, then the packages can be removed or reworked using a ‘BGA’ repair station.

The rework process involves the following steps:

1. Component removal
2. Site redresss
3. Solder paste application
4. Repair: component placement and attachment

These steps are discussed in the following sections in more details.

16.3.1 Component removal

The first step in removal of a component is the reflow of solder joints. It is recommended to preheat the PCB to 150 °C using a bottom heater. Heating of the top side of the component should be done using hot air while a special nozzle can be used for this purpose. Excessive airflow should also be avoided since this may cause shifting of adjacent components. Once the joints have reflowed, the vacuum lift-off can start. Because of their small size the vacuum pressure should be kept below 15 inch of Hg. This will prevent damage to the PCB solder land (‘pad lift’). The temperature of the package should not exceed 250 °C during this rework process since damage can occur to either the package or the PCB. The temperature profile depends on the customer application.

16.3.2 Site redress

After the component is removed, the PCB solder land needs to be cleaned properly. It is best to use a combination of a blade-style conductive tool and desoldering braid. The width of the blade should be matched to the maximum width of the footprint and the blade temperature should be low enough not to cause any damage to the circuit board. Flux residues on the PCB can be removed using IsoPropyl Alcohol (IPA).

16.3.3 Solder paste application

It is recommended to reapply solder by dispensing or stencil printing. The amount of solder applied on the terminals should be in the order of 0.08 mg. In case of dispensing, a gage 27 (0.2 mm opening) needle should be used with 0.3 s to 0.4 s shot at 4 bar. For stencil printing a mini stencil of 0.1 mm thickness can be used if application allows room for it.

16.3.4 Repair

A BGA repair station has a vacuum pick-up tool and usually some component alignment possibilities. A split-beam optical system should be used to align the component on the solder lands. This will form an image of leads overlaid on the mating footprint and aid in proper alignment. The placement machine should have the capability of allowing fine adjustments in X, Y, and rotational axes. Manual placement is not recommended, although the package allows 0.1 mm to 0.15 mm misplacement.

For resoldering of the newly placed component the same profile of bottom and top heating should be applied as for soldering.

17. Moisture sensitivity level

Moisture Sensitivity Level (MSL) of the BGW200EG is determined in accordance with JEDEC standard J-STD-020C.

The BGW200EG has MSL level 4 with a floor life of 72 h after opening of the drypack.

18. Chemical content

The BGW200EG is RoHS 2006 compliant and lead free (0 % Pb).

19. Abbreviations

Table 76. Abbreviations

Acronym	Description
ACK	Acknowledge
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AGC	Automatic Gain Control
AHB	Advanced High-performance Bus
ATIM	Announcement Traffic Indication Message
BGA	Ball Grid Array
BT	Bluetooth
CBC-MAC	Cipher Block Chaining Message Authentication Code
CCA	Clear Channel Assessment
CCCR	Card Common Control Register
CCK	Complementary Code Keying
CCM	Counter mode with CBC-MAC
CDM	Charged Device Model
CIS	Card Information Structure
CRC	Cyclic Redundancy Check
CSA	Code Storage Area
CTS	Clear To Send
DCS	Data Communication System
DMA	Direct Memory Access
DSSS	Direct-Sequencing Spread-Spectrum
EDCF	Enhanced Distributed Coordination Function
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
EVM	Error Vector Magnitude
FCC	Federal Communications Commission
FIQ	Fast Interrupt reQuest
FIRDAC	Finite Impulse Response Digital-to-Analog Converter
GPIO	General-Purpose Input/Output
GSM	Global System for Mobile communication
HASL	Hot Air Solder Level
HBM	Human Body Model
HCF	Hybrid Coordination Function
HCI	Host Controller Interface
HW	Hardware
IBSS	Independent Basic Service Set
ICU	Interrupt Control Unit
IPA	IsoPropyl Alcohol

Table 76. Abbreviations *...continued*

Acronym	Description
IPU	Instruction Pre-fetch Unit
IRQ	Interrupt ReQuest
ISI	InterSymbol Interference
ISM	Industrial, Scientific and Medical
LNA	Low Noise Amplifier
LSB	Least Significant Bit
MAC	Medium Access Control
MIC	Message Integrity Code
MIPS	Million Instructions Per Second
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
NAV	Network Allocation Vector
NIC	Network Interface Card
OSP	Organic Surface Protection
PCB	Printed-Circuit Board
PDA	Personal Digital Assistant
PER	Packet Error Rate
PHY	Physical layer
PHYRX	Physical layer receiver
PHYTX	Physical layer transmitter
PLCP	Physical Layer Convergence Procedure
PSDU	PLCP Service Data Unit
PTA	Packet Traffic Arbitration
QoS	Quality of Service
QPSK	Quadrature Phase Shift Keying
RFIF	RF InterFace
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances
ROM	Read Only Memory
RSSI	Received-Signal Strength Indicator
RTS	Request To Send
RX	Receiver
SCU	System Configuration Unit
SDIO	Secure Digital Input/Output
SDRAM	Static Dynamic Random Access Memory
SIFS	Short InterFrame Space
SPI	Serial Peripheral Interface
TBTT	Target Beacon Transmission Time
TKIP	Temporary Key Integrity Protocol
TSF	Timer Synchronization Function
TX	Transmitter

Table 76. Abbreviations *...continued*

Acronym	Description
TXOP	Transmission Opportunity
UART	Universal Asynchronous Receiver Transmitter
VCO	Voltage-Controlled Oscillator
VoIP	Voice over Internet Protocol
VPB	VLSI Peripheral Bus
WDT	WatchDog Timer
WEP	Wired Equivalent Privacy
WinCE	Windows Compact Edition
WLAN	Wireless Local Area Network
WMM	Wi-Fi Multi Media
WPA	Wi-Fi Protected Access

20. Revision history

Table 77. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BGW200EG_1	20070718	Product data sheet	-	-

21. Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

21.2 Definitions

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