+3 V, Voltage Monitoring µP Supervisory Circuits

ADM706P/R/S/T, ADM708R/S/T

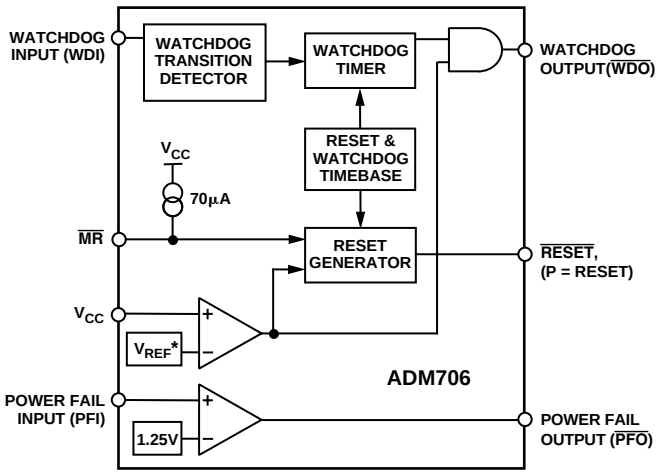
FEATURES

Precision Supply-Voltage Monitor
+2.63 V (ADM706P/R, ADM708R)
+2.93 V (ADM706S, ADM708S)
+3.08 V (ADM706T, ADM708T)
100 µA Quiescent Current
200 ms Reset Pulsewidth
Debounced Manual Reset Input ($\overline{MR}$)
Independent Watchdog Timer—1.6 sec Timeout (ADM706x)
Reset Output
Active High (ADM706P)
Active Low (ADM706R/S/T)
Both Active High and Active Low (ADM708R/S/T)
Voltage Monitor for Power-Fail or Low Battery Warning
Guaranteed $\overline{RESET}$ Valid with V_{CC} = 1 V
Superior Upgrade for MAX706P/R/S/T, MAX708R/S/T

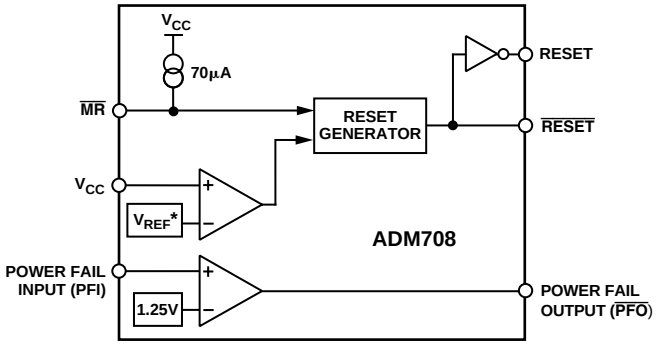
APPLICATIONS

Microprocessor Systems
Computers
Controllers
Intelligent Instruments
Critical µP Monitoring
Automotive Systems
Battery Operated Systems
Portable Instruments

FUNCTIONAL BLOCK DIAGRAMS



*VOLTAGE REFERENCE = 2.63V (P/R), 2.93V (S), 3.08V (T)



*VOLTAGE REFERENCE = 2.63V (R), 2.93V (S), 3.08V (T)

GENERAL DESCRIPTION

The ADM706P/R/S/T and the ADM708R/S/T microprocessor supervisory circuits are suitable for monitoring either 3 V or 3.3 V power supplies.

The ADM706P/R/S/T provide the following functions:

1. Power-supply monitoring circuitry which generates a Reset output during power-up, power-down and brownout conditions. The reset output remains operational with V_{CC} as low as 1 V.
2. Independent watchdog monitoring circuitry which is activated if the watchdog input has not been toggled within 1.6 seconds.
3. A 1.25 V threshold detector for power fail warning, low battery detection, or to monitor an additional power supply.
4. An active low debounced manual reset input ($\overline{MR}$).

The ADM706R, ADM706S, ADM706T are identical except for the reset threshold monitor levels which are 2.63 V, 2.93 V, and 3.08 V respectively. The ADM706P is identical to the ADM706R in that the reset threshold is 2.63 V. It differs only in that it has an active high reset output.

The ADM708R/S/T provide the same functionality as the ADM706R/S/T and only differ in that:

1. A watchdog timer function is not available.
2. An active high reset output (RESET) in addition to the active low ($\overline{RESET}$) output is available.

All parts are available in 8-lead DIP and narrow SOIC packages.

REV. A

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ADM706P/R/S/T, ADM708R/S/T–SPECIFICATIONS (V_{CC} = 2.70 V to 5.5 V (ADM70_P/R), V_{CC} = 3.00 V to 5.5 V (ADM70_S), V_{CC} = 3.15 V to 5.5 V (ADM70_T), T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
V_{CC} Operating Voltage Range	1.0		5.5	V	
Supply Current		100	200	µA	V_{CC} < 3.6 V
		150	350	µA	V_{CC} < 5.5 V
Reset Threshold (V_{RST})	2.55	2.63	2.70	V	ADM70_P/R
	2.85	2.93	3.00	V	ADM70_S
	3.00	3.08	3.15	V	ADM70_T
Reset Threshold Hysteresis		20		mV	
Reset Pulsewidth	160	200	280	ms	ADM70_P/R, V_{CC} = 3 V
	160	200	280	ms	ADM70_S/T, V_{CC} = 3.3 V
		200		ms	V_{CC} = 5.0 V
$\overline{\text{RESET}}$ Output Voltage					ADM70_R/S/T
V_{OH}	0.8 × V_{CC}			V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SOURCE} = 500 µA
V_{OL}			0.3	V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SINK} = 1.2 mA
V_{OH}	V_{CC}–1.5 V			V	4.5 V < V_{CC} < 5.5 V, I_{SOURCE} = 800 µA
V_{OL}			0.4	V	4.5 V < V_{CC} < 5.5 V, I_{SINK} = 3.2 mA
V_{OL}			0.3	V	V_{CC} = 1 V, I_{SINK} = 100 µA
RESET Output Voltage					ADM706P
V_{OH}	V_{CC}–0.6 V			V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SOURCE} = 215 µA
V_{OL}			0.3	V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SINK} = 1.2 mA
V_{OH}	V_{CC}–1.5 V			V	4.5 V < V_{CC} < 5.5 V, I_{SOURCE} = 800 µA
V_{OL}			0.4	V	4.5 V < V_{CC} < 5.5 V, I_{SINK} = 3.2 mA
RESET Output Voltage					ADM708_
V_{OH}	0.8 × V_{CC}			V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SOURCE} = 500 µA
V_{OL}			0.3	V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SINK} = 500 µA
V_{OH}	V_{CC}–1.5 V			V	4.5 V < V_{CC} < 5.5 V, I_{SOURCE} = 800 µA
V_{OL}			0.4	V	4.5 V < V_{CC} < 5.5 V, I_{SINK} = 1.2 mA
Watchdog Timeout Period	1.00	1.60	2.25	sec	ADM70_P/R; V_{CC} = 3 V. ADM70_S/T, V_{CC} = 3.3 V
WDI Pulsewidth					V_{IL} = 0.4 V, V_{IH} = (V_{CC}) × (0.8)
	100			ns	V_{RST} (max) < V_{CC} < 3.6 V
	50			ns	4.5 V < V_{CC} < 5.5 V
WDI Input Threshold					ADM706_
V_{IL}			0.6	V	V_{RST} (max) < V_{CC} < 3.6 V
V_{IH}	0.7 × V_{CC}			V	V_{RST} (max) < V_{CC} < 3.6 V
V_{IL}			0.8	V	V_{CC} = 5.0 V
V_{IH}	3.5			V	V_{CC} = 5.0 V
WDI Input Current	–1.0	0.02	1.0	µA	WDI = 0 V or V_{CC}
$\overline{\text{WDO}}$ Output Voltage					
V_{OH}	0.8 × V_{CC}			V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SOURCE} = 500 µA
V_{OL}			0.3	V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SINK} = 500 µA
V_{OH}	V_{CC}–1.5 V			V	4.5 V < V_{CC} < 5.5 V, I_{SOURCE} = 800 µA
V_{OL}			0.4	V	4.5 V < V_{CC} < 5.5 V, I_{SINK} = 1.2 mA
$\overline{\text{MR}}$ Pull Up Current					$\overline{\text{MR}}$ = 0 V
	25	70	250	µA	V_{RST} (max) < V_{CC} < 3.6 V
	100	250	600	µA	4.5 V < V_{CC} < 5.5 V
$\overline{\text{MR}}$ Pulsewidth					
	500			ns	V_{RST} (max) < V_{CC} < 3.6 V
	150			ns	4.5 V < V_{CC} < 5.5 V
$\overline{\text{MR}}$ Input Threshold					
V_{IL}			0.6	V	V_{RST} (max) < V_{CC} < 3.6 V
V_{IH}	0.7 × V_{CC}			V	V_{RST} (max) < V_{CC} < 3.6 V
V_{IL}			0.8	V	4.5 V < V_{CC} < 5.5 V
V_{IH}	2.0			V	4.5 V < V_{CC} < 5.5 V

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
$\overline{MR}$ to Reset Output Delay			750 250	ns ns	V_{RST} (max) < V_{CC} < 3.6 V 4.5 V < V_{CC} < 5.5 V
PFI Input Threshold	1.2	1.25	1.3	V	ADM70_P/R; V_{CC} = 3 V. ADM70_S/T, V_{CC} = 3.3 V, PFI falling
PFI Input Current	–25	0.01	25	nA	
$\overline{PFO}$ Output Voltage					
V_{OH}	0.8 × V_{CC}			V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SOURCE} = 500 µA
V_{OL}			0.3	V	V_{RST} (max) < V_{CC} < 3.6 V, I_{SINK} = 1.2 mA
V_{OH}	V_{CC}–1.5 V			V	4.5 V < V_{CC} < 5.5 V, I_{SOURCE} = 800 µA
V_{OL}			0.4	V	4.5 V < V_{CC} < 5.5 V, I_{SINK} = 3.2 mA

ORDERING GUIDE

Model	Temperature Range	Package Options
ADM706PAN	–40°C to +85°C	N-8
ADM706PAR	–40°C to +85°C	SO-8
ADM706RAN	–40°C to +85°C	N-8
ADM706RAR	–40°C to +85°C	SO-8
ADM706SAN	–40°C to +85°C	N-8
ADM706SAR	–40°C to +85°C	SO-8
ADM706TAN	–40°C to +85°C	N-8
ADM706TAR	–40°C to +85°C	SO-8
ADM708RAN	–40°C to +85°C	N-8
ADM708RAR	–40°C to +85°C	SO-8
ADM708SAN	–40°C to +85°C	N-8
ADM708SAR	–40°C to +85°C	SO-8
ADM708TAN	–40°C to +85°C	N-8
ADM708TAR	–40°C to +85°C	SO-8

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

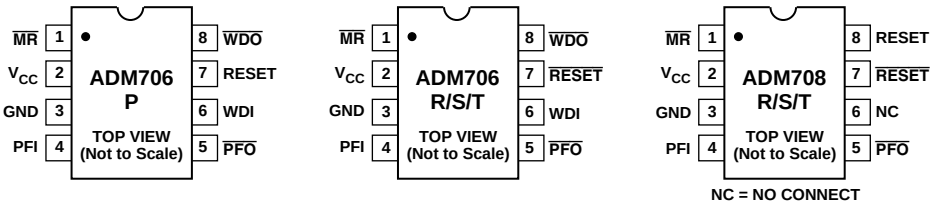
V_{CC} . . . . . –0.3 V to +6 V
All Other Inputs . . . . . –0.3 V to V_{CC} + 0.3 V
Input Current
V_{CC} . . . . . 20 mA
GND . . . . . 20 mA
Digital Output Current . . . . . 20 mA
Power Dissipation, N-8 DIP . . . . . 727 mW
θ_{JA} Thermal Impedance . . . . . 135°C/W
Power Dissipation, SO-8 SOIC . . . . . 470 mW
θ_{JA} Thermal Impedance . . . . . 110°C/W
Operating Temperature Range
Industrial (A Version) . . . . . –40°C to +85°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Vapor Phase (60 secs) . . . . . +215°C
Infrared (15 secs) . . . . . +220°C
Storage Temperature Range . . . . . –65°C to +150°C
ESD Rating . . . . . >5 kV

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

PIN FUNCTION DESCRIPTIONS

Mnemonic	Pin No. ADM706	Pin No. ADM708	Function
$\overline{MR}$	1	1	Manual Reset Input. When taken below 0.6 V a RESET is generated. $\overline{MR}$ can be driven from TTL, CMOS logic or from a manual reset switch as it is internally debounced. An internal 70 μA pull-up current holds the input high when floating.
V_{CC}	2	2	Power Supply Input.
GND	3	3	0 V. Ground reference for all signals.
PFI	4	4	Power Fail Input. PFI is the noninverting input to the Power Fail Comparator. When PFI is less than 1.25 V, PFO goes low. If unused, PFI should be connected to GND.
$\overline{PFO}$	5	5	Power Fail Output. $\overline{PFO}$ is the output from the Power Fail Comparator. It goes low when PFI is less than 1.25 V.
WDI	6	N/A	Watchdog Input. WDI is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, the watchdog output $\overline{WDO}$ goes low. The timer resets with each transition at the WDI input. Either a high-to-low or a low-to-high transition will clear the counter. The internal timer is also cleared whenever reset is asserted. The Watchdog Timer is disabled when WDI is left floating or connected to a three-state buffer.
NC	N/A	6	No Connect.
$\overline{RESET}$	7 (R/S/T Only)	7	Logic Output. $\overline{RESET}$ goes low for 200 ms when triggered. It can be triggered either by V_{CC} being below the reset threshold or by a low signal on the manual reset ($\overline{MR}$) input. $\overline{RESET}$ will remain low whenever V_{CC} is below the reset threshold. It remains low for 200 ms after V_{CC} goes above the reset threshold or $\overline{MR}$ goes from low to high. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
RESET	7 (P Only)	8	Logic Output. RESET is an active high output suitable for systems which use active high RESET logic. It is the inverse of $\overline{RESET}$.
$\overline{WDO}$	8	N/A	Logic Output. The Watchdog Output, $\overline{WDO}$, goes low if the internal watchdog timer times out as a result of inactivity on the WDI input. It remains low until the watchdog timer is cleared. $\overline{WDO}$ also goes low during low line conditions. Whenever V_{CC} is below the reset threshold, $\overline{WDO}$ remains low. As soon as V_{CC} goes above the reset threshold, $\overline{WDO}$ goes high immediately.

PIN CONFIGURATIONS



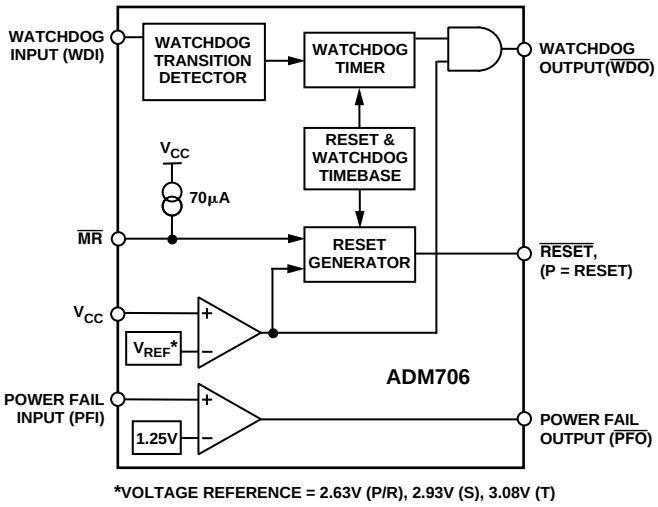


Figure 1. ADM706 Functional Block Diagram

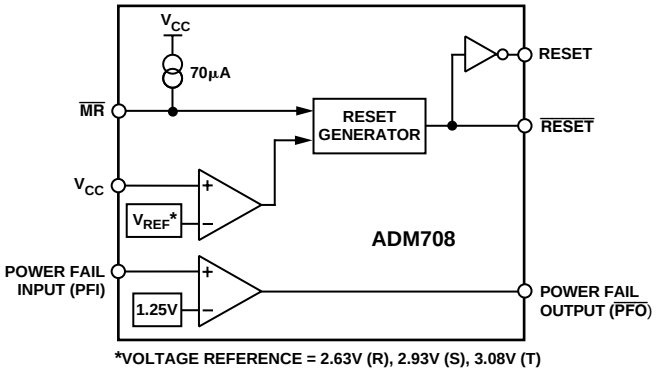


Figure 2. ADM708 Functional Block Diagram

CIRCUIT INFORMATION

Power Fail Reset

The reset output provides a reset ($\overline{\text{RESET}}$ or RESET) output signal to the Microprocessor whenever the V_{CC} input is below the reset threshold. The actual reset threshold voltage is dependent on whether a P/R, S, or T suffix device is used. An internal timer holds the reset output active for 200 ms after the voltage on V_{CC} rises above the threshold. This is intended as a power-on reset signal for the microprocessor. It allows time for both the power supply and the microprocessor to stabilize after power-up. If a power supply brownout or interruption occurs, the reset line is similarly activated and remains active for 200 ms after the supply recovers. If another interruption occurs during an active reset period, then the reset timeout period continues for an additional 200 ms.

The reset output is guaranteed to remain valid with V_{CC} as low as 1 V. This ensures that the microprocessor is held in a stable shutdown condition as the power supply starts up.

The ADM706P provides an active high reset (RESET) signal; the ADM706R/S/T provides an active low ($\overline{\text{RESET}}$) signal; while the ADM708R/S/T provides both RESET and $\overline{\text{RESET}}$.

Manual Reset

The manual reset input ($\overline{\text{MR}}$) allows other reset sources such as a manual reset switch to generate a processor reset. The input is effectively debounced by the timeout period (200 ms typical). The $\overline{\text{MR}}$ input is TTL/CMOS compatible so it may also be driven by any logic reset output. If unused, the $\overline{\text{MR}}$ input may be tied high or left floating.

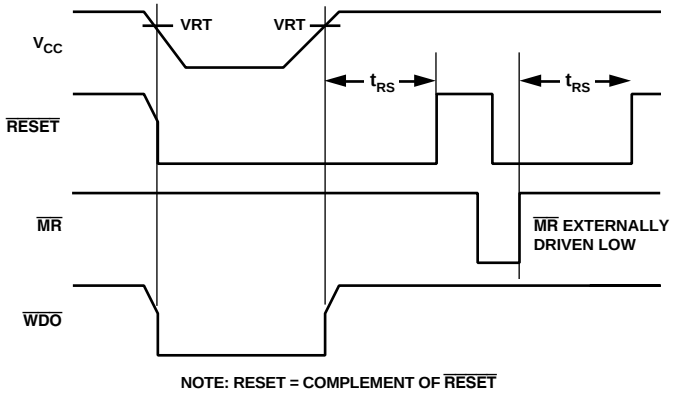


Figure 3. $\overline{\text{RESET}}$, $\overline{\text{MR}}$ and $\overline{\text{WDO}}$ Timing

Watchdog Timer (ADM706)

The watchdog timer circuit may be used to monitor the activity of the microprocessor in order to check that it is not stalled in an indefinite loop. An output line on the processor is used to toggle the Watchdog Input (WDI) line. If this line is not toggled within the timeout period (1.6 sec), the watchdog output ($\overline{\text{WDO}}$) is driven low. The $\overline{\text{WDO}}$ output may be connected to a nonmaskable interrupt (NMI) on the processor. Therefore, if the watchdog timer times out, an interrupt is generated. The interrupt service routine should then be used to rectify the problem.

The watchdog timer is cleared by either a high-to-low or by a low-to-high transition on WDI. Pulses as narrow as 50 ns are detected. The timer is also cleared by RESET/$\overline{\text{RESET}}$ going active. Therefore the watchdog timeout period begins after reset goes inactive.

When V_{CC} falls below the reset threshold, $\overline{\text{WDO}}$ is forced low whether or not the watchdog timer has timed out. Normally this would generate an interrupt but it is overridden by RESET/$\overline{\text{RESET}}$ going active.

The watchdog monitor can be deactivated by floating the Watchdog Input (WDI). The $\overline{\text{WDO}}$ output can now be used as a low line output since it will only go low when V_{CC} falls below the reset threshold.

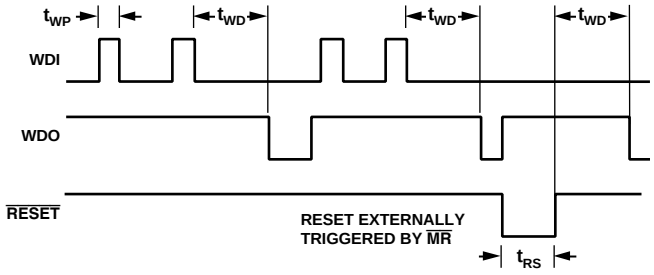


Figure 4. Watchdog Timing

Power-Fail Comparator

The power-fail comparator is an independent comparator which may be used to monitor the input power supply. The comparator's inverting input is internally connected to a 1.25 V reference voltage. The noninverting input is available at the PFI input. This input may be used to monitor the input power supply via a resistive divider network. When the voltage on the PFI input drops below 1.25 V, the comparator output ($\overline{PFO}$) goes low indicating a power failure. For early warning of power failure the comparator may be used to monitor the preregulator input simply by choosing an appropriate resistive divider network. The $\overline{PFO}$ output can be used to interrupt the processor so that a shutdown procedure is implemented before the power is lost.

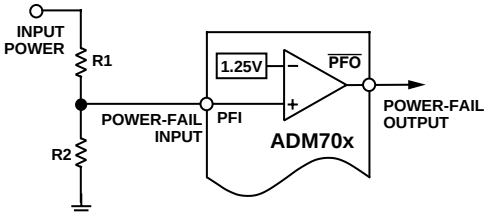


Figure 5. Power-Fail Comparator

Adding Hysteresis to the Power-Fail Comparator

For increased noise immunity, hysteresis may be added to the power-fail comparator. Since the comparator circuit is noninverting, hysteresis can be added simply by connecting a resistor between the $\overline{PFO}$ output and the PFI input as shown in Figure 6. When $\overline{PFO}$ is low, resistor R3 sinks current from the summing junction at the PFI pin. When $\overline{PFO}$ is high, resistor R3 sources current into the PFI summing junction. This results in differing trip levels for the comparator. Further noise immunity may be achieved by connecting a capacitor between PFI and GND.

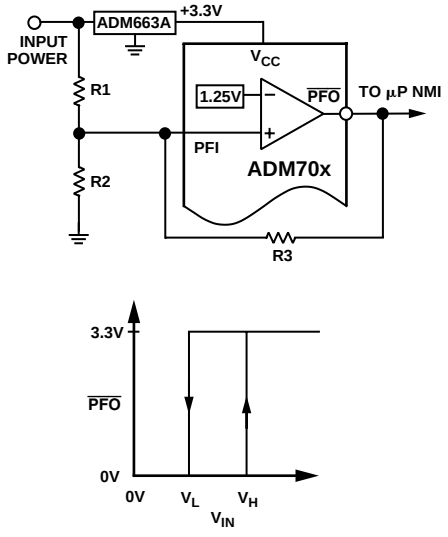


Figure 6. Adding Hysteresis to the Power-Fail Comparator

$$V_H = 1.25\left[1+\left(\frac{R2+R3}{R2\times R3}\right)R1\right]$$

$$V_L = 1.25 + R1\left(\frac{1.25}{R2} - \frac{V_{CC}-1.25}{R3}\right)$$

$$V_{MID}\ 1.25\left(\frac{R1+R2}{R2}\right)$$

Valid RESET Below 1 V V_{CC}

The ADM70x family of products are guaranteed to provide a valid reset level with V_{CC} as low as 1 V. Please refer to the Typical Performance Characteristics. As V_{CC} drops below 1 V, the internal transistor will not have sufficient drive to hold it ON so the voltage on $\overline{RESET}$ will no longer be held at 0 V. A pull-down resistor as shown in Figure 7 may be connected externally to hold the line low if it is required.

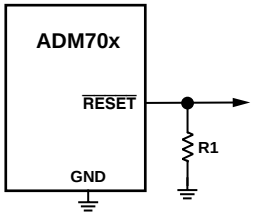


Figure 7. $\overline{RESET}$ Valid Below 1 V

Typical Performance Characteristics

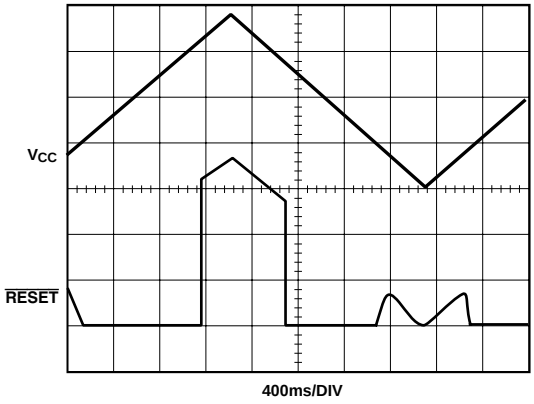


Figure 8. ADM706/ADM708 $\overline{RESET}$ Output Voltage vs. Supply Voltage

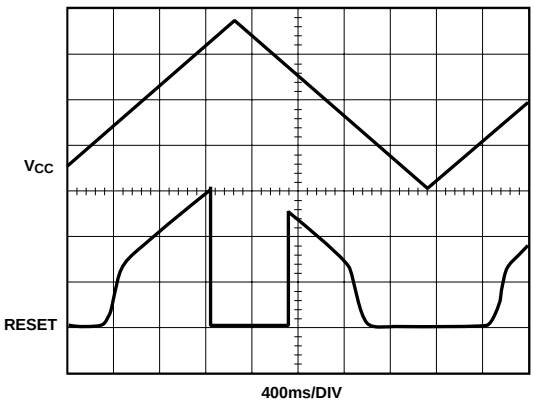


Figure 9. RESET Output Voltage vs. Supply Voltage

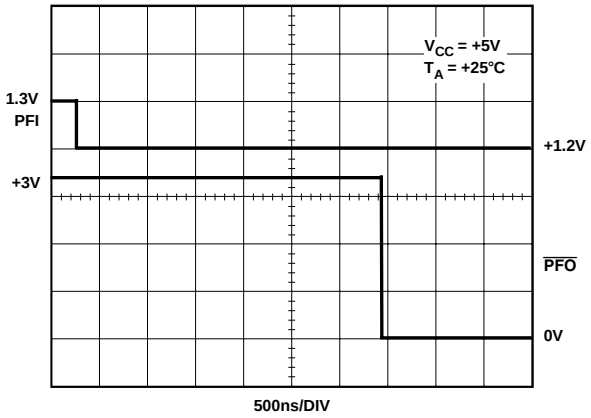


Figure 10. PFI Assertion Response Time

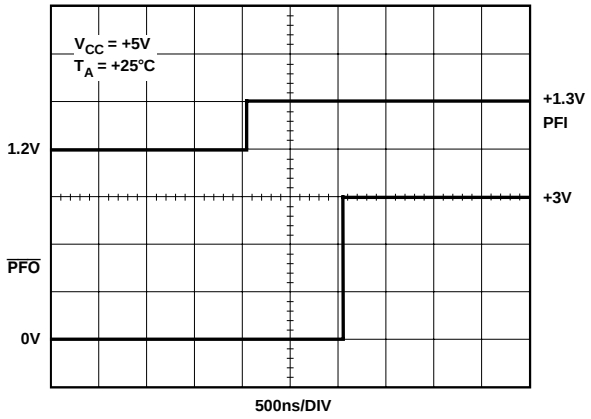


Figure 11. PFI Deassertion Response Time

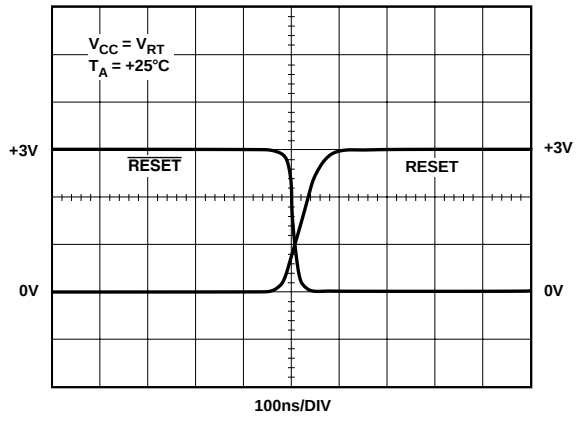


Figure 12. $\overline{RESET}$, RESET Assertion

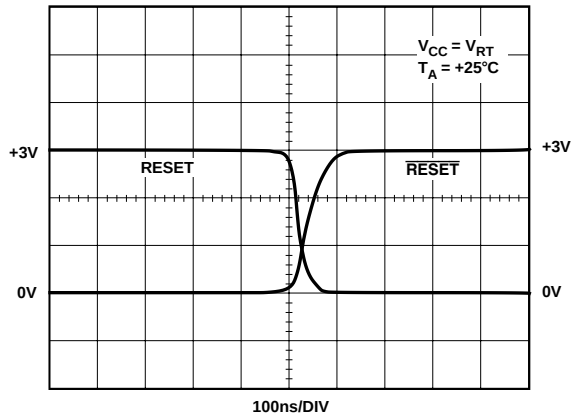


Figure 13. $\overline{RESET}$, RESET Deassertion

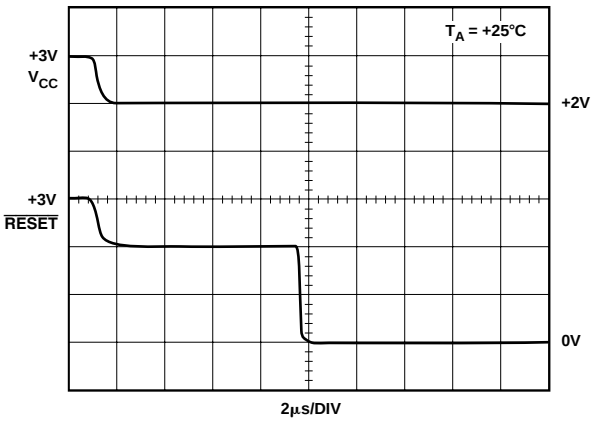


Figure 14. ADM706/ADM708 $\overline{RESET}$ Response Time

APPLICATIONS

A typical operating Circuit is shown in Figure 15. The unregulated dc input supply is monitored using the PFI input via the resistive divider network. Resistors R1 and R2 should be selected such that when the supply voltage drops below the desired level (e.g., 5 V) the voltage on PFI drops below the 1.25 V threshold thereby generating an interrupt to the µP. Monitoring the preregulator input gives additional time to execute an orderly shutdown procedure before power is lost.

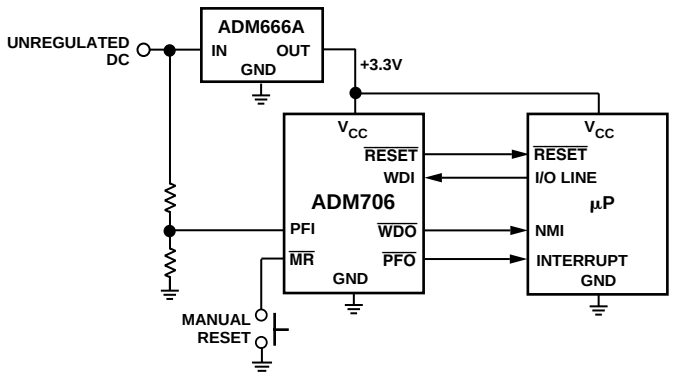


Figure 15. Typical Application Circuit

Microprocessor activity is monitored using the WDI input. This is driven using an output line from the processor. The software routines should toggle this line at least once every 1.6 seconds. If a problem occurs and this line is not toggled, then WDO goes low and a nonmaskable interrupt is generated. This interrupt routine may be used to clear the problem.

If, in the event of inactivity on the WDI line, a system reset is required, then the $\overline{\text{WDO}}$ output should be connected to the input as shown in Figure 16.

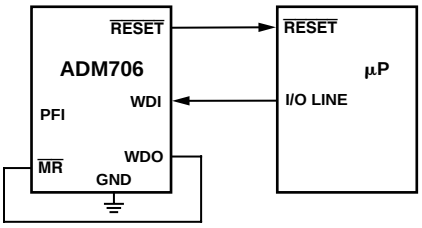


Figure 16. $\overline{\text{RESET}}$ from WDO

Monitoring Additional Supply Levels

It is possible to use the power-fail comparator to monitor a second supply as shown in Figure 17. The two sensing resistors R1 and R2 are selected such that the voltage on PFI drops below 1.25 V at the minimum acceptable input supply. The $\overline{\text{PFO}}$ output may be connected to the $\overline{\text{MR}}$ input so that a RESET is generated when the supply drops out of tolerance. In this case if either supply drops out of tolerance, a RESET will be generated.

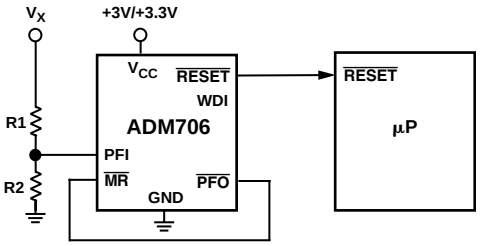


Figure 17. Monitoring 3 V/3.3 V and an Additional Supply, V_X

μPs with Bidirectional $\overline{\text{RESET}}$

In order to prevent contention for microprocessors with a bidirectional reset line, a current limiting resistor should be inserted between the ADM70x $\overline{\text{RESET}}$ output pin and the μP reset pin. This will limit the current to a safe level if there are conflicting output reset levels. A suitable resistor value is 4.7 kΩ. If the reset output is required for other uses, then it should be buffered as shown in Figure 18.

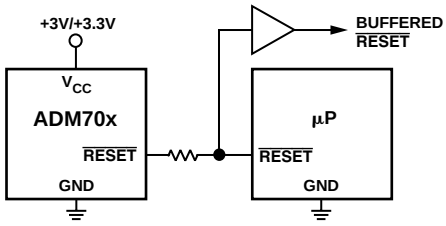


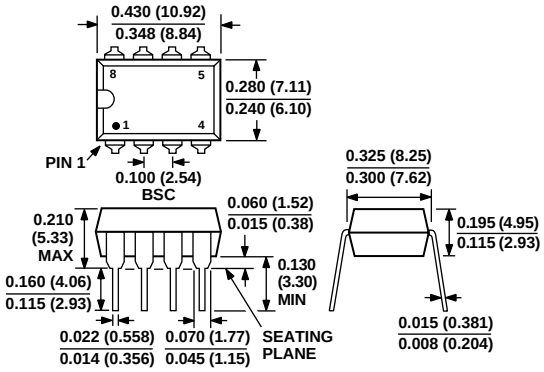
Figure 18. Bidirectional I-O RESET

C1998a–0–12/99

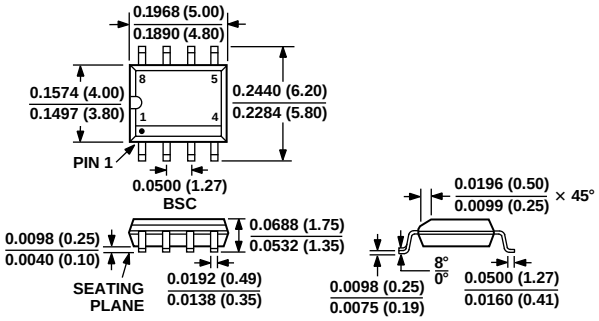
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP
(N-8)



8-Lead SOIC
(SO-8)



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