

**FEATURES**

**44 V Supply Maximum Ratings**  
**V<sub>SS</sub> to V<sub>DD</sub> Analog Signal Range**  
**Low On Resistance (< 35 Ω)**  
**Ultralow Power Dissipation (< 35 μW)**  
**Fast Transition Time (160 ns max)**  
**Break-Before-Make Switching Action**  
**Plug-In Replacement for DG419**

**APPLICATIONS**

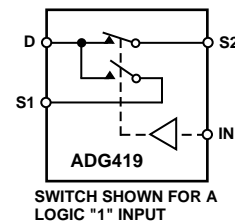
**Precision Test Equipment**  
**Precision Instrumentation**  
**Battery Powered Systems**  
**Sample Hold Systems**

**GENERAL DESCRIPTION**

The ADG419 is a monolithic CMOS SPDT switch. This switch is designed on an enhanced LC<sup>2</sup>MOS process that provides low power dissipation yet gives high switching speed, low on resistance and low leakage currents.

The on resistance profile of the ADG419 is very flat over the full analog input range, ensuring excellent linearity and low distortion. The part also exhibits high switching speed and high signal bandwidth. CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery powered instruments.

Each switch of the ADG419 conducts equally well in both directions when ON and has an input signal range that extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. The ADG419 exhibits break-before-make switching action.

**FUNCTIONAL BLOCK DIAGRAM****PRODUCT HIGHLIGHTS**

1. **Extended Signal Range**  
The ADG419 is fabricated on an enhanced LC<sup>2</sup>MOS process, giving an increased signal range that extends to the supply rails.
2. **Ultralow Power Dissipation**
3. **Low R<sub>ON</sub>**
4. **Single Supply Operation**  
For applications where the analog signal is unipolar, the ADG419 can be operated from a single rail power supply. The part is fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

**REV. A**

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# ADG419—SPECIFICATIONS<sup>1</sup>

**Dual Supply** ( $V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $V_L = +5\text{ V} \pm 10\%$ , **GND = 0 V**, unless otherwise noted)

Parameter	B Version -40°C to +85°C		T Version -55°C to +125°C		Units	Test Conditions/Comments
	+25°C		+25°C	+125°C		
<b>ANALOG SWITCH</b>						
Analog Signal Range		$V_{SS}$ to $V_{DD}$		$V_{SS}$ to $V_{DD}$	V	
$R_{ON}$	25 35	45	25 35	45	$\Omega$ typ $\Omega$ max	$V_D = \pm 12.5\text{ V}$ , $I_S = -10\text{ mA}$ $V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$
<b>LEAKAGE CURRENTS</b>						
Source OFF Leakage $I_S$ (OFF)	$\pm 0.1$ $\pm 0.25$	$\pm 5$	$\pm 0.1$ $\pm 0.25$	$\pm 15$	nA typ nA max	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ $V_D = \pm 15.5\text{ V}$ , $V_S = \mp 15.5\text{ V}$ ; Test Circuit 2
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.1$ $\pm 0.75$	$\pm 5$	$\pm 0.1$ $\pm 0.75$	$\pm 30$	nA typ nA max	$V_D = \pm 15.5\text{ V}$ , $V_S = \mp 15.5\text{ V}$ ; Test Circuit 2
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.4$ $\pm 0.75$	$\pm 5$	$\pm 0.4$ $\pm 0.75$	$\pm 30$	nA typ nA max	$V_S = V_D = \pm 15.5\text{ V}$ ; Test Circuit 3
<b>DIGITAL INPUTS</b>						
Input High Voltage, $V_{INH}$		2.4		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8		0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$		$\pm 0.005$ $\pm 0.5$		$\pm 0.005$ $\pm 0.5$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>						
$t_{TRANSITION}$	160	200	145	200	ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1} = \pm 10\text{ V}$ , $V_{S2} = \mp 10\text{ V}$ ; Test Circuit 4
Break-Before-Make Time Delay, $t_D$	30 5		30 5		ns typ ns min	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1} = V_{S2} = \pm 10\text{ V}$ ; Test Circuit 5
OFF Isolation	80		80		dB typ	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ; Test Circuit 6
Channel-to-Channel Crosstalk	90		70		dB typ	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ; Test Circuit 7
$C_S$ (OFF)	6		6		pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	55		55		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>						
$I_{DD}$	0.0001 1	2.5	0.0001 1	2.5	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ $V_{IN} = 0\text{ V}$ or $5\text{ V}$
$I_{SS}$	0.0001 1	2.5	0.0001 1	2.5	$\mu\text{A}$ typ $\mu\text{A}$ max	
$I_L$	0.0001 1	2.5	0.0001 1	2.5	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_L = +5.5\text{ V}$

## NOTES

<sup>1</sup>Temperature ranges are as follows: B Version: -40°C to +85°C; T Version: -55°C to +125°C.

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

## Single Supply ( $V_{DD} = +12\text{ V} \pm 10\%$ , $V_{SS} = 0\text{ V}$ , $V_L = +5\text{ V} \pm 10\%$ , $GND = 0\text{ V}$ , unless otherwise noted)

Parameter	B Version		T Version		Units	Test Conditions/Comments
	+25°C	-40°C to +85°C	+25°C	-55°C to +125°C		
<b>ANALOG SWITCH</b>						
Analog Signal Range		0 to $V_{DD}$		0 to $V_{DD}$	V	
$R_{ON}$	40	60	40	70	$\Omega$ typ $\Omega$ max	$V_D = +3\text{ V}$ , $+8.5\text{ V}$ , $I_S = -10\text{ mA}$ $V_{DD} = +10.8\text{ V}$
<b>LEAKAGE CURRENT</b>						$V_{DD} = +13.2\text{ V}$
Source OFF Leakage $I_S$ (OFF)	$\pm 0.1$ $\pm 0.25$	$\pm 5$	$\pm 0.1$ $\pm 0.25$	$\pm 15$	nA typ nA max	$V_D = 12.2\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/12.2\text{ V}$ ; Test Circuit 2
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.1$ $\pm 0.75$	$\pm 5$	$\pm 0.1$ $\pm 0.75$	$\pm 30$	nA typ nA max	$V_D = 12.2\text{ V}/1\text{ V}$ , $V_S = 1\text{ V}/12.2\text{ V}$ ; Test Circuit 2
Channel ON Leakage $I_D, I_S$ (ON)	$\pm 0.4$ $\pm 0.75$	$\pm 5$	$\pm 0.4$ $\pm 0.75$	$\pm 30$	nA typ nA max	$V_S = V_D = 12.2\text{ V}/1\text{ V}$ ; Test Circuit 3
<b>DIGITAL INPUTS</b>						
Input High Voltage, $V_{INH}$		2.4		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8		0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$		$\pm 0.005$ $\pm 0.5$		$\pm 0.005$ $\pm 0.5$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>						
$t_{TRANSITION}$	180	250	170	250	ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1} = 0\text{ V}/8\text{ V}$ , $V_{S2} = 8\text{ V}/0\text{ V}$ ; Test Circuit 4
Break-Before-Make Time Delay, $t_D$	60		60		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1} = V_{S2} = +8\text{ V}$ ; Test Circuit 5
OFF Isolation	80		80		dB typ	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ; Test Circuit 6
Channel-to-Channel Crosstalk	90		70		dB typ	$R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ ; Test Circuit 7
$C_S$ (OFF)	13		13		pF typ	$f = 1\text{ MHz}$
$C_D, C_S$ (ON)	65		65		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>						$V_{DD} = +13.2\text{ V}$ $V_{IN} = 0\text{ V}$ or $5\text{ V}$
$I_{DD}$	0.0001		0.0001		$\mu\text{A}$ typ	
	1	2.5	1	2.5	$\mu\text{A}$ max	
$I_L$	0.0001		0.0001		$\mu\text{A}$ typ	$V_L = +5.5\text{ V}$
	1	2.5	1	2.5	$\mu\text{A}$ max	

### NOTES

<sup>1</sup>Temperature ranges are as follows: B Version:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ ; T Version:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

**Table I. Truth Table**

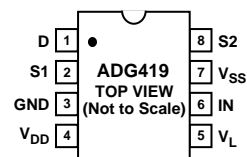
Logic	Switch 1	Switch 2
0	ON	OFF
1	OFF	ON

### ORDERING GUIDE

Model	Temperature Ranges	Package Options*
ADG419BN	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	N-8
ADG419BR	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	SO-8
ADG419BRM	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	RM-8
ADG419TQ	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	Q-8

\*N = Plastic DIP, Q = Cerdip, RM =  $\mu\text{SOIC}$ , SO = 0.15" Small Outline IC (SOIC).

### PIN CONFIGURATION DIP/SOIC/ $\mu\text{SOIC}$



# ADG419

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>DD</sub> to V <sub>SS</sub>	+44 V
V <sub>DD</sub> to GND	-0.3 V to +25 V
V <sub>SS</sub> to GND	+0.3 V to -25 V
V <sub>L</sub> to GND	-0.3 V to V <sub>DD</sub> + 0.3 V
Analog, Digital Inputs <sup>2</sup>	V <sub>SS</sub> - 2 V to V <sub>DD</sub> + 2 V or 30 mA, Whichever Occurs First
Continuous Current, S or D	30 mA
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Extended (T Version)	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Cerdip Package, Power Dissipation	600 mW
θ <sub>JA</sub> , Thermal Impedance	110°C/W
Lead Temperature, Soldering (10 sec)	+300°C

Plastic Package, Power Dissipation	400 mW
θ <sub>JA</sub> , Thermal Impedance	100°C/W
Lead Temperature, Soldering (10 sec)	+260°C
SOIC Package, Power Dissipation	400 mW
θ <sub>JA</sub> , Thermal Impedance	155°C/W
μSOIC Package, Power Dissipation	315 mW
θ <sub>JA</sub> , Thermal Impedance	205°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

## NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

<sup>2</sup>Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG419 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## TERMINOLOGY

V <sub>DD</sub>	Most positive power supply potential.
V <sub>SS</sub>	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.
V <sub>L</sub>	Logic power supply (+5 V).
GND	Ground (0 V) reference.
S	Source terminal. May be an input or an output.
D	Drain terminal. May be an input or an output.
IN	Logic control input.
R <sub>ON</sub>	Ohmic resistance between D and S.
I <sub>S</sub> (OFF)	Source leakage current with the switch "OFF."
I <sub>D</sub> (OFF)	Drain leakage current with the switch "OFF."
I <sub>D</sub> , I <sub>S</sub> (ON)	Channel leakage current with the switch "ON."
V <sub>D</sub> (V <sub>S</sub> )	Analog voltage on terminals D, S.
C <sub>S</sub> (OFF)	"OFF" switch source capacitance.

C <sub>D</sub> , C <sub>S</sub> (ON)	"ON" switch capacitance.
t <sub>TRANSITION</sub>	Delay time between the 50% and 90% points of the digital inputs and the switch "ON" condition when switching from one address state to another.
t <sub>D</sub>	"OFF" time or "ON" time measured between the 90% points of both switches when switching from one address state to the other.
V <sub>INL</sub>	Maximum input voltage for logic "0."
V <sub>INH</sub>	Minimum input voltage for logic "1."
I <sub>INL</sub> (I <sub>INH</sub> )	Input current of the digital input.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" channel.
I <sub>DD</sub>	Positive supply current.
I <sub>SS</sub>	Negative supply current.

# Typical Performance Characteristics—ADG419

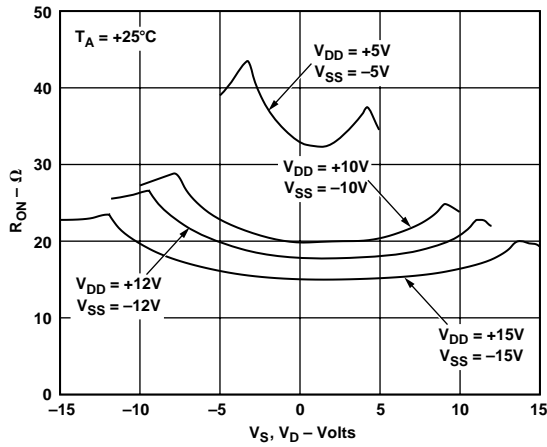


Figure 1.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ): Dual Supply Voltage

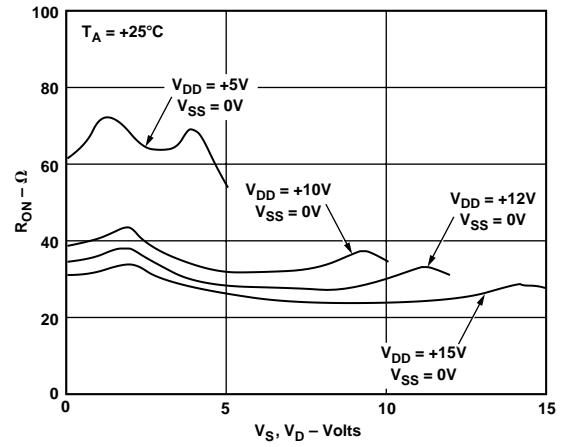


Figure 4.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ): Single Supply Voltage

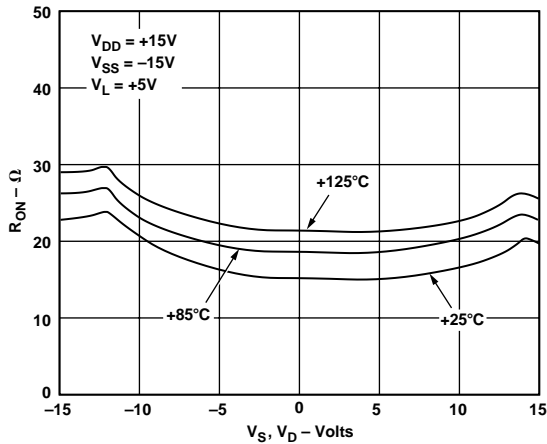


Figure 2.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures

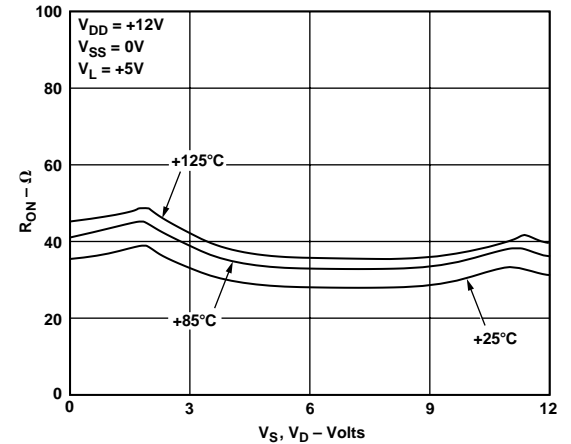


Figure 5.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures

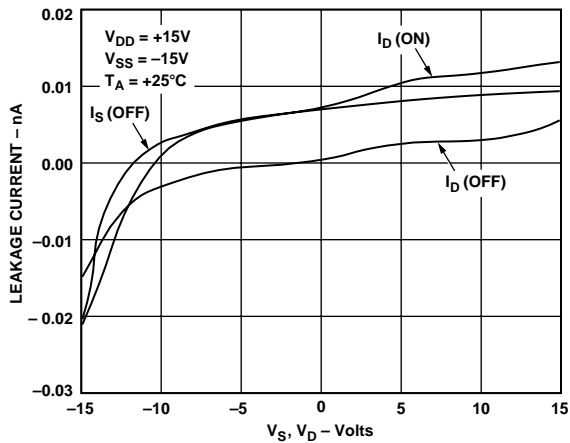


Figure 3. Leakage Currents as a Function of  $V_S$  ( $V_D$ )

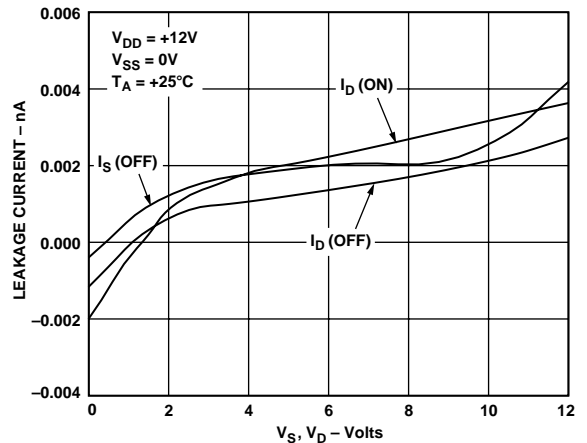


Figure 6. Leakage Currents as a Function of  $V_S$  ( $V_D$ )

# ADG419

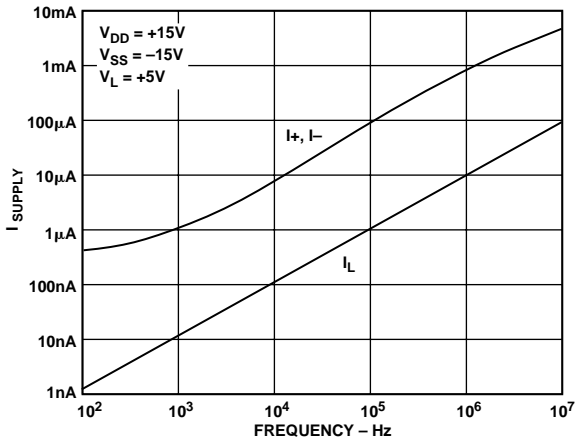


Figure 7. Supply Current vs. Input Switching Frequency

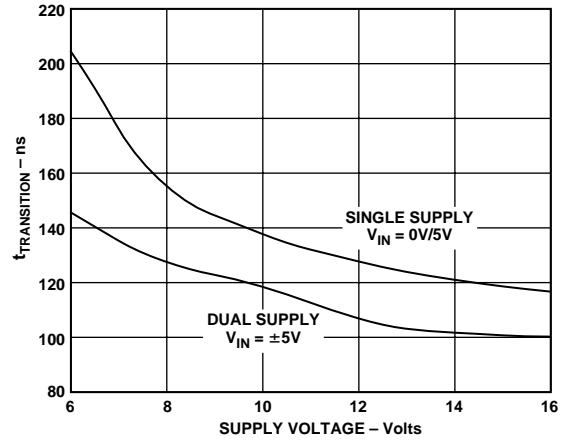
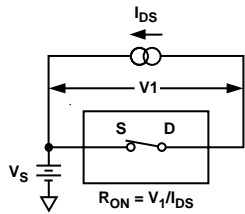
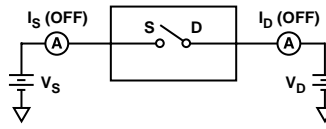


Figure 8. Transition Time vs. Power Supply Voltage

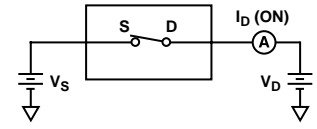
## Test Circuits



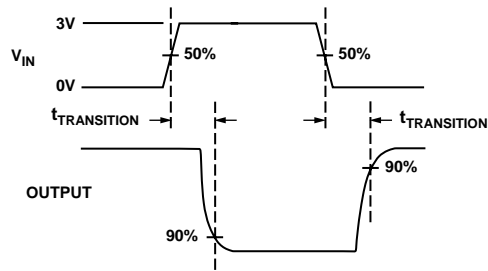
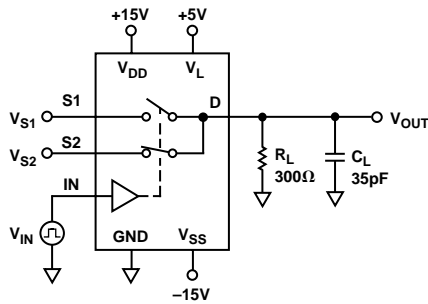
Test Circuit 1. On Resistance



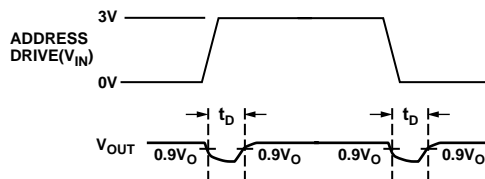
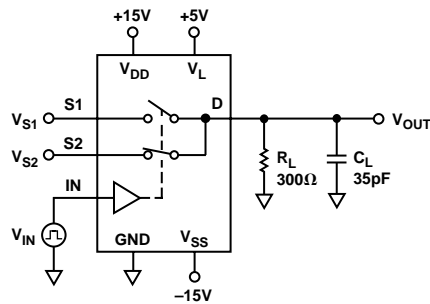
Test Circuit 2. Off Leakage



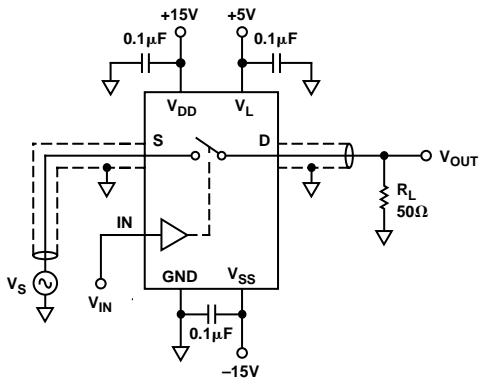
Test Circuit 3. On Leakage



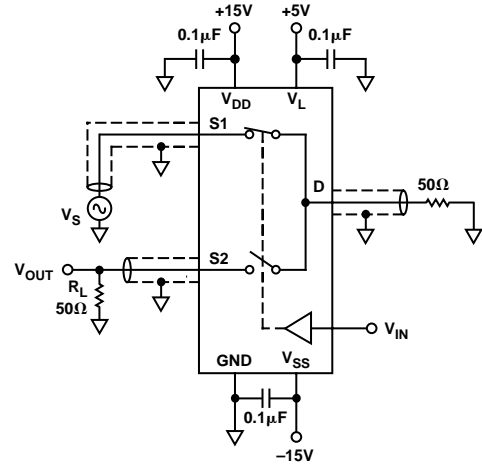
Test Circuit 4. Transition Time,  $t_{\text{TRANSITION}}$



Test Circuit 5. Break-Before-Make Time Delay,  $t_D$



Test Circuit 6. Off Isolation



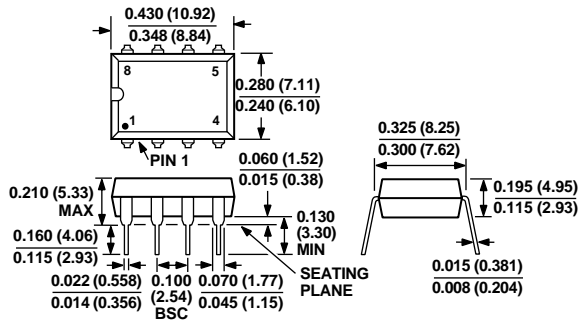
CHANNEL-TO-CHANNEL CROSSTALK =  $20 \times \text{LOG} |V_S/V_{OUT}|$

Test Circuit 7. Crosstalk

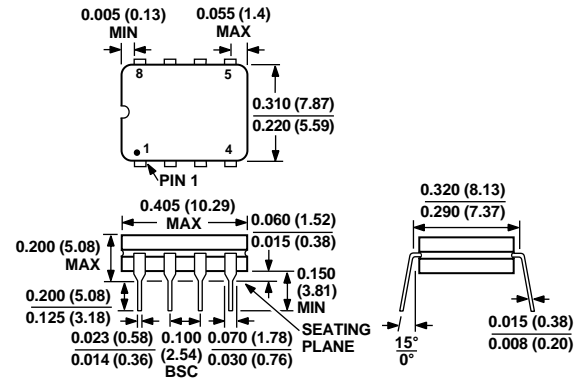
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

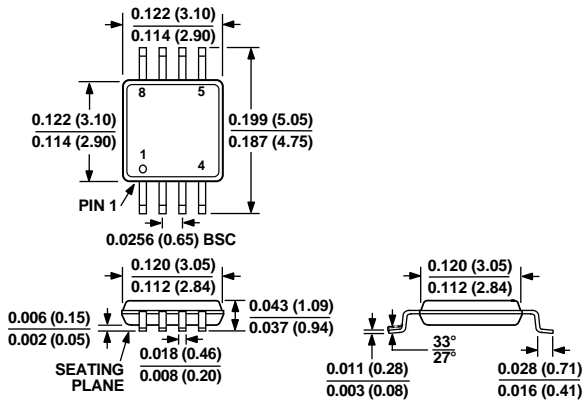
### 8-Lead Plastic DIP (N-8)



### 8-Lead Cerdip (Q-8)



### 8-Lead $\mu$ SOIC (RM-8)



### 8-Lead SOIC (SO-8) (Narrow Body)

