

## ADG411/ADG412/ADG413

### FEATURES

**44 V Supply Maximum Ratings**  
**±15 V Analog Signal Range**  
**Low On Resistance (<35 Ω)**  
**Ultralow Power Dissipation (35 μW)**  
**Fast Switching Times**  
 $t_{ON} < 175 \text{ ns}$   
 $t_{OFF} < 145 \text{ ns}$   
**TTL/CMOS Compatible**  
**Plug-In Replacement for DG411/DG412/DG413**

### APPLICATIONS

**Audio and Video Switching**  
**Automatic Test Equipment**  
**Precision Data Acquisition**  
**Battery Powered Systems**  
**Sample Hold Systems**  
**Communication Systems**

### GENERAL DESCRIPTION

The ADG411, ADG412 and ADG413 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC<sup>2</sup>MOS process which provides low power dissipation yet gives high switching speed and low on resistance.

The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. Fast switching speed coupled with high signal bandwidth also make the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

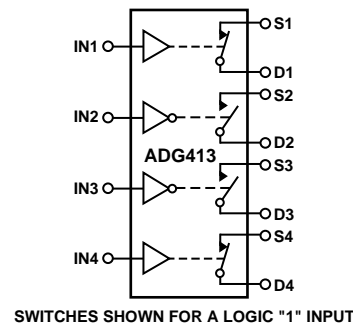
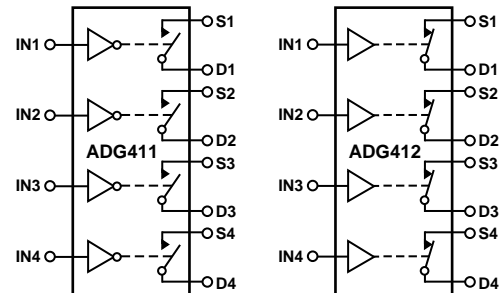
The ADG411, ADG412 and ADG413 contain four independent SPST switches. The ADG411 and ADG412 differ only in that the digital control logic is inverted. The ADG411 switches are turned on with a logic low on the appropriate control input, while a logic high is required for the ADG412. The ADG413 has two switches with digital control logic similar to that of the ADG411 while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when ON and each has an input signal range that extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

### REV. A

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### FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

### PRODUCT HIGHLIGHTS

- Extended Signal Range**  
 The ADG411, ADG412 and ADG413 are fabricated on an enhanced LC<sup>2</sup>MOS, giving an increased signal range which extends fully to the supply rails.
- Ultralow Power Dissipation**
- Low R<sub>ON</sub>**
- Break-Before-Make Switching**  
 This prevents channel shorting when the switches are configured as a multiplexer.
- Single Supply Operation**  
 For applications where the analog signal is unipolar, the ADG411, ADG412 and ADG413 can be operated from a single rail power supply. The parts are fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

# ADG411/ADG412/ADG413—SPECIFICATIONS<sup>1</sup>

Dual Supply ( $V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $V_L = +5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted)

Parameter	B Version -40°C to +25°C +85°C		T Version -55°C to +25°C +125°C		Units	Test Conditions/Comments
	+25°C	+85°C	+25°C	+125°C		
ANALOG SWITCH Analog Signal Range $R_{ON}$	25 35	$V_{DD}$ to $V_{SS}$ 45	25 35	$V_{DD}$ to $V_{SS}$ 45	V $\Omega$ typ $\Omega$ max	$V_D = \pm 8.5\text{ V}$ , $I_S = -10\text{ mA}$ ; $V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$
LEAKAGE CURRENTS Source OFF Leakage $I_S$ (OFF) Drain OFF Leakage $I_D$ (OFF) Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.1$ $\pm 0.25$ $\pm 0.1$ $\pm 0.25$ $\pm 0.1$ $\pm 0.4$	$\pm 5$ $\pm 5$ $\pm 5$ $\pm 10$	$\pm 0.1$ $\pm 0.25$ $\pm 0.1$ $\pm 0.25$ $\pm 0.1$ $\pm 0.4$	$\pm 20$ $\pm 20$ $\pm 20$ $\pm 40$	nA typ nA max nA typ nA max nA typ nA max	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ $V_D = \pm 15.5\text{ V}$ , $V_S = \mp 15.5\text{ V}$ ; Test Circuit 2 $V_D = \pm 15.5\text{ V}$ , $V_S = \mp 15.5\text{ V}$ ; Test Circuit 2 $V_D = V_S = \pm 15.5\text{ V}$ ; Test Circuit 3
DIGITAL INPUTS Input High Voltage, $V_{INH}$ Input Low Voltage, $V_{INL}$ Input Current $I_{INL}$ or $I_{INH}$		2.4 0.8  $\pm 0.5$		2.4 0.8  $\pm 0.5$	V min V max  $\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
DYNAMIC CHARACTERISTICS <sup>2</sup> $t_{ON}$ $t_{OFF}$ Break-Before-Make Time Delay, $t_D$ (ADG413 Only) Charge Injection OFF Isolation Channel-to-Channel Crosstalk $C_S$ (OFF) $C_D$ (OFF) $C_D$ , $C_S$ (ON)	110 100 25 5 68 85 9 9 35	175 145	110 100 25 5 68 85 9 9 35	175 145	ns typ ns max ns typ ns max ns typ pC typ dB typ dB typ pF typ pF typ pF typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = \pm 10\text{ V}$ ; Test Circuit 4 $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = \pm 10\text{ V}$ ; Test Circuit 4 $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1} = V_{S2} = +10\text{ V}$ ; Test Circuit 5 $V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 10\text{ nF}$ ; Test Circuit 6 $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 7 $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 8 $f = 1\text{ MHz}$ $f = 1\text{ MHz}$ $f = 1\text{ MHz}$
POWER REQUIREMENTS  $I_{DD}$  $I_{SS}$  $I_L$	0.0001 1 0.0001 1 0.0001 1	5 5 5 5	0.0001 1 0.0001 1 0.0001 1	5 5 5 5	$\mu\text{A}$ typ $\mu\text{A}$ max $\mu\text{A}$ typ $\mu\text{A}$ max $\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ Digital Inputs = 0 V or 5 V

## NOTES

<sup>1</sup>Temperature ranges are as follows: B Versions: -40°C to +85°C; T Versions: -55°C to +125°C.

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

**Single Supply** ( $V_{DD} = +12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $V_L = +5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted)

Parameter	B Version		T Version		Units	Test Conditions/Comments
	+25°C	-40°C to +85°C	+25°C	-55°C to +125°C		
ANALOG SIGNAL RANGE $R_{ON}$	40 80	0 V to $V_{DD}$ 100	40 80	0 V to $V_{DD}$ 100	V $\Omega$ typ $\Omega$ max	$0 < V_D = 8.5\text{ V}$ , $I_S = -10\text{ mA}$ ; $V_{DD} = +10.8\text{ V}$
LEAKAGE CURRENTS						$V_{DD} = +13.2\text{ V}$ $V_D = 12.2/1\text{ V}$ , $V_S = 1/12.2\text{ V}$ ; Test Circuit 2
Source OFF Leakage $I_S$ (OFF)	$\pm 0.1$ $\pm 0.25$	$\pm 5$	$\pm 0.1$ $\pm 0.25$	$\pm 20$	nA typ nA max	Test Circuit 2
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.1$ $\pm 0.25$	$\pm 5$	$\pm 0.1$ $\pm 0.25$	$\pm 20$	nA typ nA max	$V_D = 12.2/1\text{ V}$ , $V_S = 1/12.2\text{ V}$ ; Test Circuit 2
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.1$ $\pm 0.4$	$\pm 10$	$\pm 0.1$ $\pm 0.4$	$\pm 40$	nA typ nA max	$V_D = V_S = +12.2\text{ V}/+1\text{ V}$ ; Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, $V_{INH}$		2.4		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8		0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005	$\pm 0.5$	0.005	$\pm 0.5$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
DYNAMIC CHARACTERISTICS <sup>2</sup>						
$t_{ON}$	175	250	175	250	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = +8\text{ V}$ ; Test Circuit 4
$t_{OFF}$	95	125	95	125	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = +8\text{ V}$ ; Test Circuit 4
Break-Before-Make Time Delay, $t_D$ (ADG413 Only)	25		25		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1} = V_{S2} = +10\text{ V}$ ; Test Circuit 5
Charge Injection	25		25		pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 10\text{ nF}$ ; Test Circuit 6
OFF Isolation	68		68		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 7
Channel-to-Channel Crosstalk	85		85		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 8
$C_S$ (OFF)	9		9		pF typ	$f = 1\text{ MHz}$
$C_D$ (OFF)	9		9		pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	35		35		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS						$V_{DD} = +13.2\text{ V}$ Digital Inputs = 0 V or 5 V
$I_{DD}$	0.0001 1	5	0.0001 1	5	$\mu\text{A}$ typ $\mu\text{A}$ max	
$I_L$	0.0001 1	5	0.0001 1	5	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_L = +5.25\text{ V}$

NOTES

<sup>1</sup>Temperature ranges are as follows: B Versions: -40°C to +85°C; T Versions: -55°C to +125°C.

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

**Truth Table (ADG411/ADG412)**

ADG411 In	ADG412 In	Switch Condition
0	1	ON
1	0	OFF

**Truth Table (ADG413)**

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

# ADG411/ADG412/ADG413

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>DD</sub> to V <sub>SS</sub> .....	+44 V
V <sub>DD</sub> to GND .....	-0.3 V to +25 V
V <sub>SS</sub> to GND .....	+0.3 V to -25 V
V <sub>L</sub> to GND .....	-0.3 V to V <sub>DD</sub> + 0.3 V
Analog, Digital Inputs <sup>2</sup> .....	V <sub>SS</sub> -2 V to V <sub>DD</sub> +2 V or 30 mA, Whichever Occurs First
Continuous Current, S or D .....	30 mA
Peak Current, S or D .....	100 mA
(Pulsed at 1 ms, 10% Duty Cycle max)	
Operating Temperature Range	
Industrial (B Version) .....	-40°C to +85°C
Extended (T Version) .....	-55°C to +125°C
Storage Temperature Range .....	-65°C to +150°C
Junction Temperature .....	+150°C
Cerdip Package, Power Dissipation .....	900 mW
θ <sub>JA</sub> Thermal Impedance .....	76°C/W
Lead Temperature, Soldering (10 sec) .....	+300°C
Plastic Package, Power Dissipation .....	470 mW
θ <sub>JA</sub> Thermal Impedance .....	117°C/W
Lead Temperature, Soldering (10 sec) .....	+260°C
SOIC Package, Power Dissipation .....	600 mW
θ <sub>JA</sub> Thermal Impedance .....	77°C/W
TSSOP Package, Power Dissipation .....	450 mW
θ <sub>JA</sub> Thermal Impedance .....	115°C/W
θ <sub>JC</sub> Thermal Impedance .....	35°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec) .....	+215°C
Infrared (15 sec) .....	+220°C

### NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

<sup>2</sup>Overtoggles at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Option <sup>2</sup>
ADG411BN	-40°C to +85°C	N-16
ADG411BR	-40°C to +85°C	R-16A
ADG411TQ	-55°C to +125°C	Q-16
ADG411BRU	-40°C to +85°C	RU-16
ADG412BN	-40°C to +85°C	N-16
ADG412BR	-40°C to +85°C	R-16A
ADG412TQ	-55°C to +125°C	Q-16
ADG413BN	-40°C to +85°C	N-16
ADG413BR	-40°C to +85°C	R-16A

### NOTES

<sup>1</sup>To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.

<sup>2</sup>N = Plastic DIP; R = 0.15" Small Outline IC (SOIC); RU= Thin Shrink Small Outline (TSSOP); Q = Cerdip.

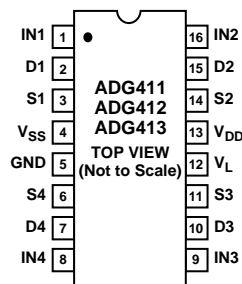
## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG411/ADG412/ADG413 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## TERMINOLOGY

V <sub>DD</sub>	Most positive power supply potential.
V <sub>SS</sub>	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.
V <sub>L</sub>	Logic power supply (+5 V).
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
R <sub>ON</sub>	Ohmic resistance between D and S.
I <sub>S</sub> (OFF)	Source leakage current with the switch "OFF."
I <sub>D</sub> (OFF)	Drain leakage current with the switch "OFF."
I <sub>D, I<sub>S</sub></sub> (ON)	Channel leakage current with the switch "ON."
V <sub>D</sub> (V <sub>S</sub> )	Analog voltage on terminals D, S.
C <sub>S</sub> (OFF)	"OFF" switch source capacitance.
C <sub>D</sub> (OFF)	"OFF" switch drain capacitance.
C <sub>D, C<sub>S</sub></sub> (ON)	"ON" switch capacitance.
t <sub>ON</sub>	Delay between applying the digital control input and the output switching on.
t <sub>OFF</sub>	Delay between applying the digital control input and the output switching off.
t <sub>D</sub>	"OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.

## PIN CONFIGURATION (DIP/SOIC)



## Typical Performance Graphs

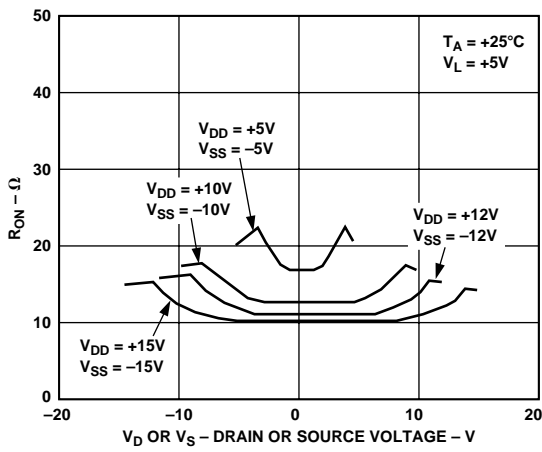


Figure 1. On Resistance as a Function of  $V_D$  ( $V_S$ ) Dual Supplies

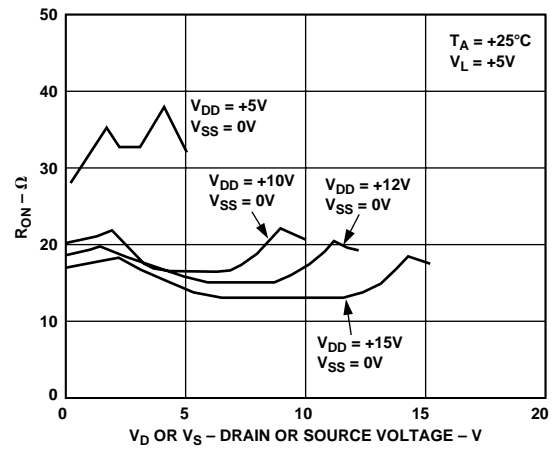


Figure 4. On Resistance as a Function of  $V_D$  ( $V_S$ ) Single Supply

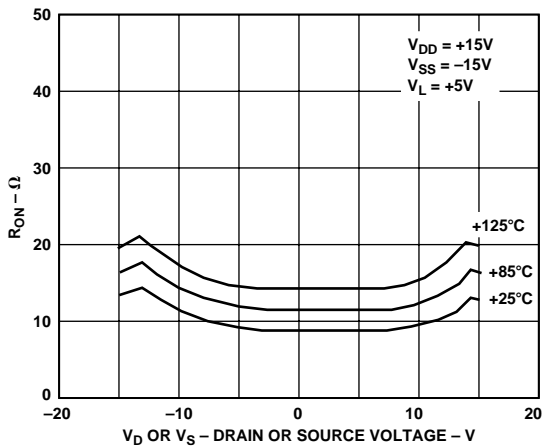


Figure 2. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures

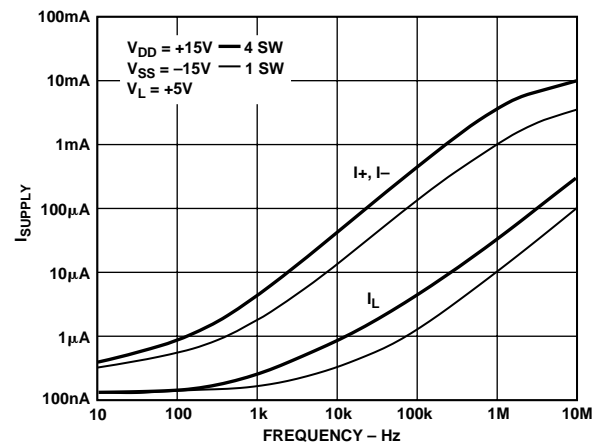


Figure 5. Supply Current vs. Input Switching Frequency

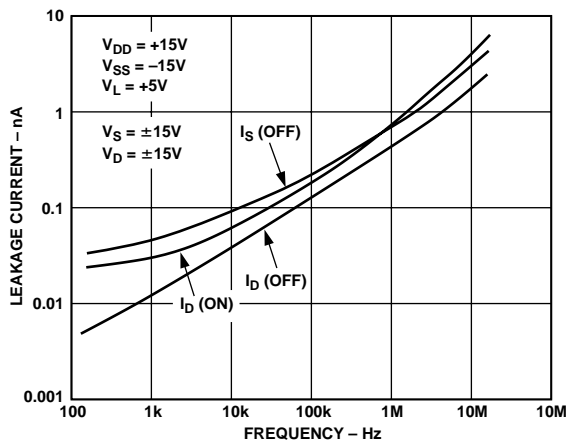


Figure 3. Leakage Currents as a Function of Temperature

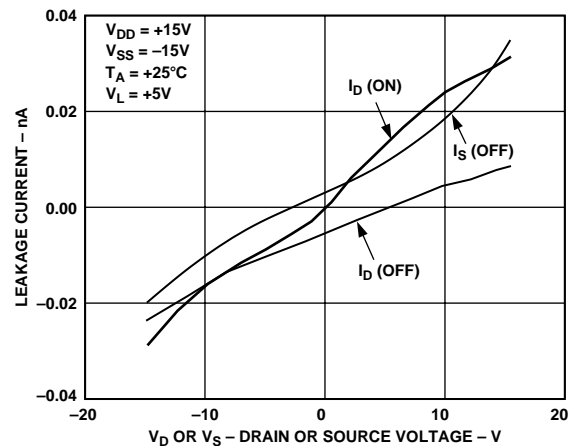


Figure 6. Leakage Currents as a Function of  $V_D$  ( $V_S$ )

# ADG411/ADG412/ADG413

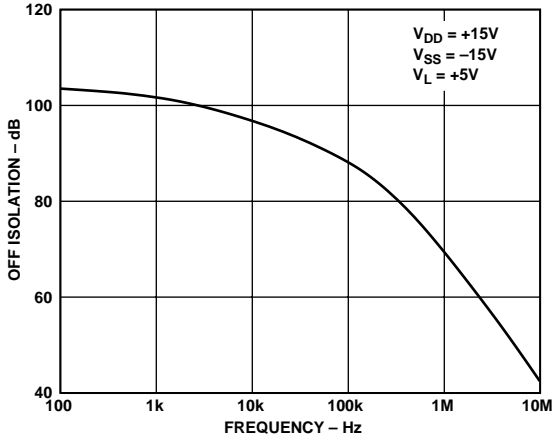


Figure 7. Off Isolation vs. Frequency

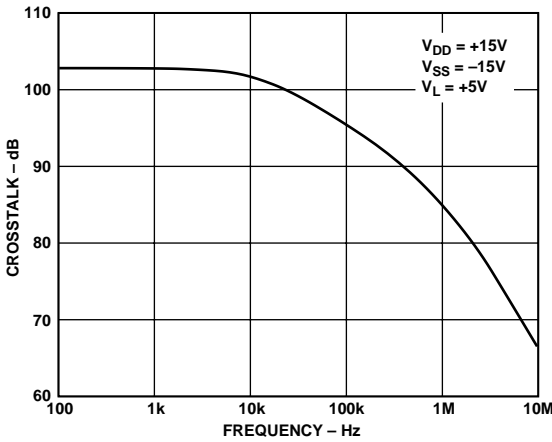


Figure 8. Crosstalk vs. Frequency

## APPLICATION

Figure 9 illustrates a precise, fast, sample-and-hold circuit. An AD845 is used as the input buffer while the output operational amplifier is an AD711. During the track mode, SW1 is closed and the output  $V_{OUT}$  follows the input signal  $V_{IN}$ . In the hold mode, SW1 is opened and the signal is held by the hold capacitor  $C_H$ .

Due to switch and capacitor leakage, the voltage on the hold capacitor will decrease with time. The ADG411/ADG412/ADG413 minimizes this droop due to its low leakage specifications. The droop rate is further minimized by the use of a poly-styrene hold capacitor. The droop rate for the circuit shown is typically  $30 \mu\text{V}/\mu\text{s}$ .

A second switch, SW2, which operates in parallel with SW1, is included in this circuit to reduce pedestal error. Since both switches will be at the same potential, they will have a differential effect on the op amp AD711, which will minimize charge injection effects. Pedestal error is also reduced by the compensation network  $R_C$  and  $C_C$ . This compensation network also reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the  $\pm 10 \text{ V}$  input range. Both the acquisition and settling times are 850 ns.

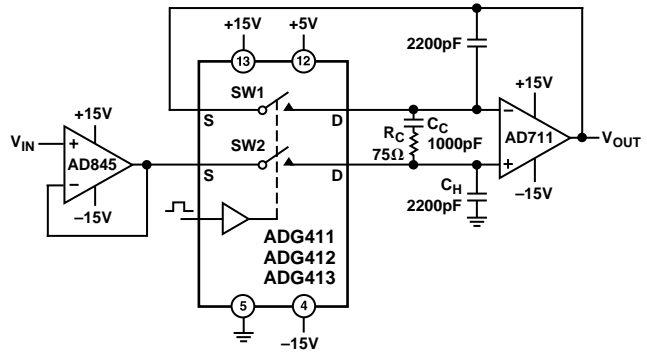
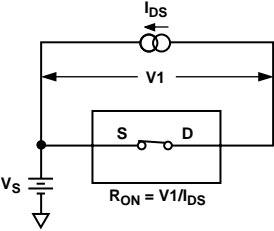
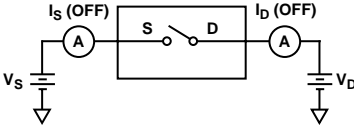


Figure 9. Fast, Accurate Sample-and-Hold

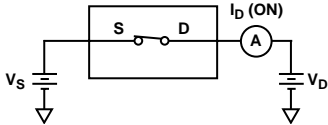
Test Circuits



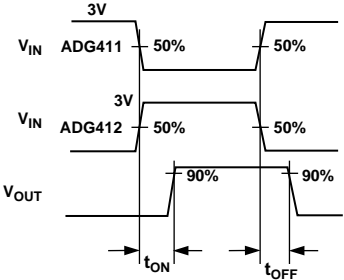
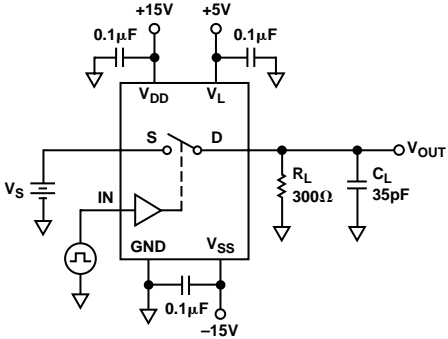
Test Circuit 1. On Resistance



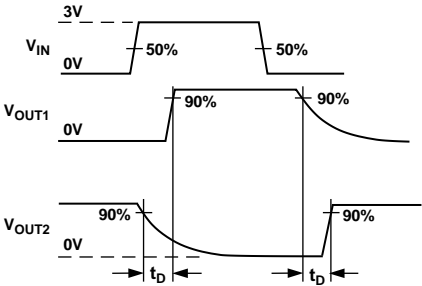
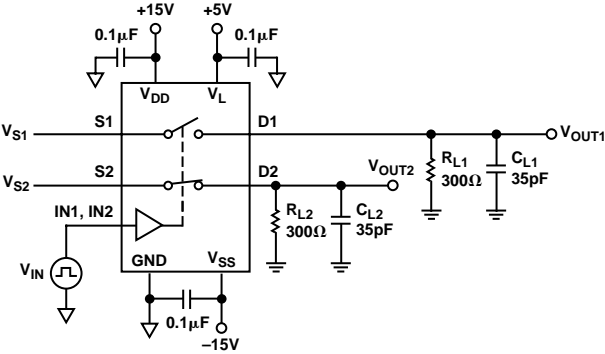
Test Circuit 2. Off Leakage



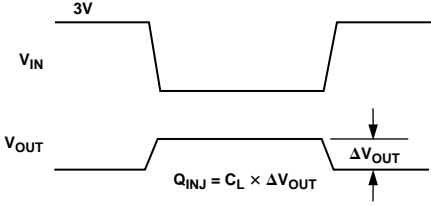
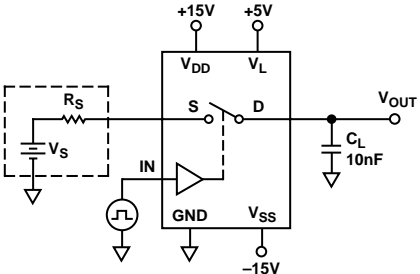
Test Circuit 3. On Leakage



Test Circuit 4. Switching Times

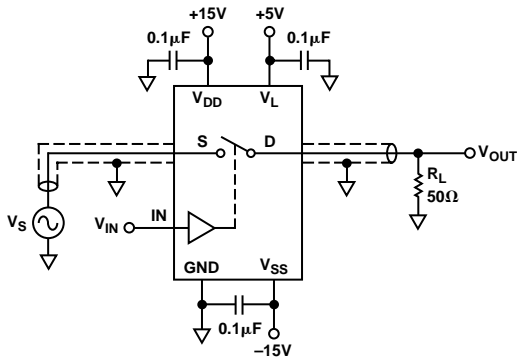


Test Circuit 5. Break-Before-Make Time Delay

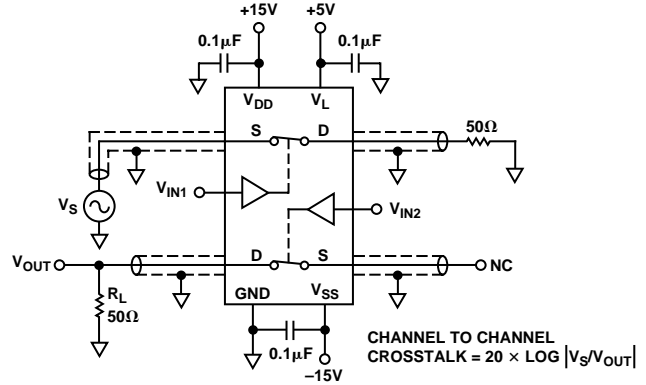


Test Circuit 6. Charge Injection

# ADG411/ADG412/ADG413



Test Circuit 7. Off Isolation

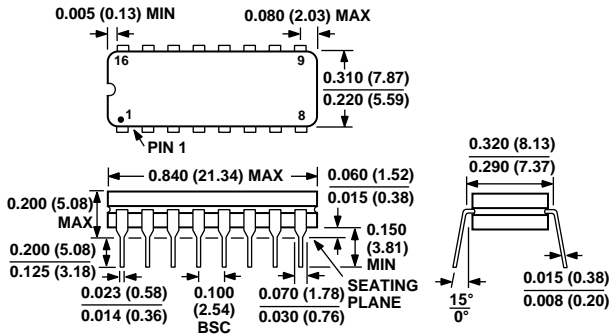


Test Circuit 8. Channel-to-Channel Crosstalk

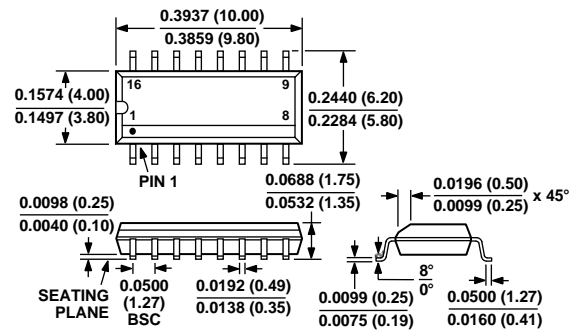
## MECHANICAL INFORMATION

Dimensions are shown in inches and (mm).

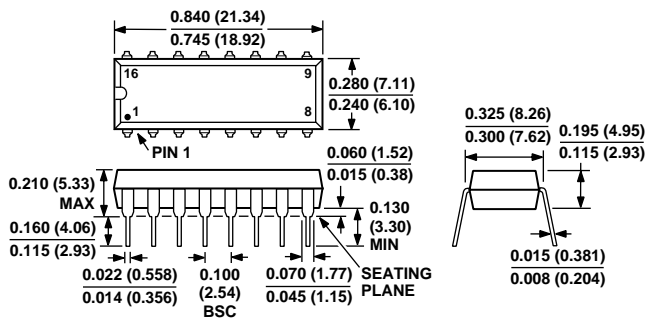
### 16-Lead Cerdip (Q-16)



### 16-Lead SOIC (R-16A)



### 16-Lead Plastic DIP (Narrow) (N-16)



### 16-Lead TSSOP (RU-16)

