NEC

MOS FIELD EFFECT TRANSISTOR
2SK3900

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3900 is N-channel MOS Field Effect Transistor designed for high current switching applications.

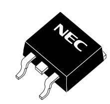
ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3900-ZP	TO-263 (MP-25ZP)

FEATURES

- Super low on-state resistance
  $R_{DS(on)1}$ = 8.0 mΩ MAX. (V_{GS} = 10 V, I_D = 41 A)
  $R_{DS(on)2}$ = 10 mΩ MAX. (V_{GS} = 4.5 V, I_D = 41 A)
- Low C_{iss}: C_{iss} = 3500 pF TYP.
- Built-in gate protection diode

(TO-263)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	60	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±82	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±246	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	104	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Energy Note2	E_{AS}	141	mJ
Repetitive Avalanche Current Note3	I_{AR}	37.5	A
Repetitive Avalanche Energy Note3	E_{AR}	141	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 30 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

3. R_G = 25 Ω, $T_{ch(peak)}$ ≤ 150°C

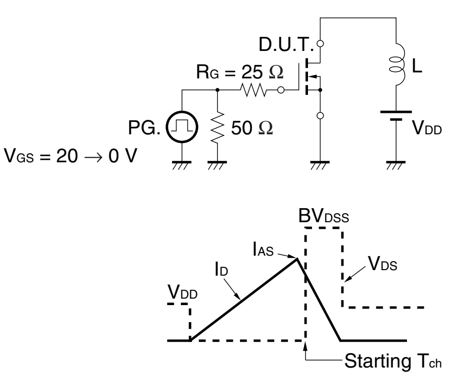
Document No. D17175EJ1V0DS00 (1st edition)
Date Published May 2004 NS CP(K)
Printed in Japan

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

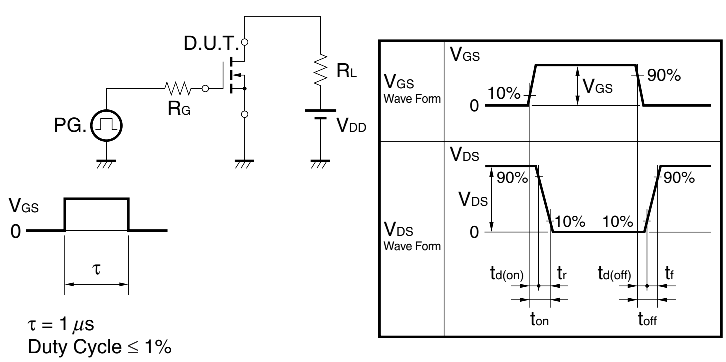
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	| y_{fs} |	V_{DS} = 10 V, I_D = 41 A	28.1	56		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 41 A		6.3	8.0	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 41 A		7.4	10	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		3500		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		660		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		240		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 41 A		18		ns
Rise Time	t_r	V_{GS} = 10 V		11		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		62		ns
Fall Time	t_f			5.5		ns
Total Gate Charge	Q_G	V_{DD} = 48 V		65.5		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		11.5		nC
Gate to Drain Charge	Q_{GD}	I_D = 82 A		16.5		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 82 A, V_{GS} = 0 V		0.95	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 82 A, V_{GS} = 0 V		41		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		61		nC

Note Pulsed

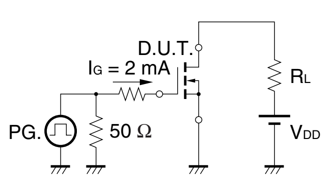
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

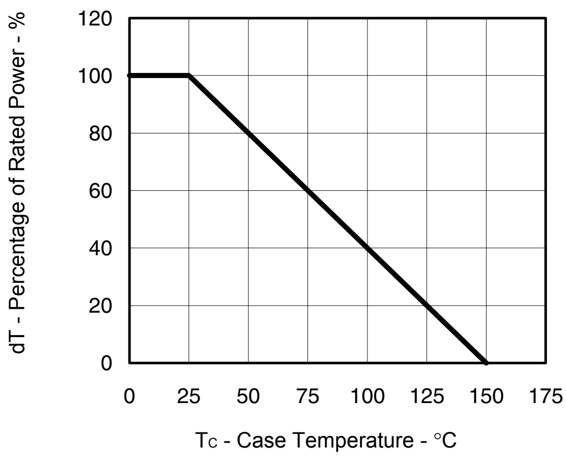


TEST CIRCUIT 3 GATE CHARGE

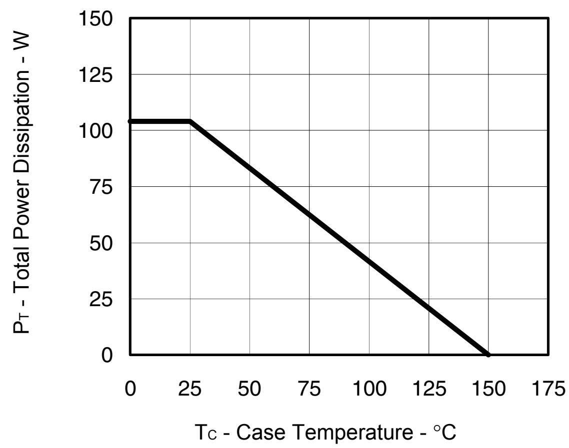


TYPICAL CHARACTERISTICS (T_A = 25°C)

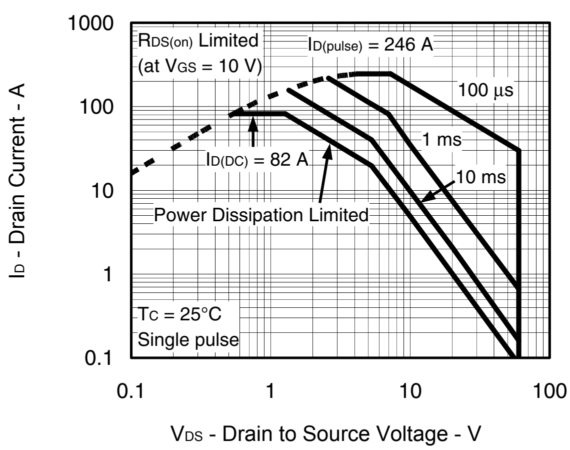
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



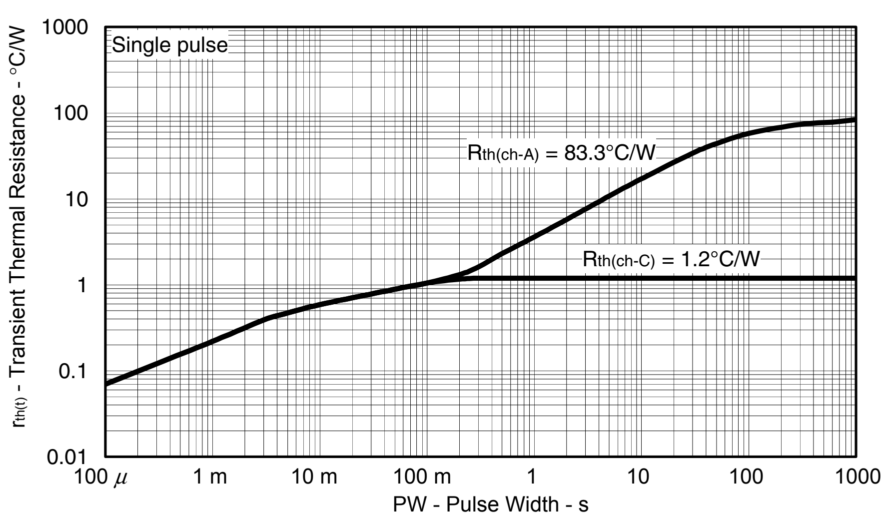
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



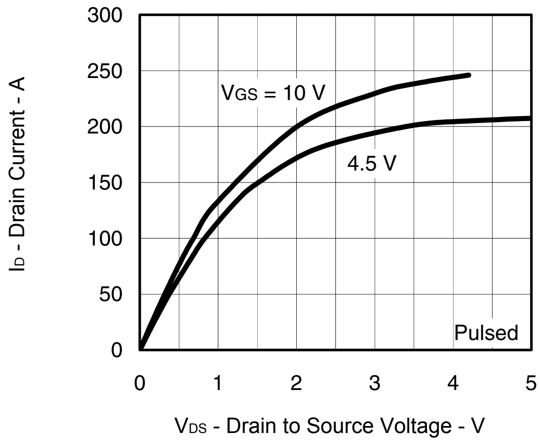
FORWARD BIAS SAFE OPERATING AREA



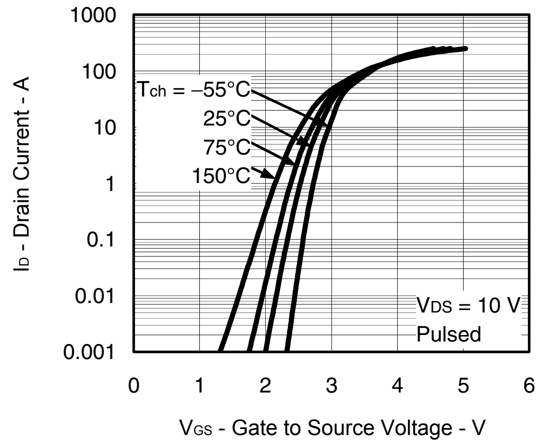
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



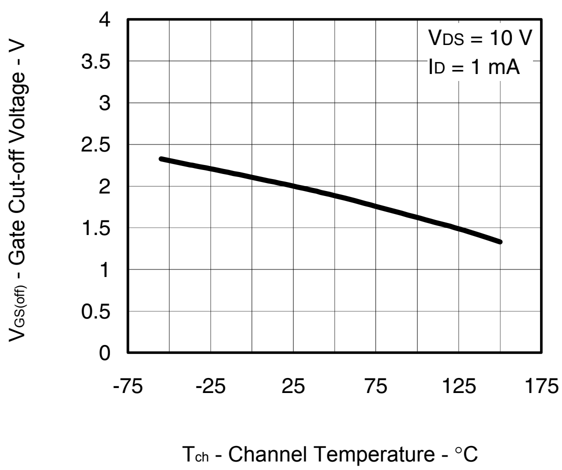
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



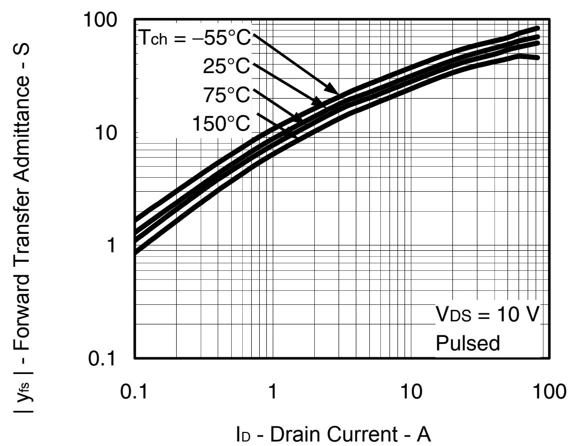
FORWARD TRANSFER CHARACTERISTICS



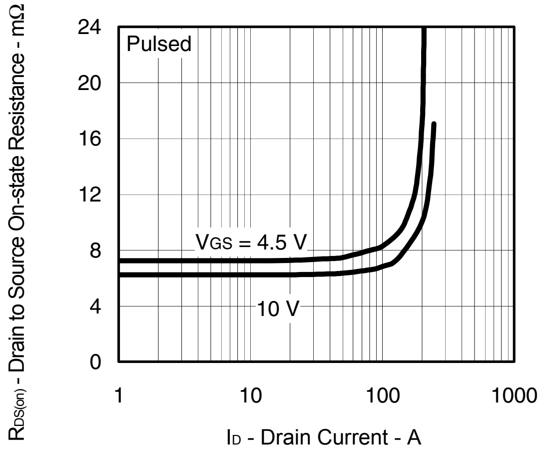
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



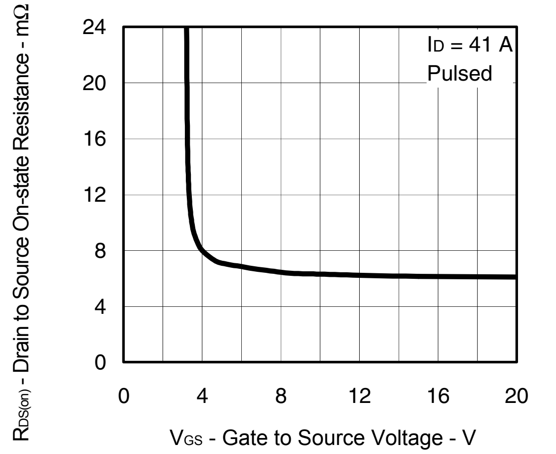
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



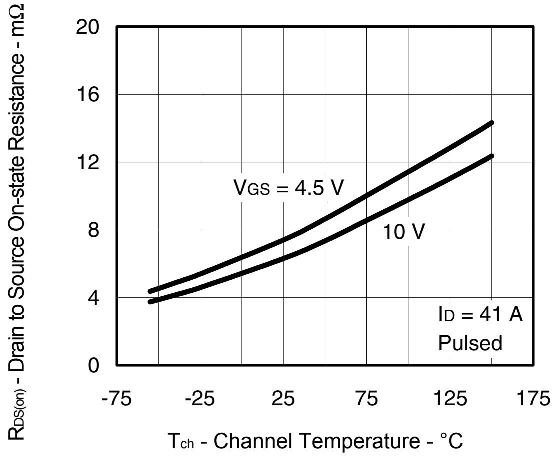
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



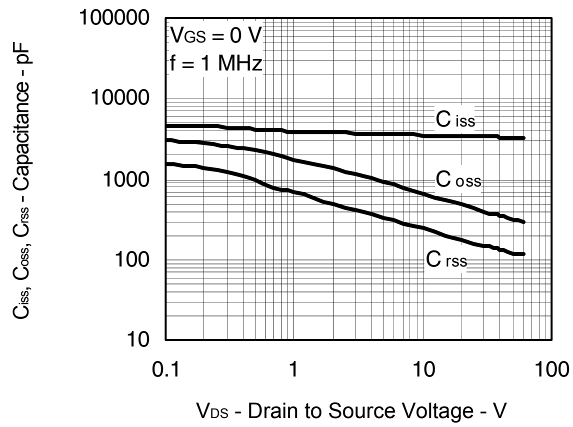
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



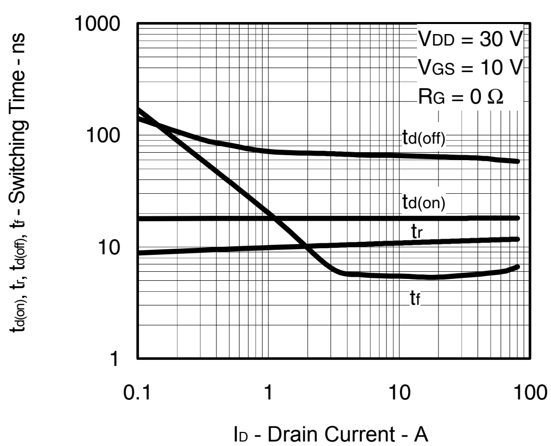
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



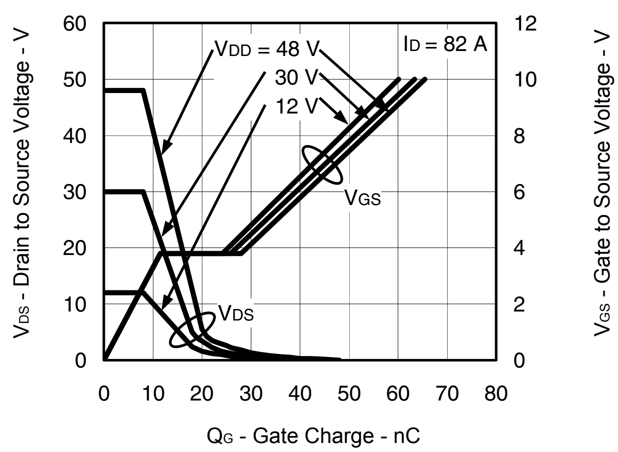
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



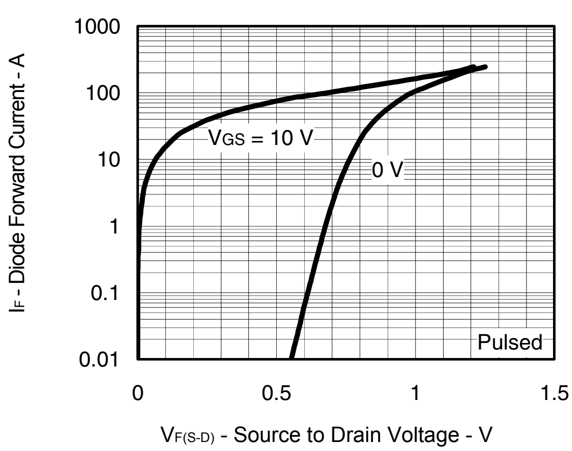
SWITCHING CHARACTERISTICS



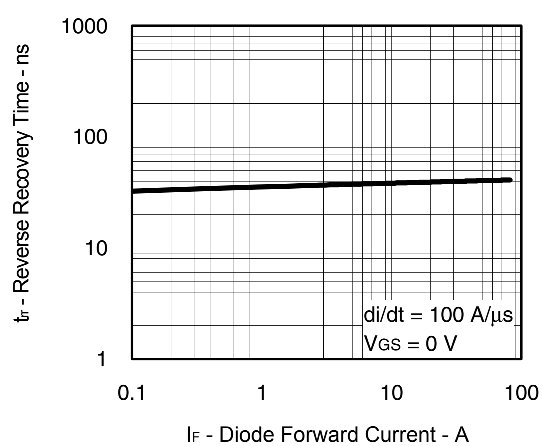
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



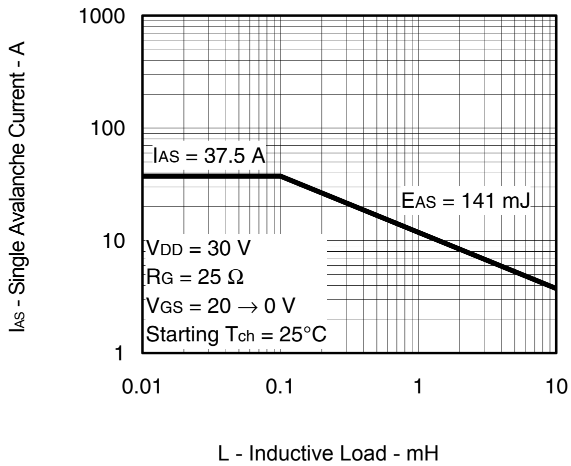
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



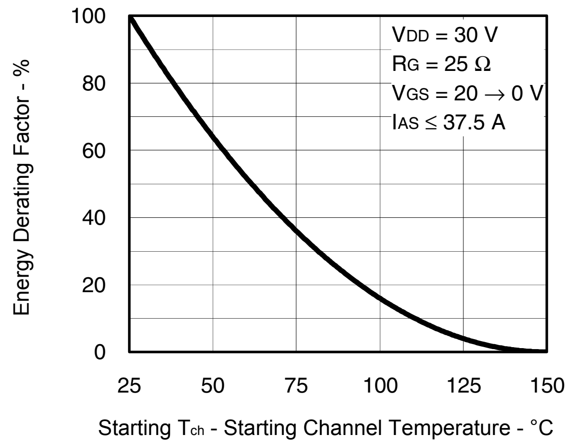
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

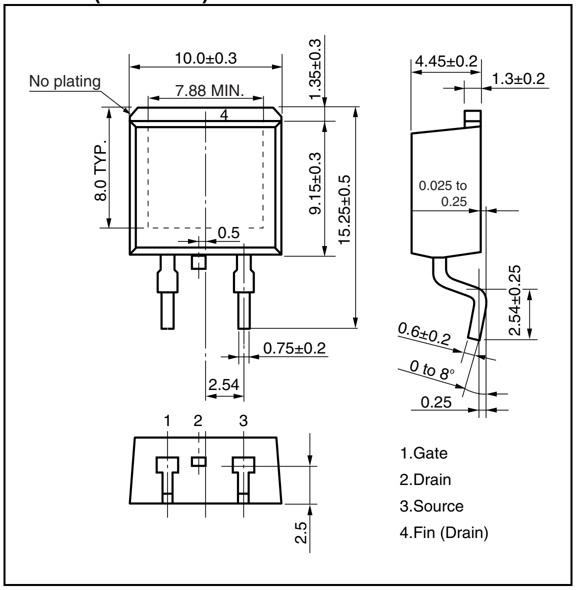


SINGLE AVALANCHE ENERGY
DERATING FACTOR

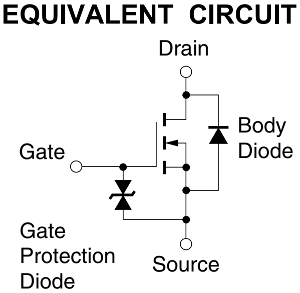


PACKAGE DRAWING (Unit: mm)

TO-263 (MP-25ZP)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.