(PNP) 2N6034, 2N6035, 2N6036 (NPN) 2N6038, 2N6039

Plastic Darlington Complementary Silicon Power Transistors

. . . designed for general−purpose amplifier and low−speed switching applications.

- ESD Ratings: Machine Model, C; > 400 V
  Human Body Model, 3B; > 8000 V
- Epoxy Meets UL 94, V−0 @ 1/8”

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage 2N6034 2N6035, 2N6038 2N6036, 2N6039	V_{CEO}	40 60 80	Vdc
Collector−Base Voltage 2N6034 2N6035, 2N6038 2N6036, 2N6039	V_{CBO}	40 60 80	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector Current − Continuous Peak	I_C	4.0 8.0	Adc Apk
Base Current	I_B	100	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 320	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

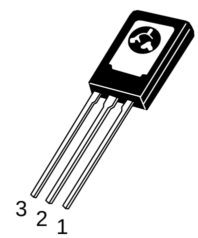
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	3.12	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	83.3	°C/W

ON Semiconductor®

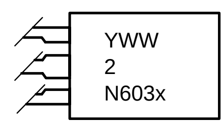
http://onsemi.com

4.0 A DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS 40, 60, 80 V, 40 W



TO−225AA
CASE 77
STYLE 1

MARKING DIAGRAM



x	= 4, 5, 6, 8, 9
Y	= Year
WW	= Work Week

ORDERING INFORMATION

Device	Package	Shipping
2N6034	TO−225AA	500 Units/Box
2N6035	TO−225AA	500 Units/Box
2N6036	TO−225AA	500 Units/Box
2N6038	TO−225AA	500 Units/Box
2N6039	TO−225AA	500 Units/Box

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage		$V_{CEO(sus)}$			Vdc
(I_C = 100 mAdc, I_B = 0)	2N6034		40	—	
	2N6035, 2N6038		60	—	
	2N6036, 2N6039		80	—	
Collector−Cutoff Current		I_{CEO}			μA
(V_{CE} = 40 Vdc, I_B = 0)	2N6034		—	100	
(V_{CE} = 60 Vdc, I_B = 0)	2N6035, 2N6038		—	100	
(V_{CE} = 80 Vdc, I_B = 0)	2N6036, 2N6039		—	100	
Collector−Cutoff Current		I_{CEX}			μA
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6034		—	100	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6035, 2N6038		—	100	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	2N6036, 2N6039		—	100	
(V_{CE} = 40 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6034		—	500	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6035, 2N6038		—	500	
(V_{CE} = 80 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 125°C)	2N6036, 2N6039		—	500	
Collector−Cutoff Current		I_{CBO}			mAdc
(V_{CB} = 40 Vdc, I_E = 0)	2N6034		—	0.5	
(V_{CB} = 60 Vdc, I_E = 0)	2N6035, 2N6038		—	0.5	
(V_{CB} = 80 Vdc, I_E = 0)	2N6036, 2N6039		—	0.5	
Emitter−Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			—
(I_C = 0.5 Adc, V_{CE} = 3.0 Vdc)			500	—	
(I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)			750	15,000	
(I_C = 4.0 Adc, V_{CE} = 3.0 Vdc)			100	—	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 2.0 Adc, I_B = 8.0 mAdc)			—	2.0	
(I_C = 4.0 Adc, I_B = 40 mAdc)			—	3.0	
Base−Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 40 mAdc)		$V_{BE(sat)}$	—	4.0	Vdc
Base−Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Small−Signal Current−Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	25	—	—
Output Capacitance		C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6034, 2N6035, 2N6036		—	200	
	2N6038, 2N6039		—	100	

*Indicates JEDEC Registered Data.

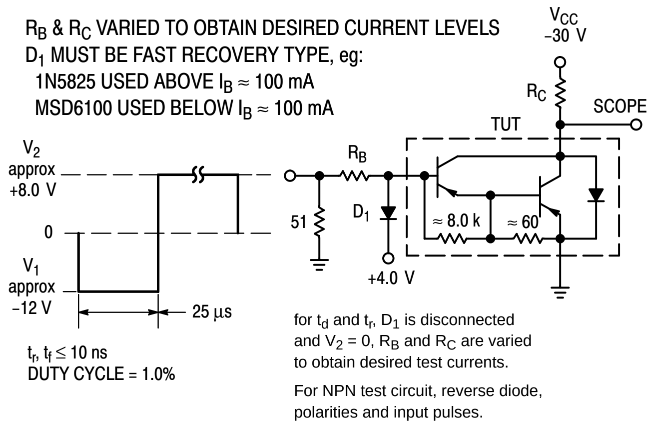


Figure 1. Switching Times Test Circuit

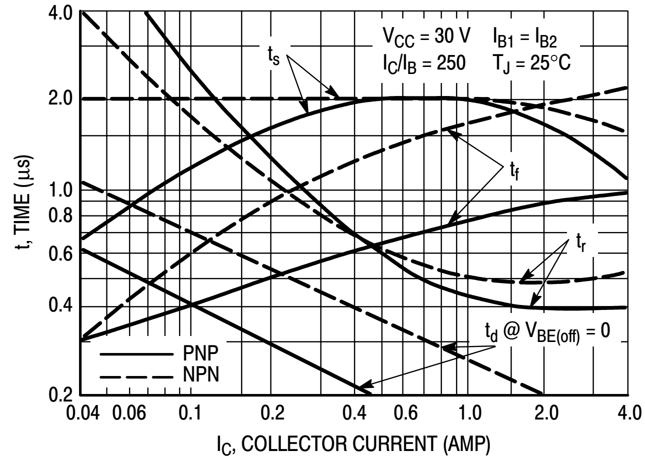


Figure 2. Switching Times

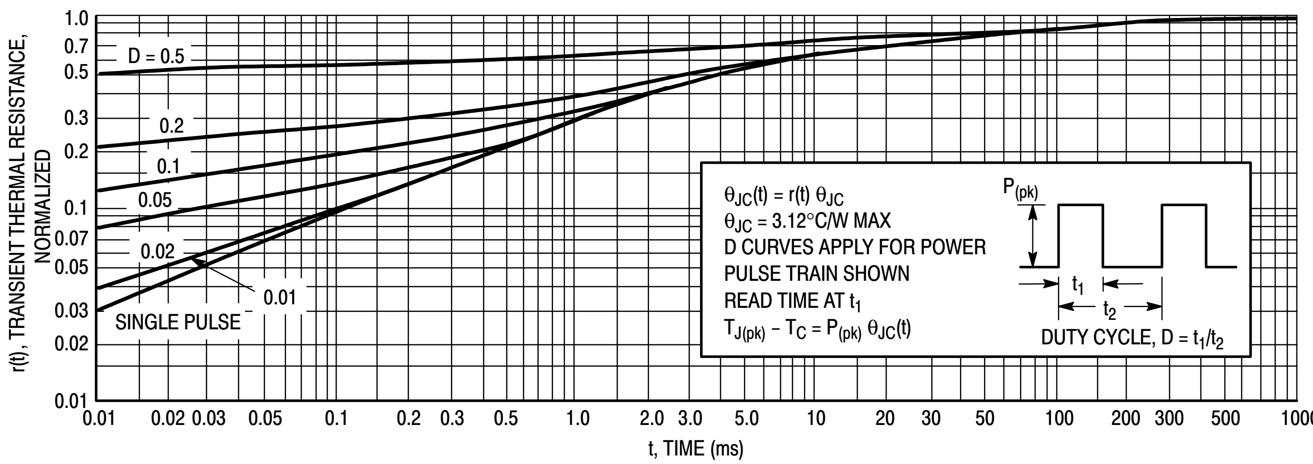


Figure 3. Thermal Response

ACTIVE−REGION SAFE−OPERATING AREA

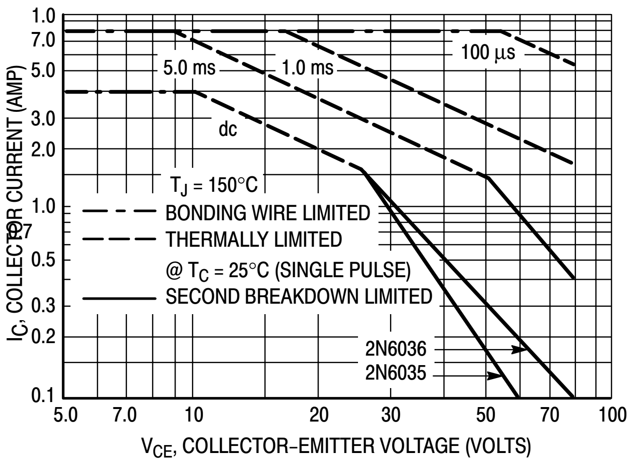


Figure 4. 2N6035, 2N6036

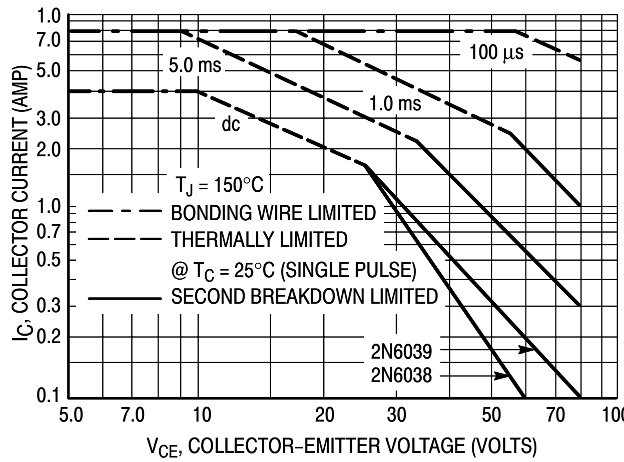


Figure 5. 2N6038, 2N6039

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 4 and 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

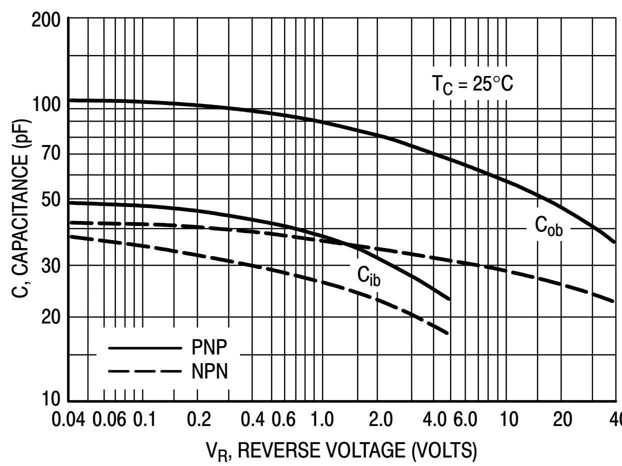


Figure 6. Capacitance

PNP
2N6034, 2N6035, 2N6036

NPN
2N6038, 2N6039

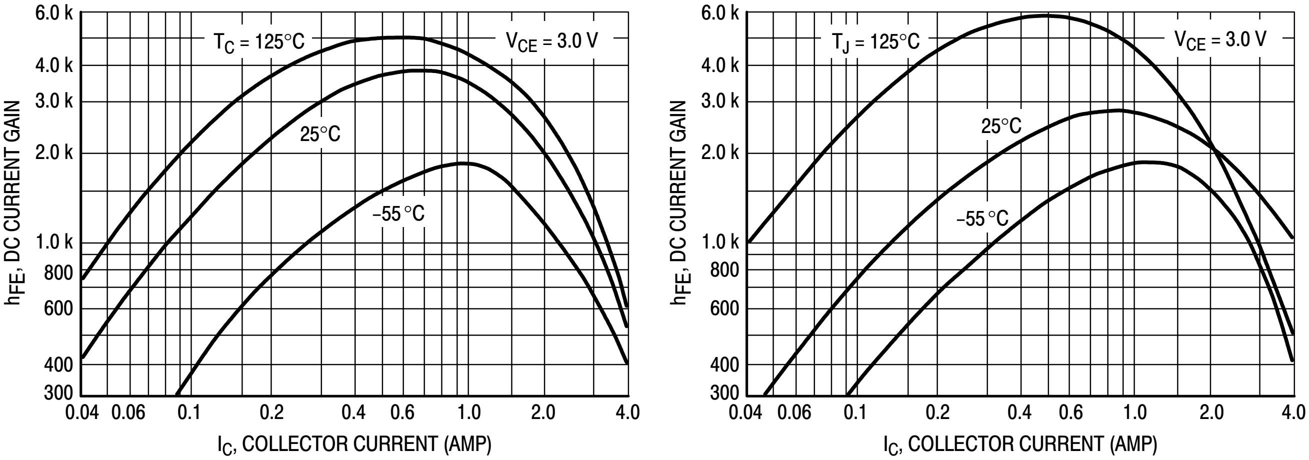


Figure 7. DC Current Gain

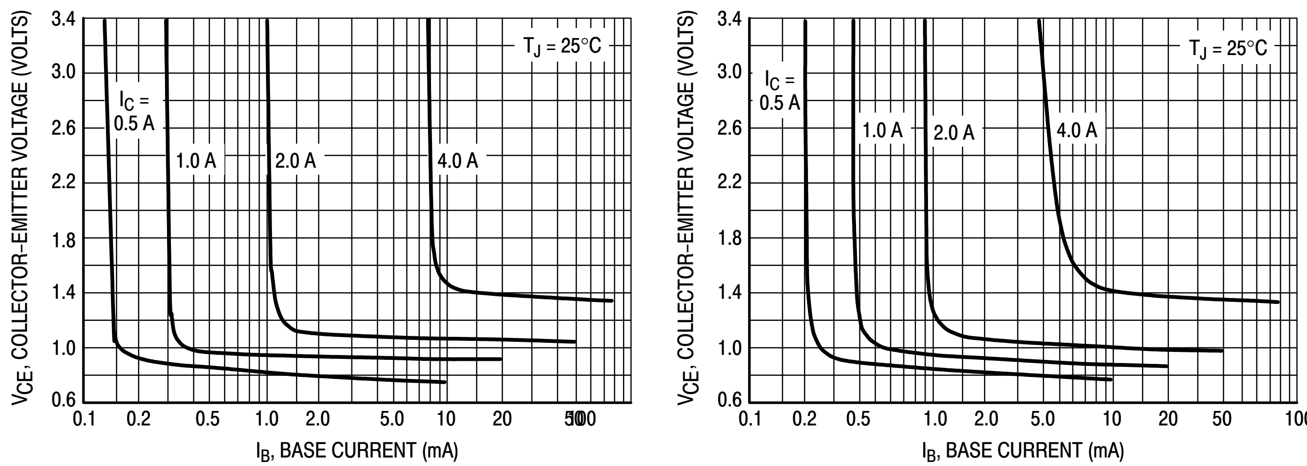


Figure 8. Collector Saturation Region

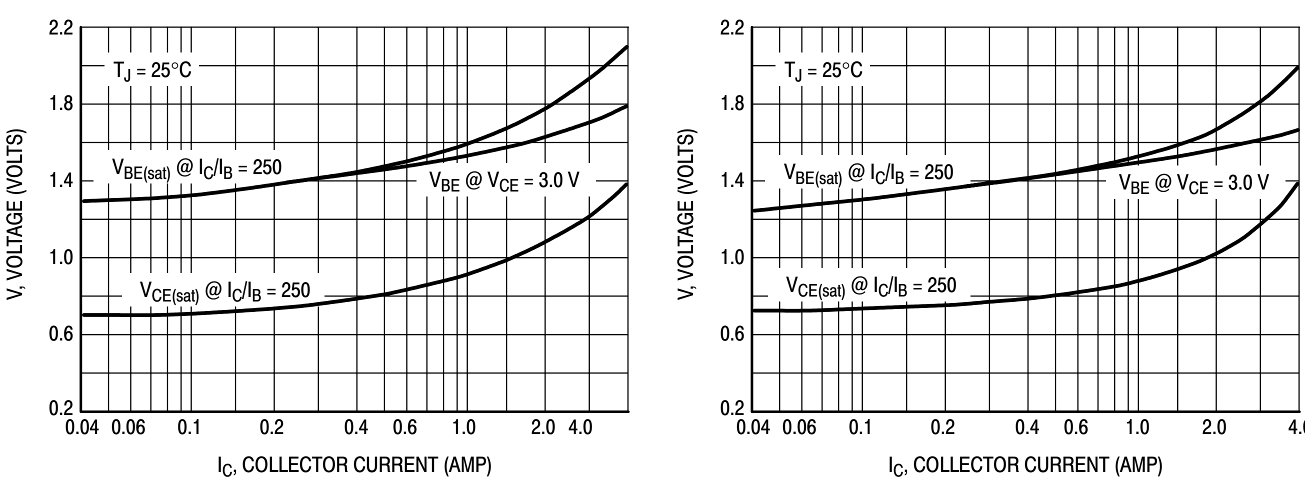
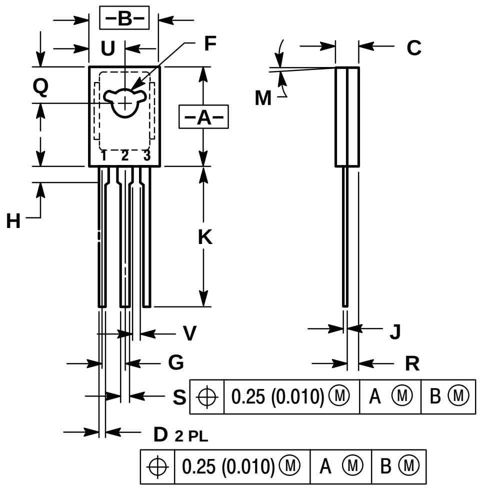


Figure 9. “On” Voltages

PACKAGE DIMENSIONS

TO−225AA
CASE 77−09
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 077−01 THRU −08 OBSOLETE, NEW STANDARD 077−09.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	---	1.02	---

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

PUBLICATION ORDERING INFORMATION

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